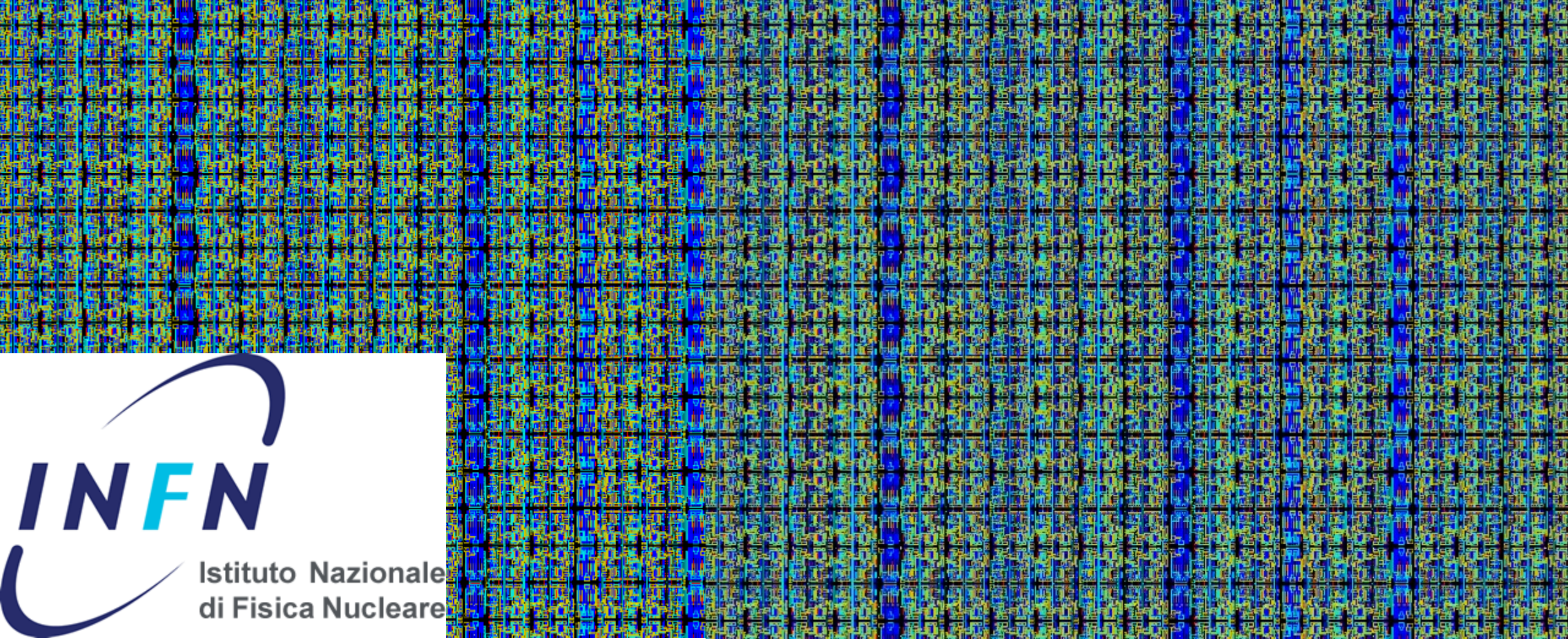


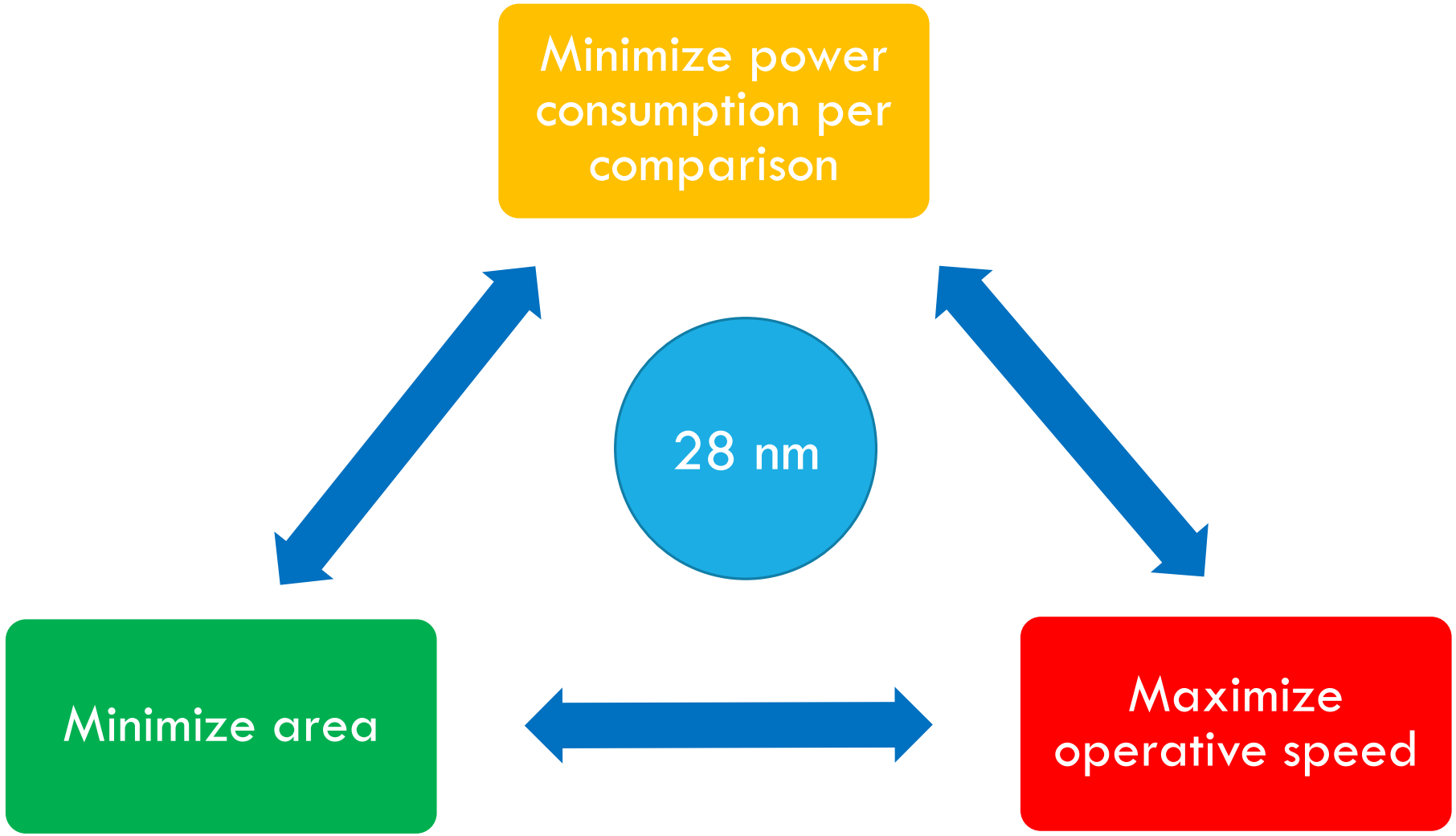
INFN
Istituto Nazionale
di Fisica Nucleare

XORAM MEMORY CELLS

Design and power consumption

L. Fontini – A. Stabile

ASSOCIATIVE MEMORY CELLS GOALS



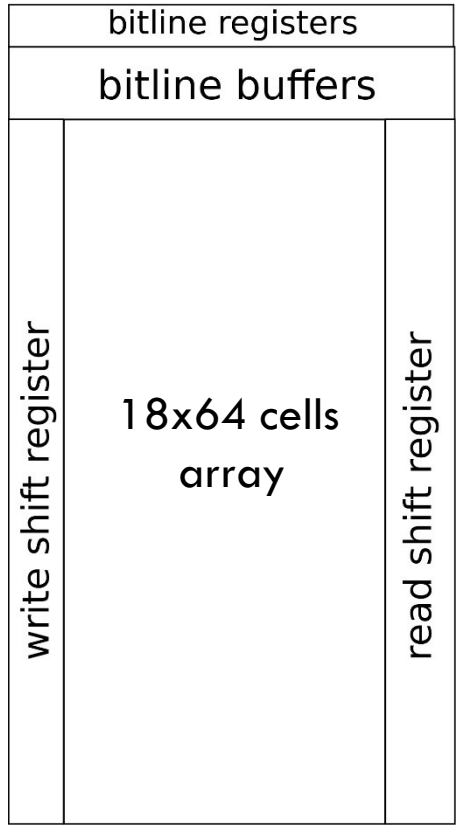
BLOCK ARCHITECTURE – AM07A

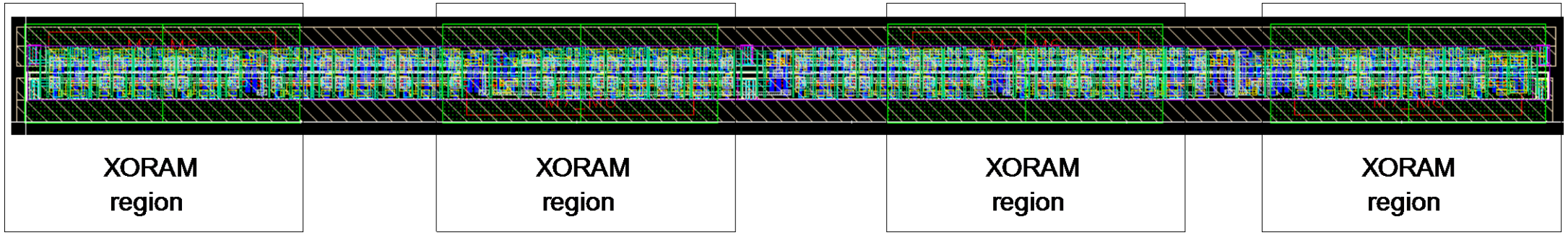
The 18-bit word line blocks have been piled up to compose and array of **18 × 64 bits**

Buffers placed at the top of the array

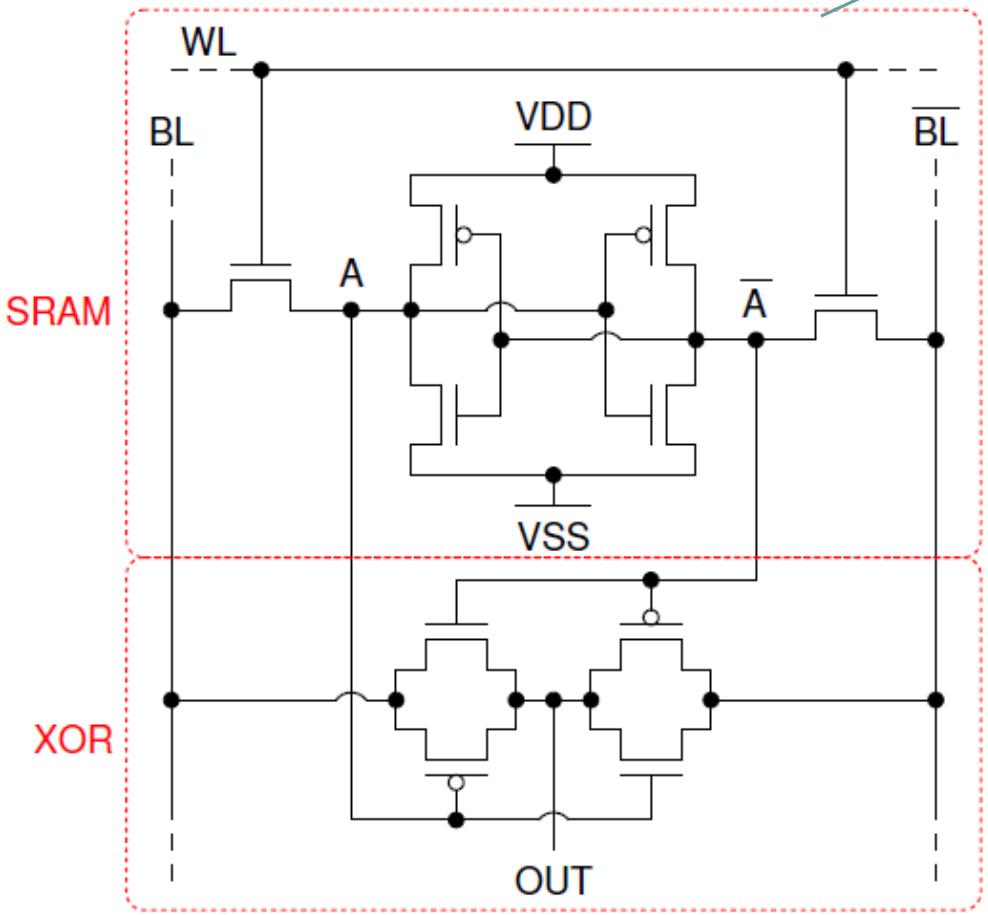
The **shift registers** is used to write and read the memory bank just for prototype characterization; in the new chip there will be different logic

Single cell area is 1.17 µm × 0.98 µm, and the block area is 6925 µm^2 : **factor 3** w.r.t. old cell designed at 65 nm



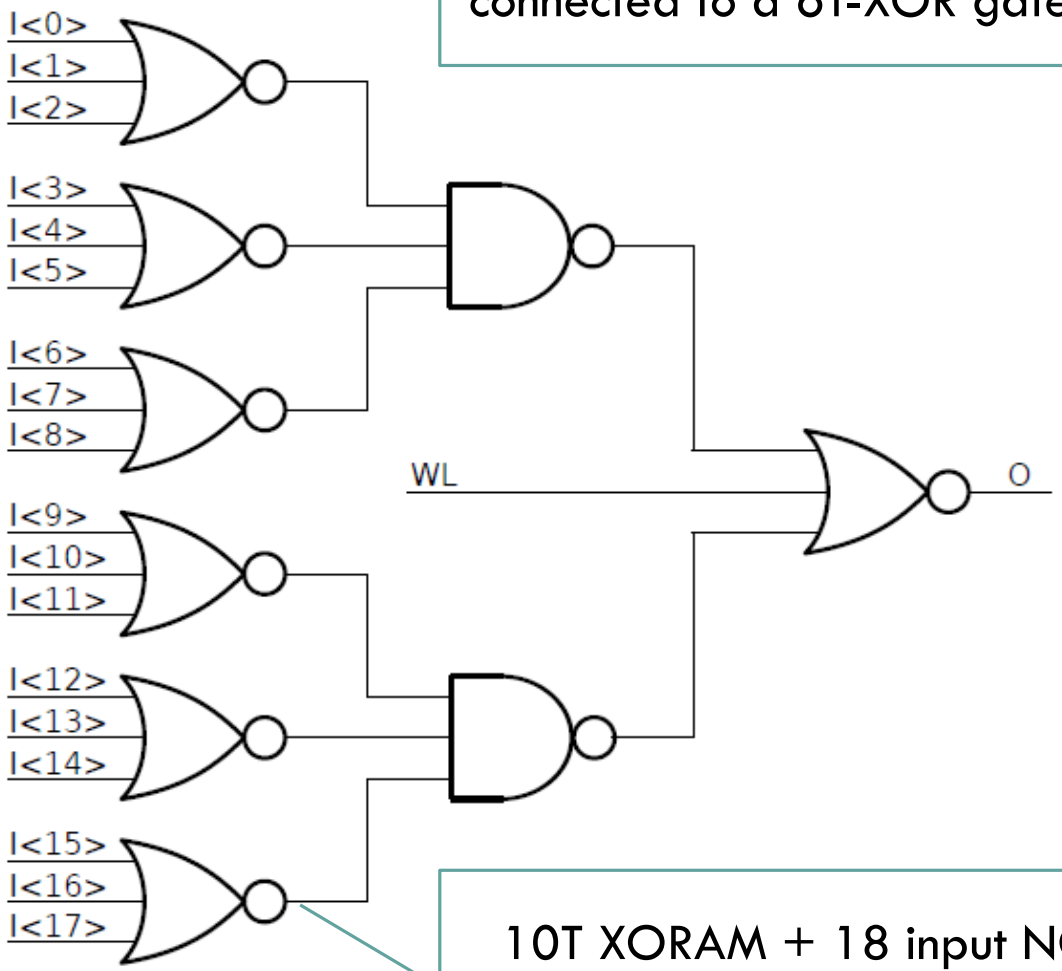


THE XORAM CELL



Based on XORAM CELL instead of NAND and NOR function.

Is made of a 6T SRAM cell connected to a 6T-XOR gate

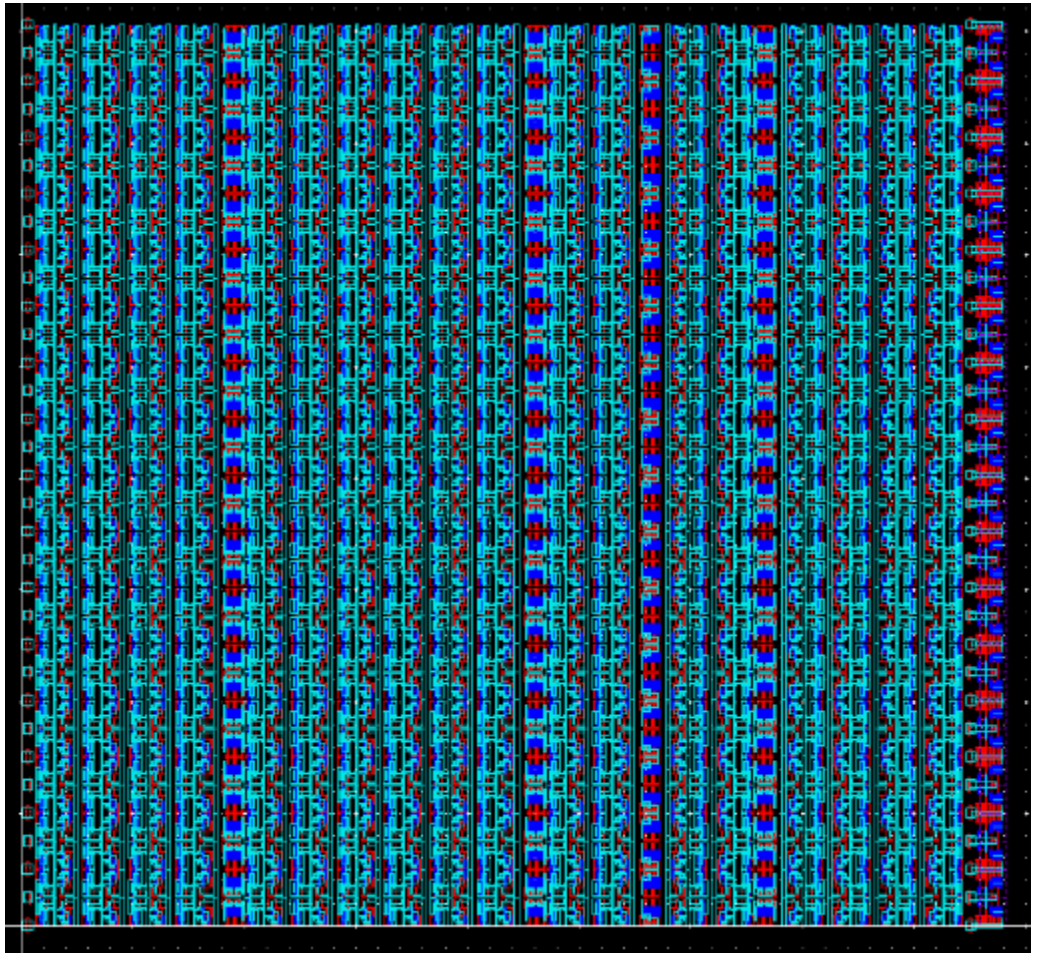


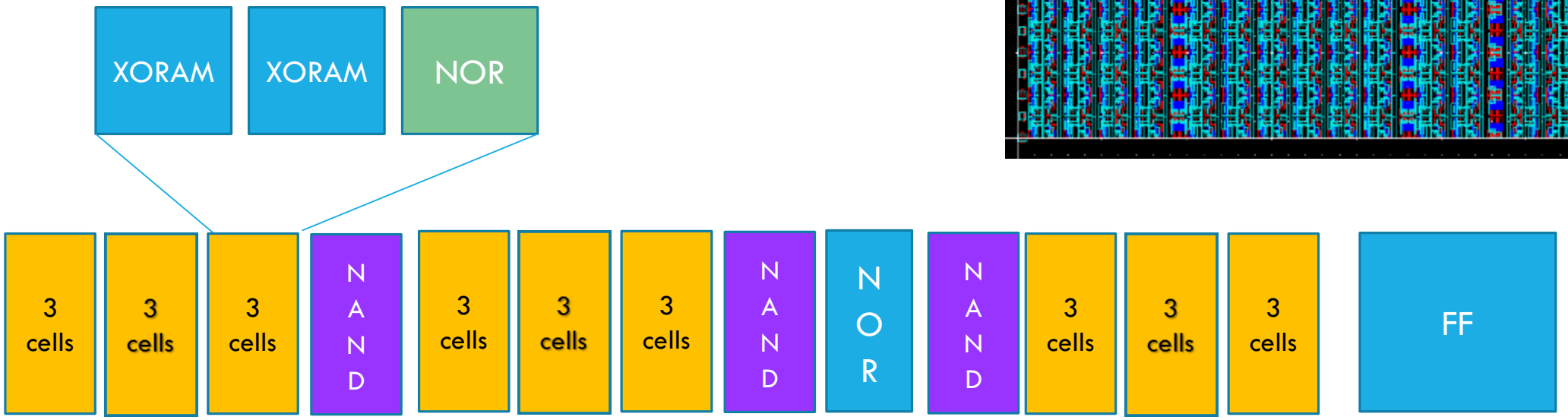
10T XORAM + 18 input NOR

BLOCK DESIGN

- Bit Lines propagation: top to bottom
- Write-lines propagation: left to right

- Flip-Flop at the end of each layer enabled by an EN signal
- Logic NOR tree integrated into the layer

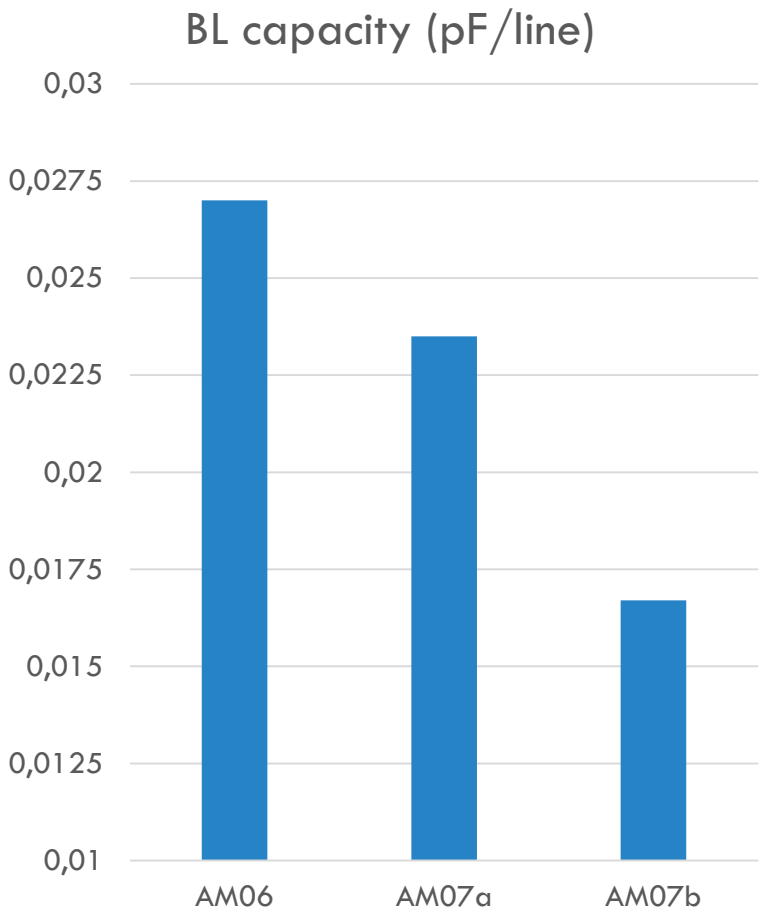


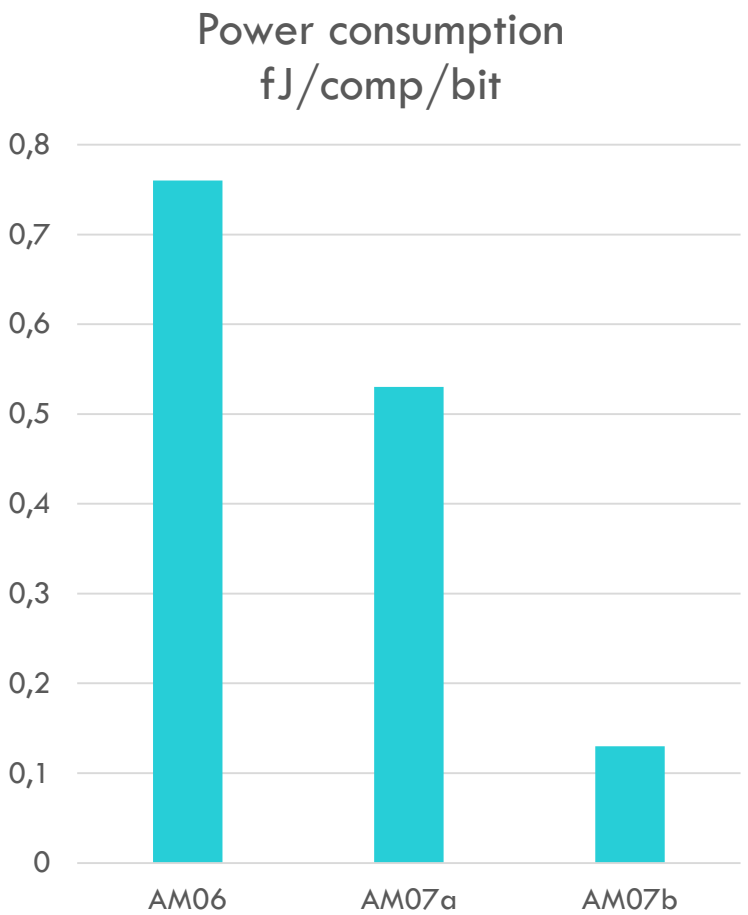


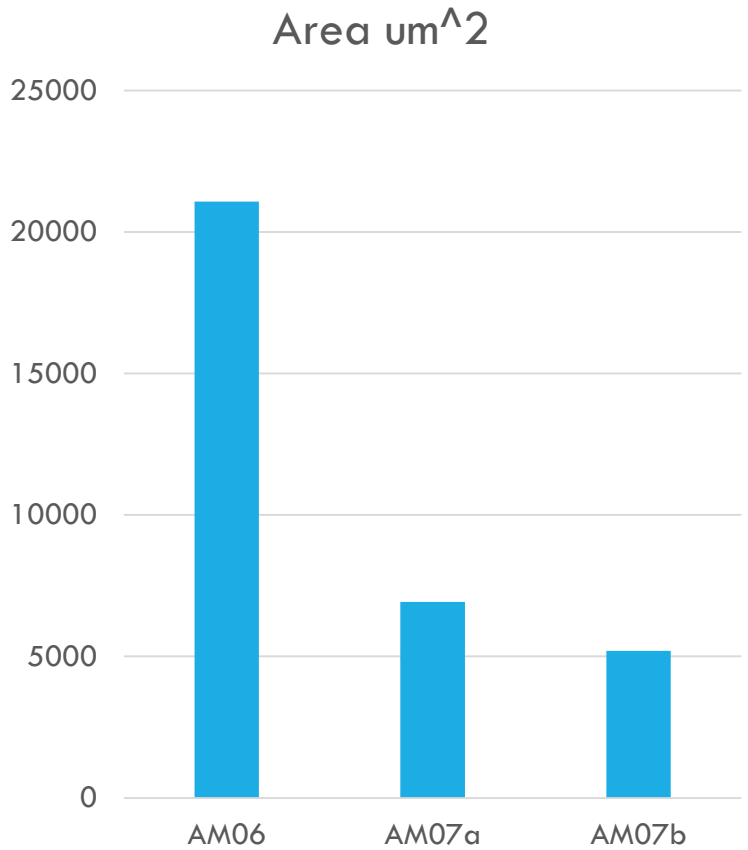
SOME STORY

Version	XORAM version	Technology	TOP2 size (um^2)	Consumption (fJ/comp/bit)	BL cap. (fF/line)
AM05a	v3	65nm	Selective Precharge		
AM06	v4	65nm	21075	0.76	0.027
AM07a	v5	28nm	6925	0.53	0.0235
AM07b	v6	28nm	5202	0.13	0.0167

DESIGN PROGRESS







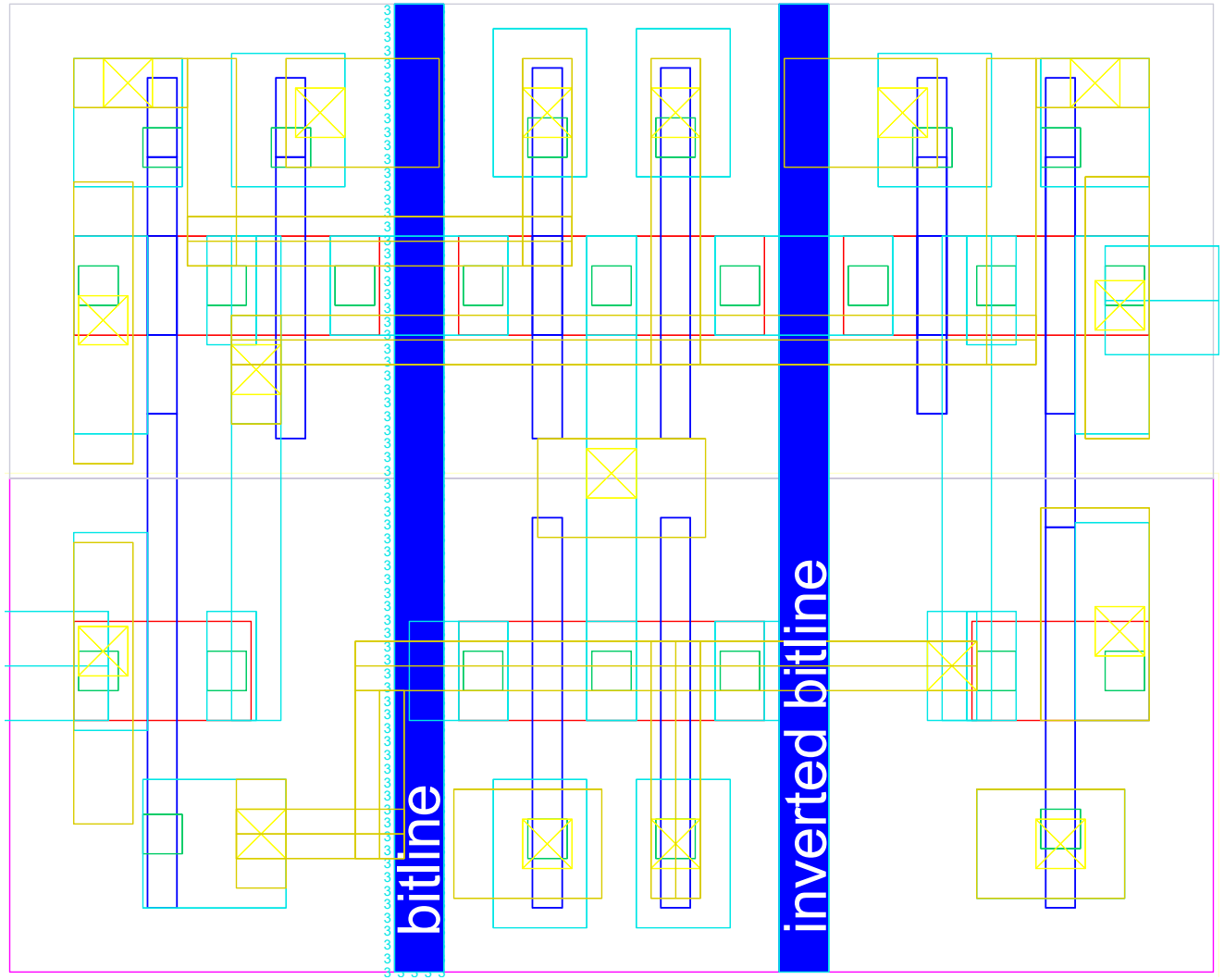
POWER SAVE METHODS

Minimization of parasitics

- 70% of dynamic power consumption is due to **propagation of bitline data**
- Block layout has been designed aiming at **minimizing bitline RC parasitic**
- Bitline wires have been designed in the **first metal layer (M1)**
- Bitline capacitance: 18 fF at CMOS 28 nm w.r.t 27 fF at CMOS 65 nm

Clockless circuit

- enable is given on the 18th bitline



OPTIMIZE BUFFER W/L AND # OF ROWS

Given 6 different worst cases:

- TT: 0.9 V, 27 °C
- SS: 0.81 V, 0 °C
- …

Given a fix $t_{prop}(BL, BL_{out})$=218ps $\psi = \frac{t_{prop}(BL,BL_{out})}{n}$; $n\,\epsilon\{16, 32, 64, 128, 256\}\ \psi = 218\,ps/64$

W/L should be change with the # of rows within the macro block.

Each macro block have Buffers on the top

We extract RC parasitcs for 5 different row blocks:

- 16,32,64,128,256

Find the optimum solution that minimize the power consumption for each 5 different row block, W/L and worst cases

SIMULATIONS

Tuning the W/L and the stades of BL and SL buffers

Parametric simulation by changing the W/L and the C(load)

Comparing the result with simulations:

If the minum point of the table is the same we demonstrate a strong correlation between the C(load) and the power consumption

CONCLUSIONS

DONE:

- ✓Design of 28nm XORAM cell
- ✓Optimization of BL capacitance
- ✓Power consumption minimization
- ✓Area reduction

TO DO:

- ➢BL buffer design
- ➢Cell characterization