



**Istituto Nazionale di Fisica Nucleare**  
*Sezione di Perugia*

Tel. 075/5852741

E-mail: Bruno.checcucci@pg.infn.it

*Responsabile del servizio elettronico unico  
INFN e Dip. di Fisica & Geologia  
Università degli Studi di Perugia*

SPECIFICATIONS FOR:

**PCB for a CORRECTED version of PRM (Pattern Recognition Mezzanine) for AM06 chips  
(ATLAS & CMS experiments)**

**List of changes respect PRM used AM05 chips:**

1) AM Chips

**Old scenario:** 4 banks of 4AM05 Chips

**New scenario:** 12 chips.

Proposal of 2 banks of 4AM06 Chips & 2 banks of 2 AM06.

2) Clk logic for the FPGA of the PRM:

125Mhz generation

**Old scenario:** Crystal at 25Mhz (8Y-25.000MAAJ-T) plus multiplier x5 (ICS844021I Clock Generator)

**New scenario:** Crystal (XTAL CS023 114.285) + Si5328 for gtx clock / Si570 for system clock

3) Memory:

**Old scenario:** One bank of memory (DDRII)

**New scenario:**

1 RLDRAM3 part n.MT44k32M36RB107E ITA

1 flash RAM ?? it's not clear yet if there will be enough space

4) FPGA:

**Old scenario:** 1 chip XC7K355T

**New scenario:** 1 chip XCKU060 FFVA1156 35x35mm2 -1L o

-1 @0.95V

5) Dc Power strategy :

**Old scenario**: n°3 DC/DC 20A@1V - n°1 DC/DC 12A@2.5V - n°3 DC/DC 12A@1.2 V / n°1 DC/DC 3A@1.8V.

**New scenario**: FPGA (n°1 DC/DC 20A@0.95V n°1 DC/DC 5A@1V - n°1 DC/DC 3A@1.2 V - n°1 DC/DC 1A@1.8 V) AM(n°2 DC/DC 20A@1V -n°1 DC/DC 5A@1.2V) - n°1 DC/DC 6A@2.5V - n°1 DC/DC 3A@1.8V

6) AM chip foot print

**Old scenario**: see foot print added

**New scenario**: see foot print added

7) LEDs for the Vrails

3.3V

2.5V

1.8V

1.35V (Memory)

1.2V

1V

8) Mechanical connection between Pulsar and PRM card.  
2 FMC HPC connectors screws for fixing will be foreseen.

9) Temperature probes:

Will be used the ones foreseen inside the FPGA

10) Will be included fuses (n.6) at the Vrails inputs.

11) DtestOut pin (AM chip) Test points will be foreseen on the board.

ITEMS REQUESTED TO THE COMPANY WHICH  
RECEIVE: ELECTRICAL SCHEME (Altium release 14.0),  
NETLIST AND BOM.

- 1) PROTOTYPE BOARDS TO BE PRODUCED:  
N.....(N.....assembled);
- 2) LAYOUT DEFINITIONS;
- 3) ENGINEERING STUDY OF THE BOARD STARTING FROM THE  
PREVIOUS GERBER FILES;
- 4) PARTS PROCUREMENT(partially, do not consider AM chips and FPGA);
- 5) PCBs TEST;
- 6) PCBs ASSEMBLY;
- 7) PCBs DELIVERY.

Legenda:

**Old scenario**: means PRM05

**New scenario**: means PRM06

*Perugia 30/11/2015*