Triggerless readout for silicon detectors at PANDA

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Summary

PANDA is a key experiment of the future FAIR facility, under construction in Darmstadt, Germany. It will study the collisions between an antiproton beam with momenta between 1.5 GeV/c and 15 GeV/c and a fixed proton or nuclear target, allowing to study QCD at intermediate energies.

The data acquisition concept of PANDA foresees a fully triggerless readout system and, together with the upgrade of LHCb, represents one of the first applications of a software-only triggering concept in a particle physics experiment. The triggerless architecture allows for the application of different filters on the same data sample, thus enabling the study of parallel physics topologies. The nominal collision rate, up to 20 MHz, poses significant challenges both on the detector readout electronics and on the data acquisition infrastructure.

The Micro Vertex Detector (MVD) is the innermost part of the tracking system of the experiment and its main task is the precise spatial identification of primary and secondary vertices.

The detector will be composed of four concentric barrels and six forward disks; the inner layers will be instrumented with silicon hybrid pixel detectors, while for the outer two barrels and for the outer part of the last two disks double-sided silicon microstrip detectors were chosen.

Precise timestamp, signal amplitude capabilities, as well as low power consumption, a high dynamic range and radiation tolerance for both total ionising dose and single event effects, are common requests to the readout system of both parts.

The readout of the pixel part uses the ToPix chip, which is a custom development in a 0.13 um commercial CMOS technology.
It will consist of a 116×110 pixel matrix arranged in 55 double columns and a Chip Control Unit (CCU) which multiplexes the data from the column controllers and sends them to the off-detector electronics via two 320 Mb/s serial links.
In the pixel cell, the feedback capacitor of a preamplifier is discharged by a constant current. The preamplifier is followed by a comparator; a digital control unit detects the rising and falling edges of the comparator output and stores the respective timestamps.
Due to the constant discharge of the integrating capacitor, the length of the comparator output is a linear measure of the integrated charge and therefore the difference between the trailing and leading edge timestamps provides a measure of the charge released by the particle in the detector; this approach is known as Time-over-Threshold (ToT).
Four prototypes have been realized; the latest features 640 full pixel cells divided into 8 columns. The functionality and the radiation hardness of the prototypes have been extensively tested, both in the laboratory and during beam tests.

For the readout of the strip sensors of the MVD, the PASTA (PAnda STrip ASIC) chip has been developed. Its architecture is also based on the Time-over-Threshold technique and is inherited from TOFPET [1], a chip developed in the framework of the EndoTOFPET-US collaboration for the readout of Silicon Photomultipliers signals for a medical PET application.
The analog frontend of PASTA consists of a preamplifier which can be connected to both n-type and p-type strips, and a second stage where a constant current discharges a feedback capacitance to extract a linear ToT information.
The leading and trailing edges of the ToT signal are measured with time-to-digital converters with linear analog interpolators, providing a time resolution adjustable between 50 and 500 ps.
The chip is designed to work with a clock of 160 MHz, with a maximum power consumption of 4 mW per channel.
A 64 channel chip prototype has been submitted in a commercial 110 nm CMOS technology; the final prototype size is 3.4 x 4.5 mm2. The evaluation of the prototype is currently ongoing.

An overview of these systems and of their relevance to the triggerless acquisition at PANDA will be presented.

[1] M.D. Rolo et al.
TOFPET ASIC for PET Applications, 2013 JINST 8 C02050

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