# Triggerless readout for silicon detectors at PANDA

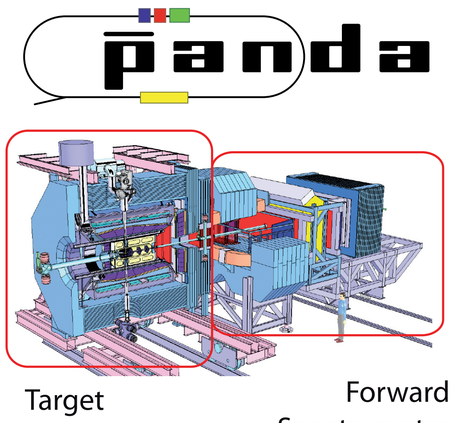
Tommaso Quagli[1, 2] on behalf of MVD Group - INFN, Sezione di Torino

[1]II. Physikalisches Institut, Justus-Liebig-Universität Gießen; [2]INFN, Sezione di Torino

Terzo Incontro Nazionale di Fisica Nucleare INFN2016, LNF, Frascati

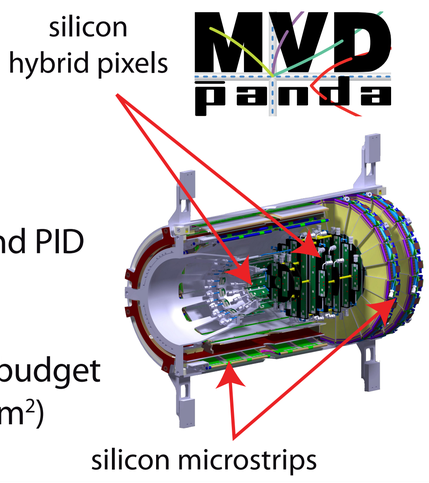
## The PANDA Experiment

- Fixed target experiment
- Almost 4π acceptance
- Cooled antiproton beam using electron and stochastic cooling
- Proton or heavy nuclear target
- Momentum from 1.5 up to 15 GeV/c
- Trigger-less readout at ~$10^7$ interactions / s



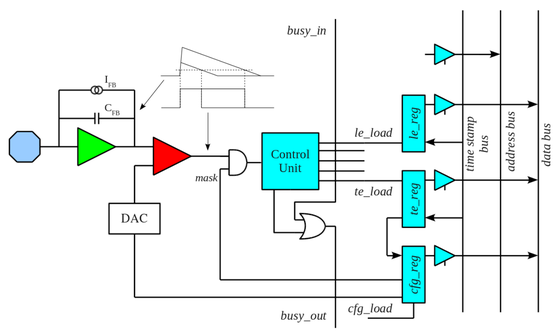

## The Micro-Vertex-Detector

- 4 concentric barrels and 6 forward disks
- Vertex reconstruction for primary and secondary vertices
- Improvement of momentum resolution and PID
- Requirements:
  - spatial resolution (tens of μm)
  - good time resolution and low material budget
  - high radiation tolerance ($10^{14}$ $n_{1MeV\,eq}$ / $cm^2$)

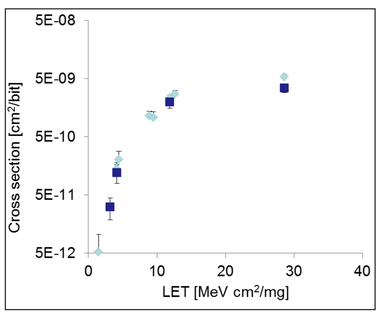



## Hybrid Pixel Detector Readout: ToPix

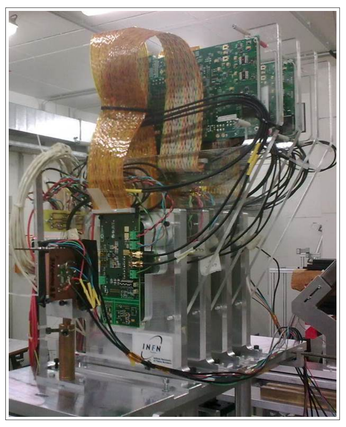
- Detector modules based on epitaxial pixel sensors and ToPix readout chip
- Main features of ToPix:
  - pixel size: 100 x 100 μm²
  - chip active area: 11.4 x 11.6 mm² (116 rows, 110 columns)
  - dE/dx measurement: ToT, 12 bits dynamic range
  - Max. input charge: 50 fC
  - Noise floor: < 200 $e^-$
  - Input clock frequency: 160 MHz
  - Time resolution: 6.43 ns (1.86 ns r.m.s.)
  - Power consumption: < 800 mW / cm²
  - Max. event rate: 6.1· $10^6$ / s
  - Total Ionizing Dose: < 100 kGy




Schematic of the pixel cell



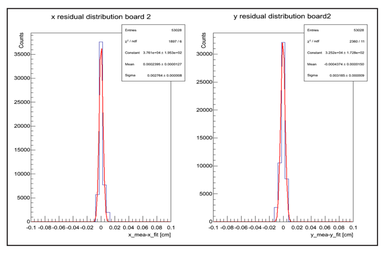

SEU tests of ToPix_v4 with ion beams @ LNL-INFN. Study of the configuration registers inside the pixels. SEU cross section one order of magnitude lower with respect to ToPix_v3 (D-type flip-flops circuits with TMR instead of latches with TMR)



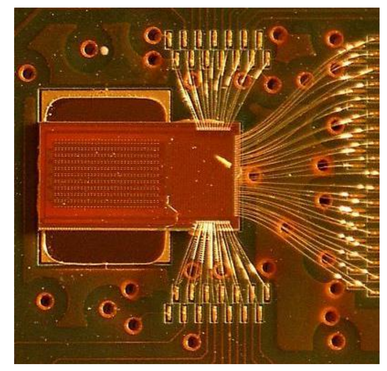
4 single-chip assemblies under test at FZJ with 2.9 GeV/c proton beam

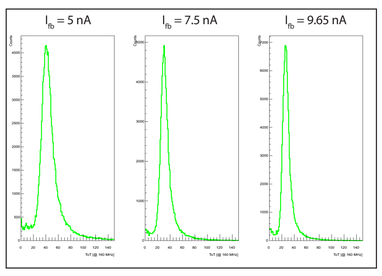
## ToPix_v4 prototype

- ASIC size: 3 x 6 mm², clock frequency 160 MHz
- 130 nm CMOS technology
- Pixel matrix: 640 cells, 2x2x128 and 2x2x32 columns
- Time over Threshold technique, 12 bits dynamic range
- Compatible with sensors of previous version (ToPix_v3)
- Hamming encoding and TMR pixel logic protection
- Leading and trailing edge registers with DICE-protected latches
- SEU protected EoC
- Serial data output (SDR and DDR)
- GBT compatible SLVS I/O

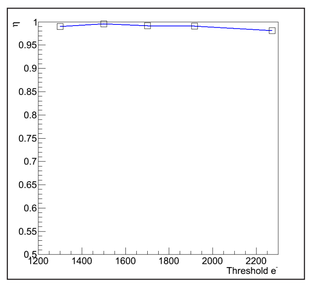



Residual distributions






ToT at several discharge currents of the feedback capacitor

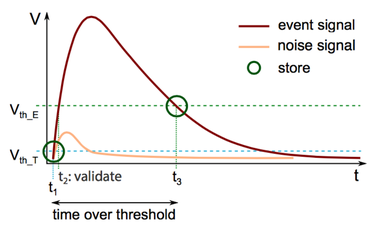



Efficiency vs. threshold

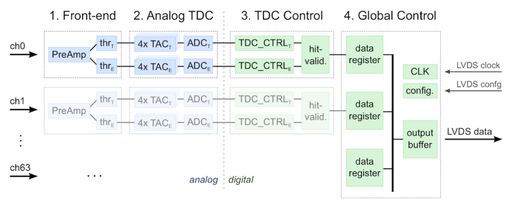
## Double-sided Silicon Strip Detector Readout: PASTA

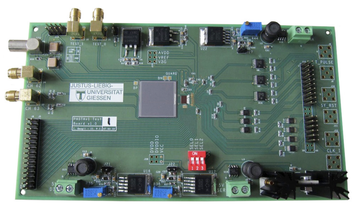
- Barrels: rectangular and square strip sensors
- Disks: trapezoidal strip sensors
- Front-end readout chip: PASTA (PANDA STrip ASIC)
- Chip concept inspired by TOFPET
- Main features of PASTA:
  - channels: 64
  - input pitch: 63 μm
  - clock frequency: 160 MHz
  - rate capability: 100 kHz / ch
  - time bin width: 50 - 400 ps
  - dE/dx measurement: ToT, 8 bits dynamic range
  - Front-end noise: < 600 $e^-$
  - Power consumption: < 4 mW / ch
  - Radiation tolerance: 100 kGy (TID)
  - Technology: CMOS 110 nm

### Measurement Concept



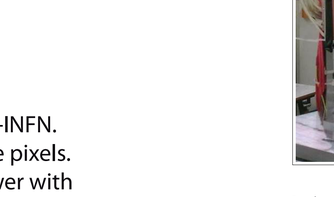

### Chip Architecture



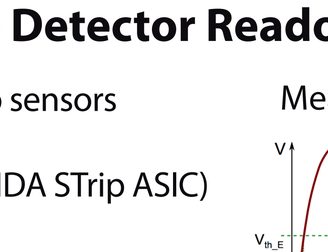



PASTA on the DISH (Digital Interface for Strip data Handling) test board with a strip sensor

### Chip Simulations

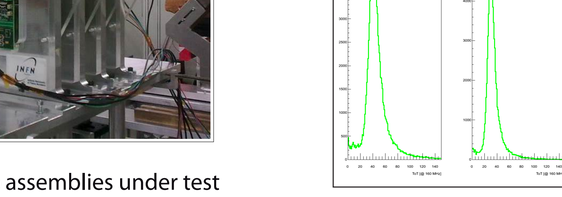


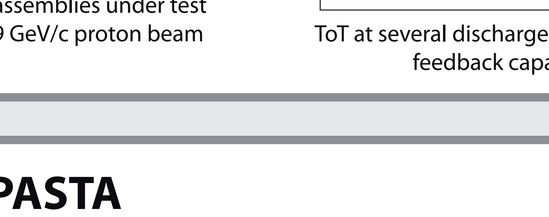

ToT linearity in the input charge range from 1 fC to 40 fC with a capacitance of 25 pF




Electronic noise with an input charge of 4 fC, for a capacitance from 1 pF to 30 pF

### Analog TDC




Analog TDC architecture and working principle

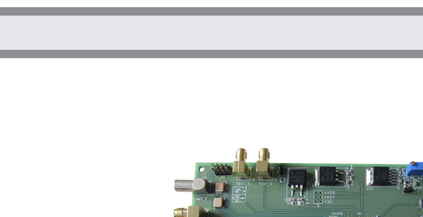
$C_{TDC} = 4 \cdot C_{TAC}$ ; $I_{TDC} = 1/32\ I_{TAC}$

$V_{TDC} = V_{TAC} \rightarrow t_{TDC} = 128 \cdot t_{TAC}$

### First test results




Example of chip test signals for an injected pulse




ToT linearity with ToT = $t_{coarse\_E}$ - $t_{coarse\_T}$


Electronic noise with an input charge of 4 fC, for a capacitance from 1 pF to 30 pF

JUSTUS-LIEBIG-UNIVERSITÄT GIESSEN
JÜLICH FORSCHUNGSZENTRUM
INFN
GEFÖRDERT VOM Bundesministerium für Bildung und Forschung
HIC for FAIR Helmholtz International Center

Tommaso Quagli
II. Physikalisches Institut, JLU
Heinrich-Buff-Ring 16
D-35392 Gießen
Tommaso.Quagli@exp2.physik.uni-giessen.de