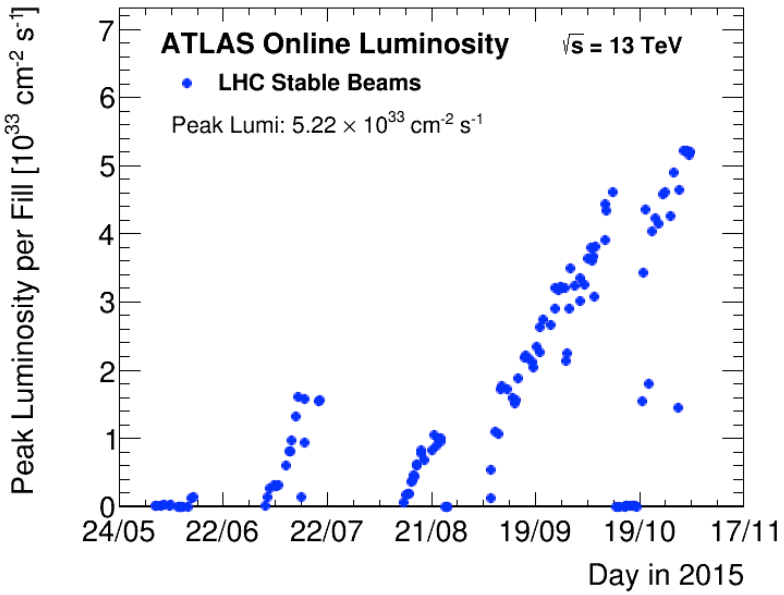
Status della attività ATLAS TDAQ a Napoli

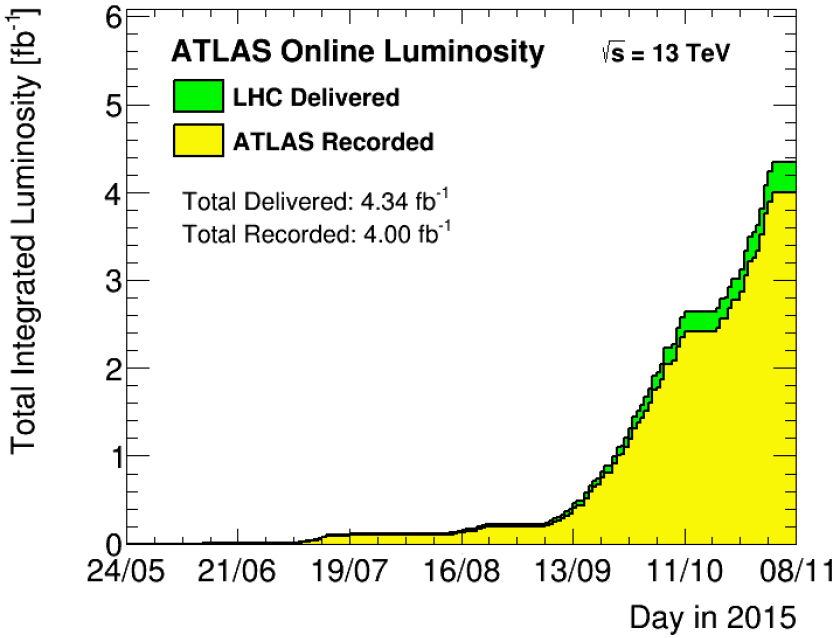
Run 2 operations &
Phase1 perspectives

Vincenzo Izzo

Run 2 Operations

Run 2 Operations





- L_{int}: 4.00 fb^{-1}, L_{peak}=5.22x10^{33}cm^{-2}s^{-1}
- μ ≅ 20 for 50ns, μ ≅ 17 for 25ns

- Data taking efficiency: ~92%
- In **25 ns**, the inst. L increased by a factor of ~4 wrt 50 ns

- Technical stop 3 ongoing this week
- ion run starting next week
- winter shutdown starting 14th December

- new TDAQ release being finalized
- only 64 bit (32bit not supported anymore)
- still CMT based, gcc 4.9, ROOT 6.04

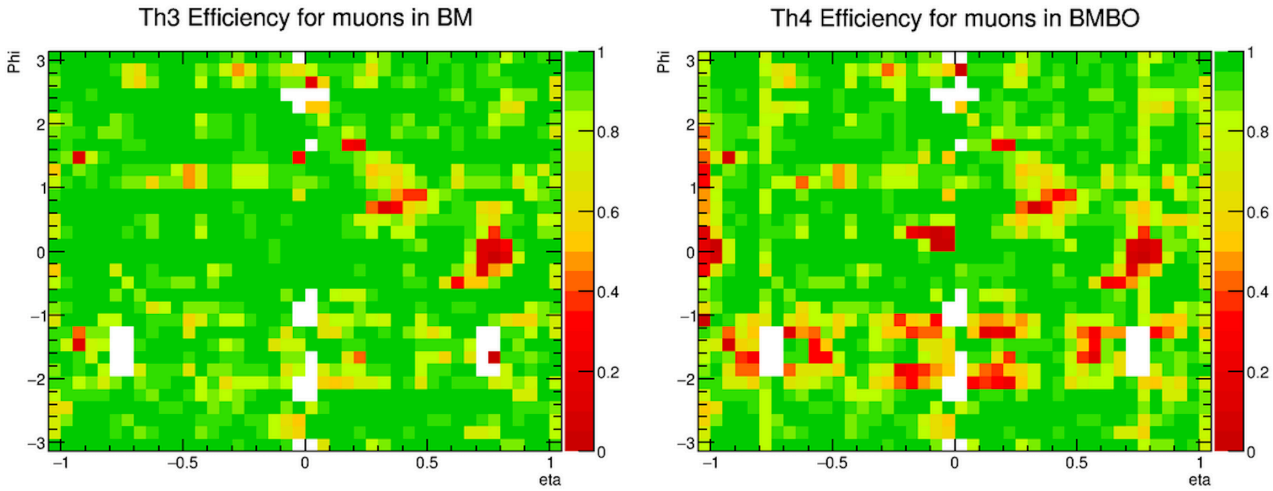
L1 Operation

*INFN BO, LE, NA, Roma1, Roma2, Roma3

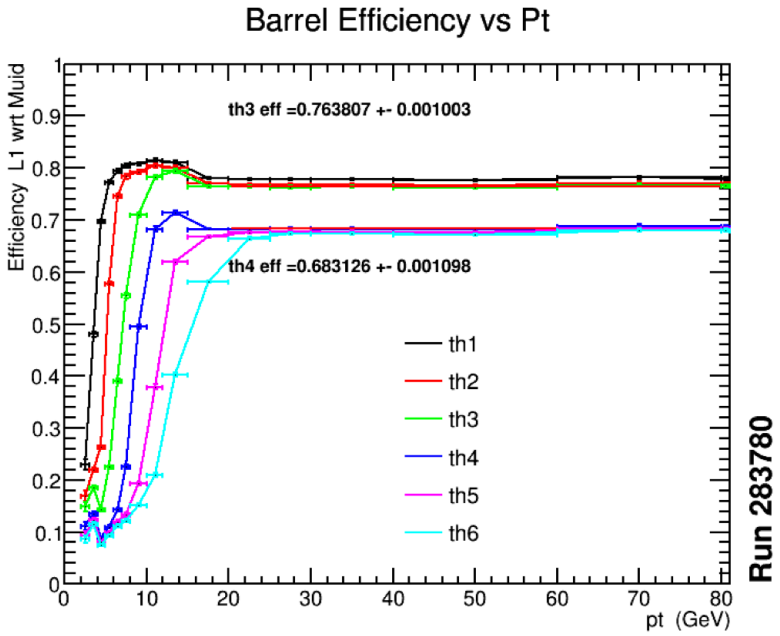
- RPCs show at least 7 localized inefficiency regions in 2015 wrt 2012
- Experts working to understand the reason of inefficiencies
- Working on MC realistic simulation

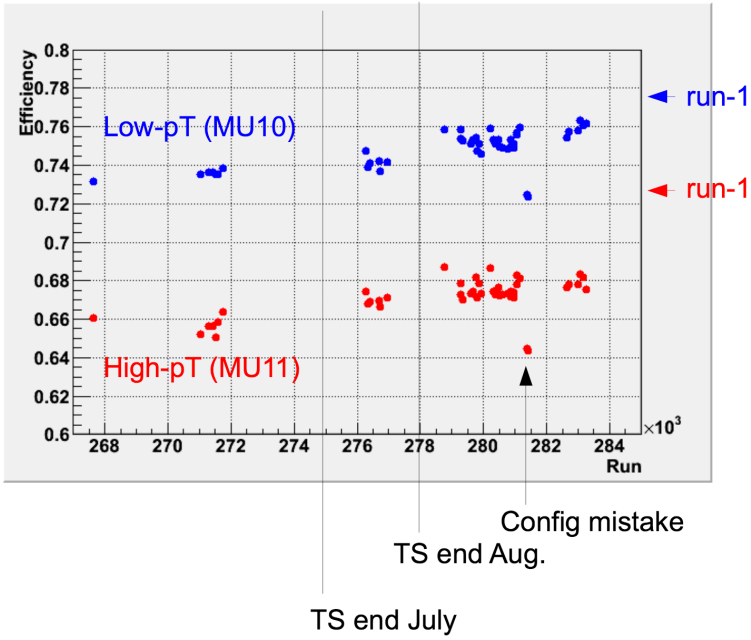
	Low p_T	High p_T
MC12	76%	71%
MC15	85%	81%
data12	78%	72%
data15*	72%	64%

* 50 ns data



Eta-phi efficiency maps: muons going through RPC1+2 & RPC1+2+3





Muon Barrel L1 trigger (NA)

- schede ROD e link ottici per la lettura dei dati di trigger
- DAQ RPC
- **L1 Muon Trigger Operation:** F. Conventi, M. Della Pietra, V. Izzo, S. Perrella, E. Rossi, V. Bruscino (da Informatica)
- **monitoring online per Data Quality:** resp. M. Della Pietra
- **maintenance trigger e DAQ:** M. Della Pietra, V. Izzo, S. Perrella

  aggiornamento software per il trigger dei **muoni** di I liv.
- **inclusione nel TDAQ degli RPC 'dei piedi' del magnete e 'degli ascensori':** M. Della Pietra, V. Izzo, S. Perrella

PHASE 1

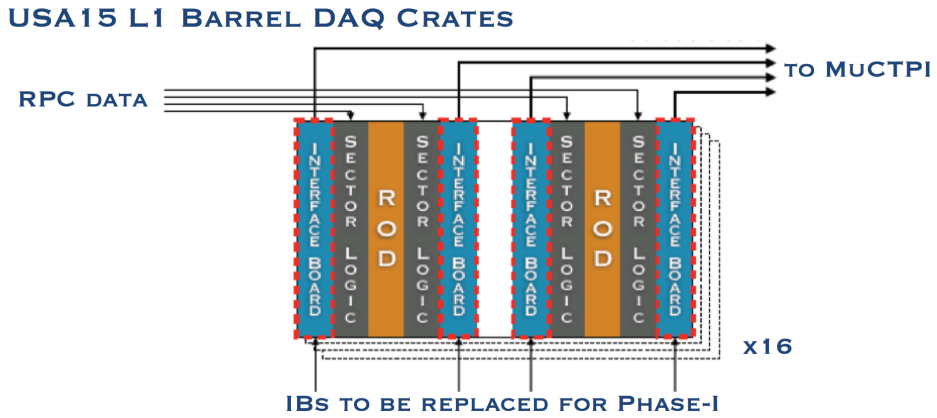
- **sviluppo, realizzazione e test delle schede MuCTPI Interfaces**, per trasferire i dati di trigger delle SL, su fibra ottica, da USA15 verso il CTP: M. Della Pietra, R. Giordano, V. Izzo, S. Perrella

(in verde le attività 2015/2016)

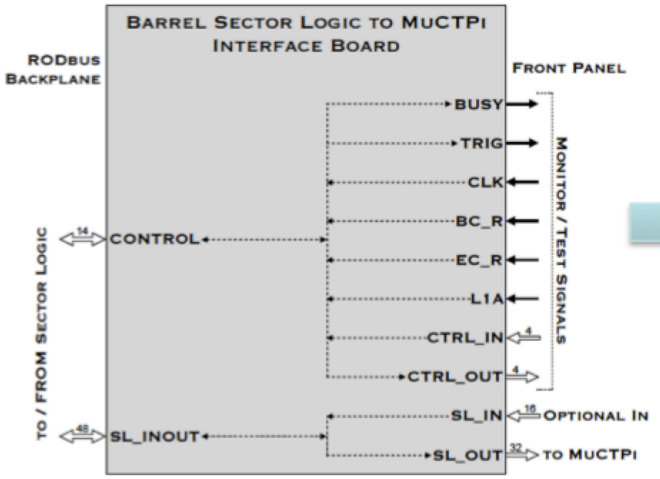
Phase 1

New MuCTPI Interface Board

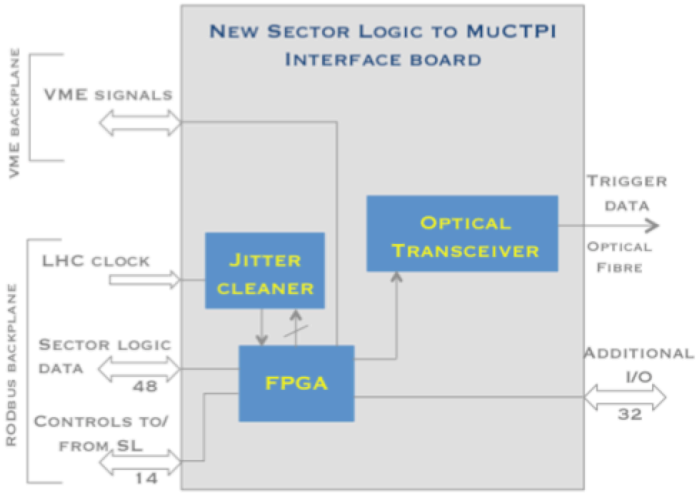
*INFN Napoli, Roma1, Roma2



Attuale IB

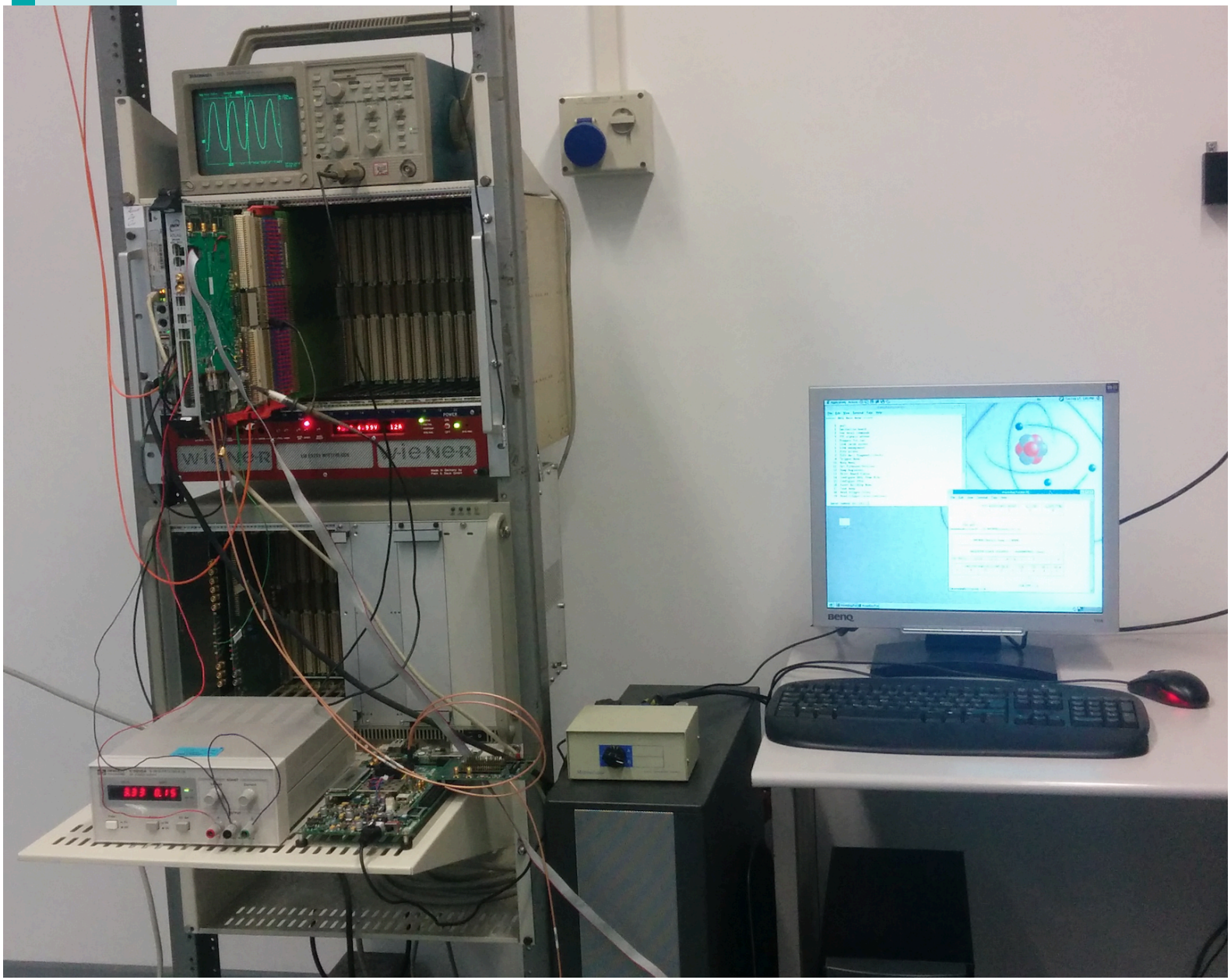


Futura IB



- New Interface board equipped with a last-generation FPGA, allowing VME communication and serialization to MuCTPI via optical fibre
- Optical SFP+ transceiver, Data Rate: 6.4 Gb/s : 128 bit @ 40 MHz or 64bit @ 80MHz
- Serialization logic synchronous with 40 MHz LHC clock

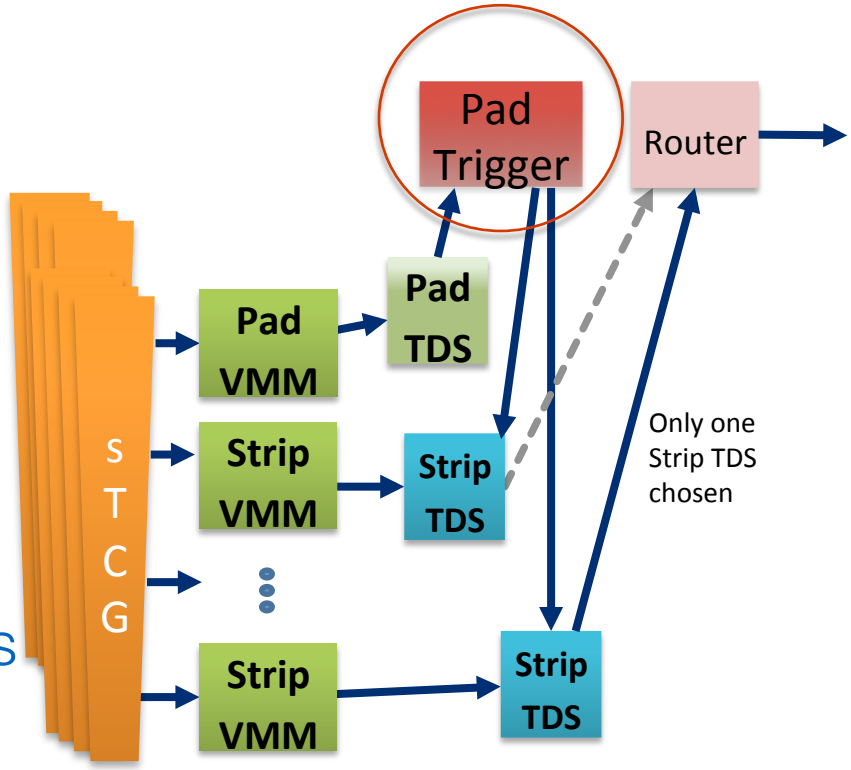
Tests Preliminari



NSW sTGC PAD Trigger Board

*INFN Napoli, Roma1

- The PAD Trigger board is used to select the NSW regions having a hit, thus reducing the amount of data to be transferred Off-detector
- Find a Pad hit coincidence in a tower of logical Pads within one Bunch Crossing.
- 3/4 majority logic is required on both sTGC quadruplet.
- Candidate geometrical coordinates and BCID sent to the front-end strip-TDS chips.
- Strip-TDS sends only selected strip data to the routers.

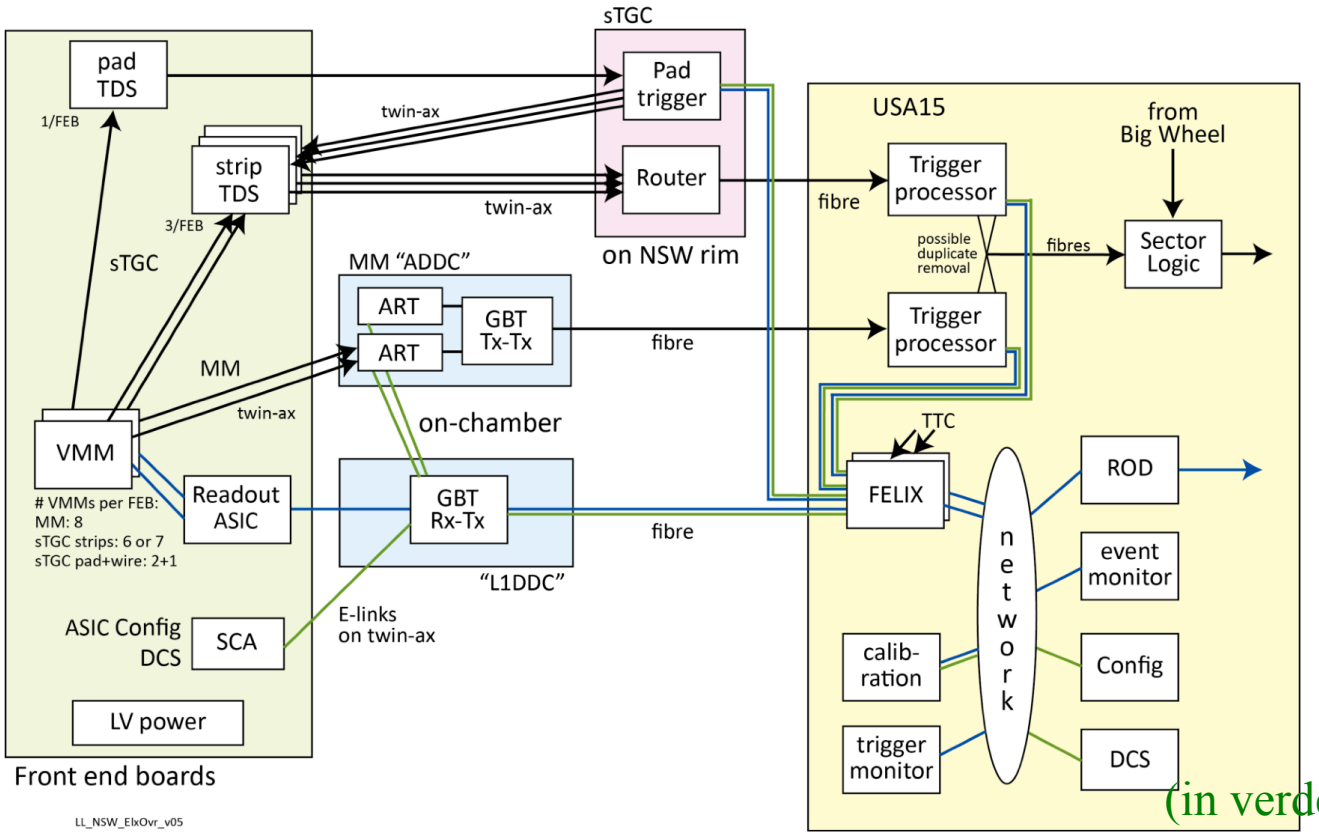


On-Detector NSW sTGC electronics

Attività Trigger NSW

- **Sviluppo hardware e firmware per scheda PAD Trigger, per rivelatori sTGC** (V. Izzo, S. Perrella, R. Giordano)

- Sviluppo di un link seriale ad alta velocità su FPGA per DAQ MM e trigger per le NSW (V. Izzo, S. Perrella, R. Giordano)

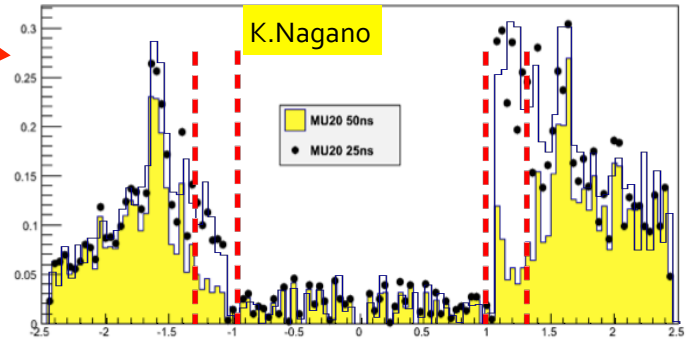


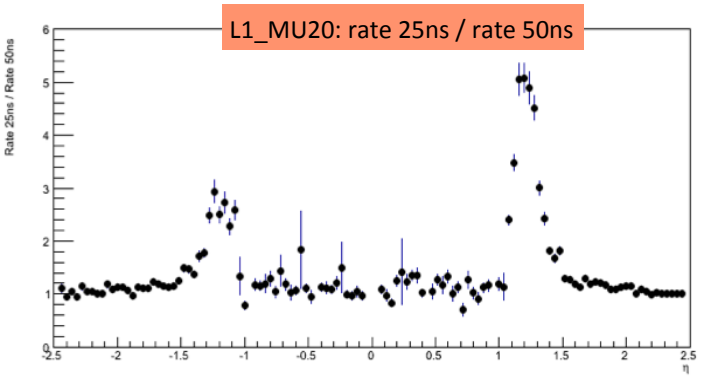
(in verde le attività 2015/2016)

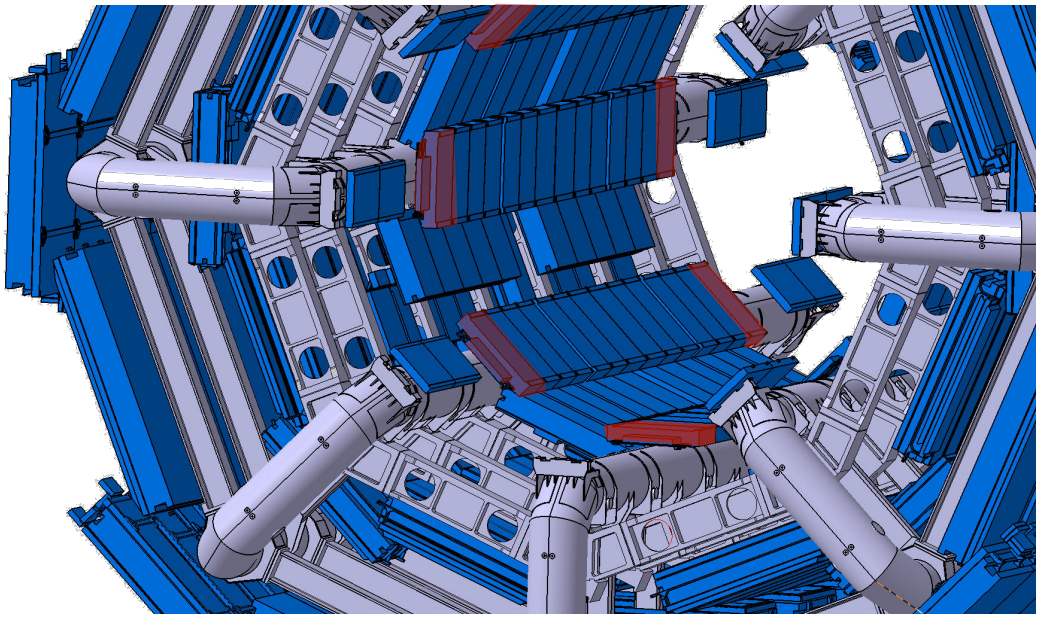
The BIS78 project

*INFN Napoli, Roma1

- The Barrel/EndCap transition region ($1 < \eta < 1.3$), not covered by the NSW, will suffer from high trigger fake rate with increasing luminosity.
- The additional RPC chambers in the Barrel Inner Small region (16 new stations) can significantly reduce the foreseen fake rate.
- 16 Pads will receive RPC time hit data and produce the muon trigger candidate to be sent to the End-Cap Sector Logic boards in USA15.
- Extrapolated occupancy for high luminosity pile-up shows less than 1 candidate per BC per Pad.







Phase-1 Pad Board

- On-detector board, receives data from sTGC (or RPC) front-end ASICs.
- 16 NSW boards per side (8 for the BIS78), 32 (16) Pads in total.
- Performs a 3/4 (2/3) majority logic and sends the trigger candidate to the End-Cap Sector Logic through an optical fibre.
- Performs also the sTGC Pads (RPC) readout logic. Readout data and TTC signals are sent/received through the GBT/Felix system.
- Tight latency requests for sTGC PAD, no tight requests for BIS78.
- The Pad optical output has to be fan-out in USA15 to be connected to up to 4 End-Cap Sector Logic boards (to match the different phi segmentation).
- System is compatible with Phase-2.

(in verde le specifiche per BIS78)

Phase1 Timeline & Costs

NSW Pad:
2014.Q4: demonstrator board (to be used in test beams)
2015.Q1: Preliminary Design Review.
2015.Q4 - 2016.Q3: 1st & 2nd Pad board prototype
2016.Q2: Final Design Review.
2017.Q2: Production Readiness Review.
2017.Q2: production of the 32 Pad boards + 4/5 spares.
2017.Q3: installation and commissioning

Fundings:
94 kCHF + contingency (in 200 kCHF NSW contingency)
5 k€ for prototypes (2016) sub-judice (to MM module-0)

BIS78:
2015.Q3: PDR
Other milestones to be defined

Costs:
about 50 kCHF by USTC

SL_to_MuCTPi board upgrade:
2014.12: evaluation board
2015.02: PDR
2016.Q1: prototype1
2016.Q2: FDR
2016.Q4: prototype2
2017.Q1: PRR
2017.Q2: production

Fundings:
37 kCHF + contingency (6 kCHF)
Tot. foreseen = 64 kCHF, shared with Dutch institutes
6 k€ for prototypes (2016)

Spending Profile for the three projects: 2017

Attività prevista

- **Acquisto scheda di valutazione KC705 (finanziata per 2015, via BO) OK**
- **Progettazione PCB MuCTPI Interface Board presso S.E.R. (Q4 2015) OK**
- **Realizzazione PCB per prototipi MuCTPI Interface Board (ordine completato nel 2015, con PCB da sottomettere a gen-feb 2016)**
- **Progettazione, Implementazione, Simulazione e Test del Firmware preliminare per prototipi MuCTPI Interface Board (2016)**
- **Ripristino stazione di Test e collaudo dei links ottici, presso il S.E.R. OK**
- **Verifica e riparazione spares delle schede ROD, presso il S.E.R. (…)**

(in verde le attività 2015/2016)

Backup

Operation

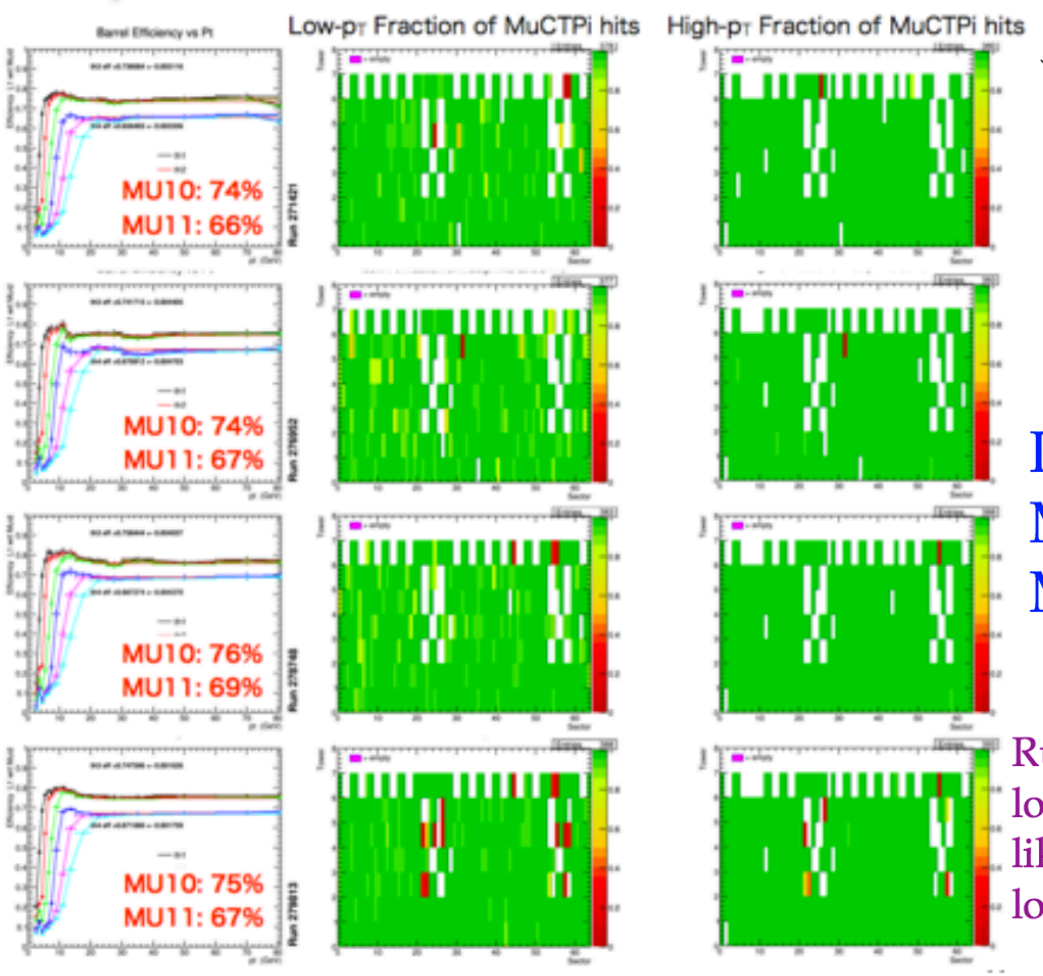
RPC-LV1 trend in run II

Run 271421
(12 Jul. 2015)
14 pads off, 9 missing input
(feet/elevators=36)

Run 276952
(23 Aug. 2015)
before TS

Run 278748
(7 Sep. 2015)
after TS
some HV gaps recovered

Run 279813
(19 Sep. 2015)
some feet pads in the run
but no timing calibration yet



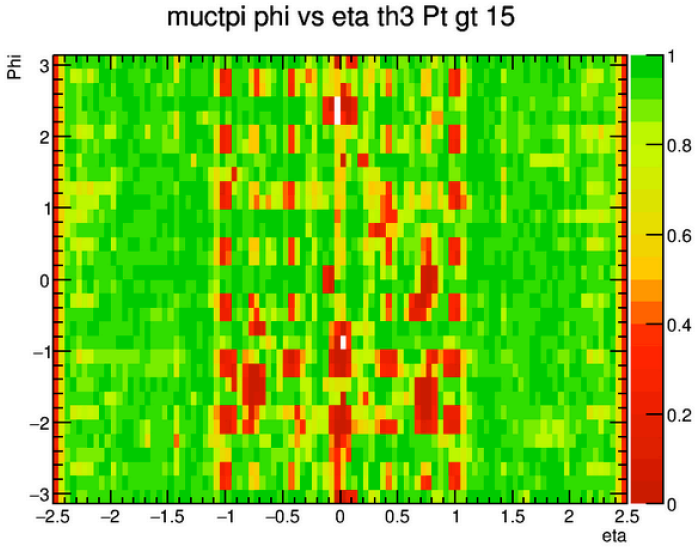
Riccardo Vari

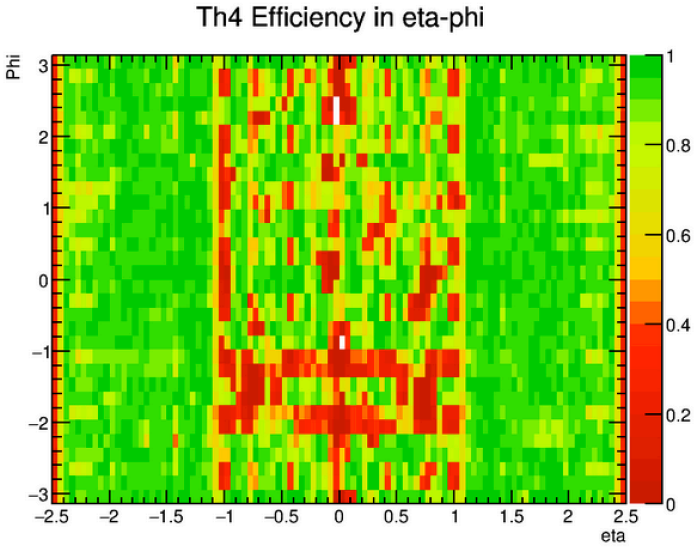
Run 1:
MU10 78%
MU11 72%

Run2 apparently lower efficiency likely due to localized defects

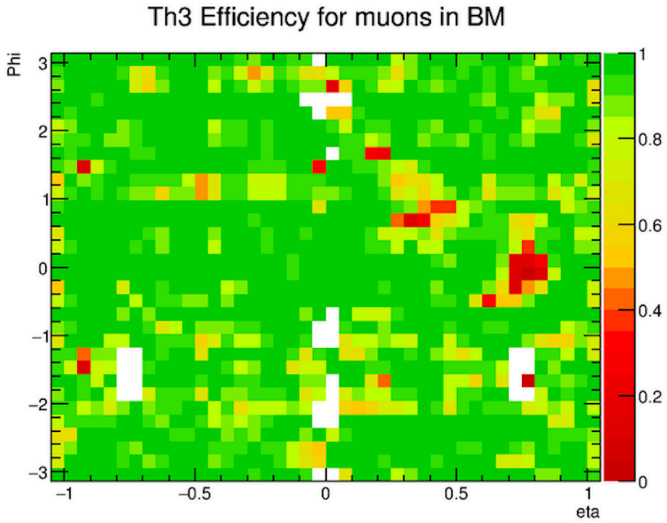
L1 Operation

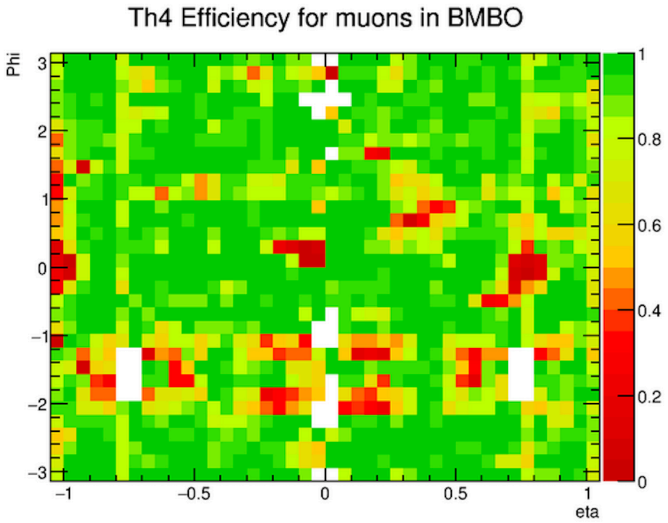
Eta-phi efficiency maps: barrel+endcap





Eta-phi efficiency maps: muons going through RPC1+2 & RPC1+2+3





Dataflow Operations

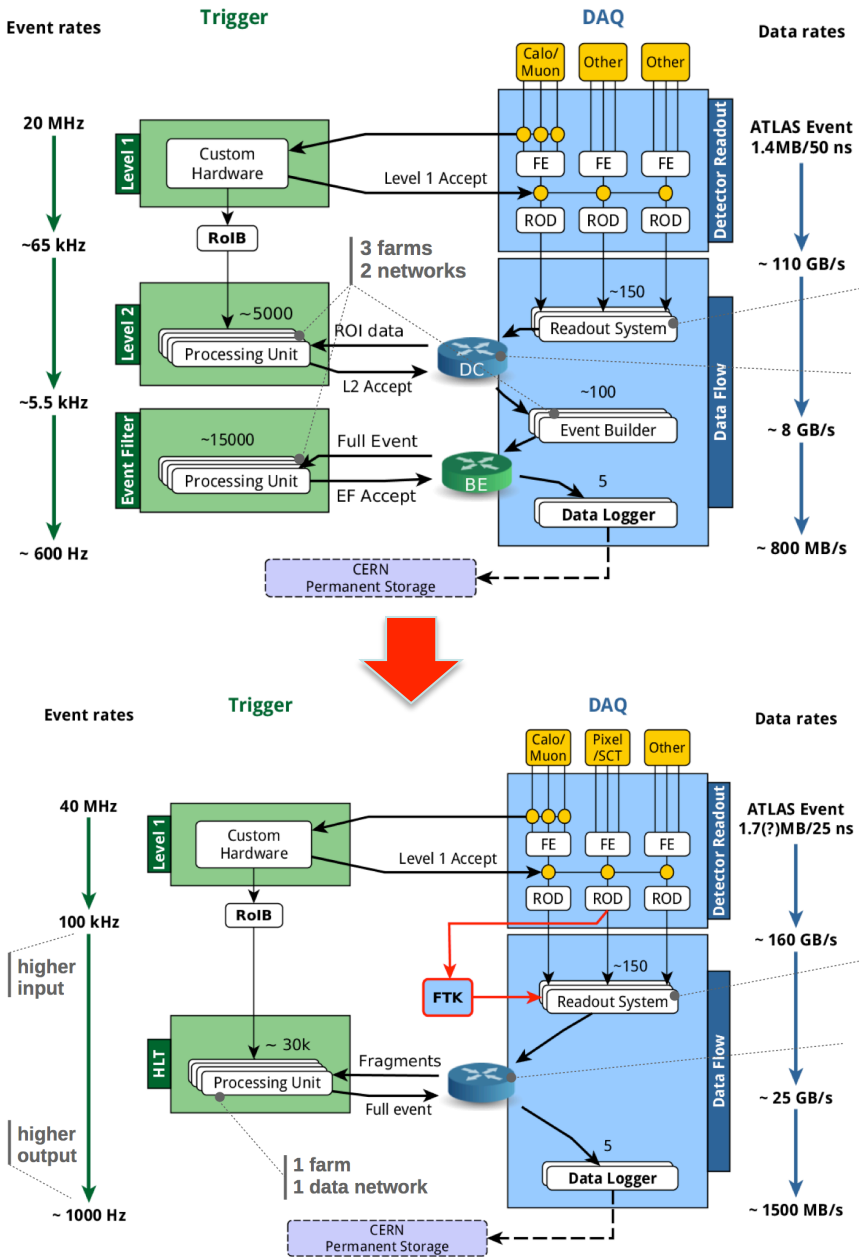
*INFN Pavia

- Dataflow completely redesigned, it is performing well, according with expectations

- A new two-level based architecture (**L1+HLT**) successfully implemented
  - EF, L2 and event builder farms combined together, to create a unique HLT steering
  - possibility for incremental event building
  - steering and algorithms modified accordingly, in order to profit from the new system

- Network redesigned, removing bottlenecks
  - The only limitation is on the disk-writing rate. Present HW allows to reach 3GB/s (0.7 GB/s in run 1)
  - No fundamental modification foreseen in 2016, only minor changes for the coming releases

- No major changes for Phase-1:
  - Farm will be updated via HW rolling replacement with ATLAS fundings (MOF-A)
  - Use of graphics accelerator processors not yet defined
  - Dataflow & computing resources have different timings wrt detector. Computing market is evolving fast and decisions cannot be taken too early



Preliminary trigger and readout schema