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The embedded and high-performance computing sectors have in the past been very isolated and unaware of each other's needs and technologies. Similar isolations have occurred between HPC and the mobile/tablets commodity markets. We are now experiencing a very important convergence between markets, both in constraints and needs as well as in technologies. High computational demands, power consumption limitation, parallelism, heterogeneous computing and cost effectiveness are now driving constraints of both the HPC and embedded sectors. This convergence opens the way to the possibility of performing scientific computation on low power architecture originally developed for the embedded or mobile world. In this talk, we present the panorama of the low power architectures suitable for scientific computation. The INFN experience in building a low power cluster based on System-on-Chips (SoCs) is discussed together with the performance results in terms of power ratio and energy consumption obtained on that cluster. The applications used in the tests range from synthetic benchmarks to real life use cases. Results are compared to those obtained on traditional HPC architectures.

Relatore: CESINI, Daniele (INFN - CNAF)