



# The future of the Calocube prototype

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- General information
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# **Current prototype**

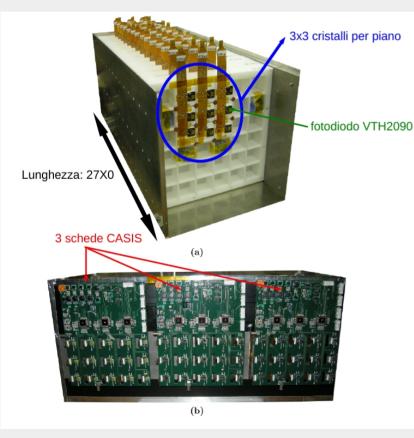
- 15 Layers
- 3 x 3 Csl(Tl) crystals in each layer
- 135 crystals in total
- Crystal side ~ Moliere radius (3.6 cm)
- Crystal distance 0.4 cm
- 135 Big Photo Diodes (VTH2090)
- 3 Small Photo Diodes on the central cube of the third, fourth, fifth layers (VTH9412)

- Crystal are covered by Vikuiti (high efficient reflector).
- 54 cm of Csl
- 29 X<sub>0</sub> <--> 1.46 λ<sub>l</sub>
- Front-end electronics consist of CASIS chip:
  - 1) 16 independent channels
  - 2) charge sensitive amplifier
  - 3) correlated double sampling system
  - 4) automatic gain selection.



### **Current prototype**

# In this image the crystal are covered with Teflon (2013).



In this image the crystals are covered with Vikuiti (2015)



Better light collection with Vikuiti. Double signal with respect to the crystal covered with teflon



### Current prototype: kapton problems

- In the current prototype the kapton cables are welded with photodiodes and are directly connected with the CASIS boards
- Because of the boards position the final section of the cables has a 90 degree bend.
- During the preparation of the Aug. beam test many Kapton cables broke.

The solution for the Aug. and Sept. beam test: replace kapton cables with normal cables.

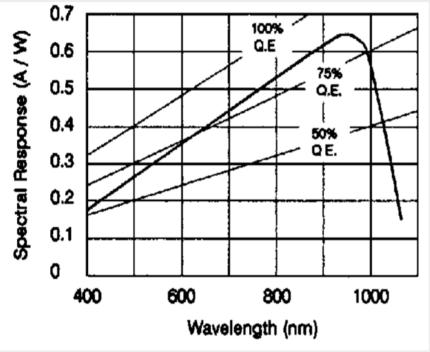
Actually the prototype assembly is <u>very</u> <u>complicated</u>



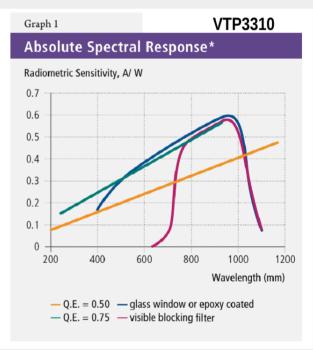


# **Current photo-diodes**

Big photo-diode: VTH2090 active area 84.64 mm<sup>2</sup>



# Small photo-diode: VTH9412 active area 1.6 mm<sup>2</sup>



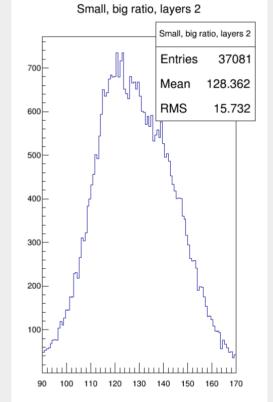
Expected ratio of signals ~90



# **Current photo-diodes**

#### **Expected ratio of signals = ~75**

- We measured the Big/Small ratio of signal in lab. (see Olek presentation)
- From a first online analysis of the test beam (SPS Aug.) I found a ratio of signals ~ 130 (measured with electron at 50 GeV)
- For more details see Miriam presentations
- Open question: differences between estimated and real ratio of signals



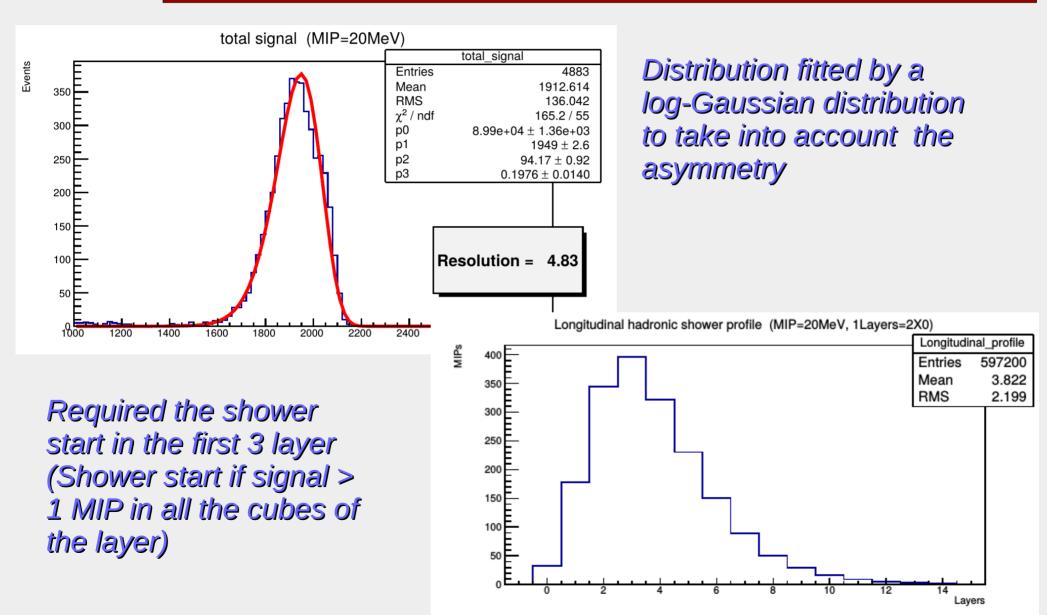
Assuming BigPD/SamllPD = 100

Single crystal max energy With big PD: ~ 30 GeV With small PD: ~3 TeV Beam test: saturation of front-end electronics with big PD for electron @ 150 GeV



# **Prototype performance**

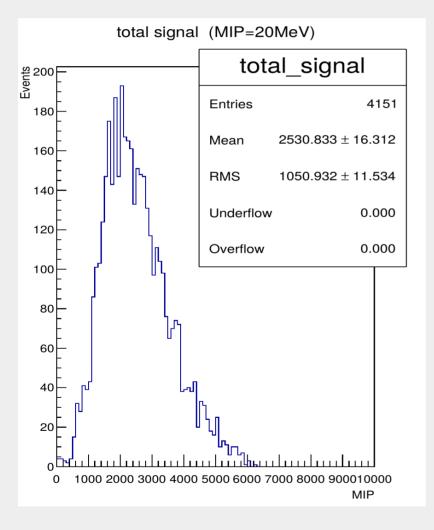
#### **Online analysis: energy resolution for electron @ 50 GeV**





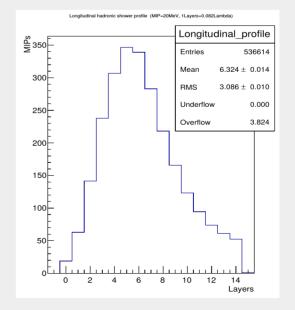
### **Prototype performance**

#### **Online analysis: energy resolution for pion @ 50 GeV**



Resolution = RMS/Mean ~ 40%

Required the shower start in the first 3 layer (Shower start if signal > 1 MIP in all the cubes of the layer)





# **Future prototype**

- 20 Layers
- 6 x 6 CsI(TI) crystals in each layer
- 720 crystals in total
- Crystal side ~ Moliere radius (3.6 cm)
- Horizontal crystal distance 0.4 cm
- Vertical crystal distance (0.4+??) cm
- 720 Big Photo Diodes (VTH2090)
- 720 Small Photo Diodes (VTP9812FH)

- Crystal are covered by Vikuiti (high efficient reflector).
- 72 cm of Csl
- 39 X<sub>0</sub> <--> 1.95 λ<sub>l</sub>
- Front-end electronics consist of HIDRA chip:
  - 1) 28 independent channels
  - 2) charge sensitive amplifier
  - 3) correlated double sampling system
  - 4) automatic gain selection.

Depend on the new mechanical structure



# Numbers of CsI(tl) and photo-diodes

### Crystal

- 77, first order, only one smooth face
- 135, second order, all faces are smooth
- 100+145, third order, all faces are smooth, rounded corners
- 200, next ordder.
- Total: 657



### **Big photodiodes VTH2080**

- 135, in the current prototype
- ~ 355, new
- 170 next order
- Total: 660

### Current small pPhotodiodes VTP9412

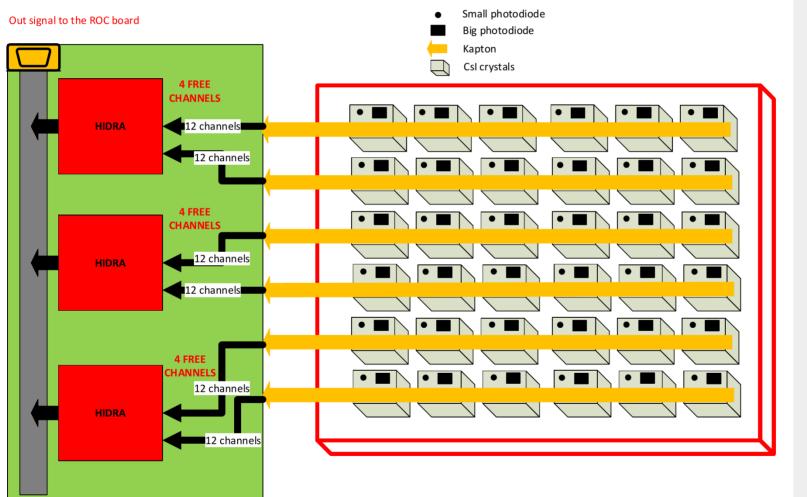
- 135 in the current prototype
- ~ 50 new

### New small photodiodes VTP9812

• 3!!



### Future prototype: front-end electronic



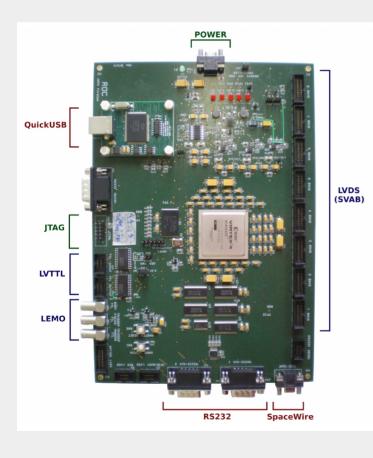
### HIDRA chp

- 40 alreay present
- We nedd
   ~30 HIDRA



# Future prototype: DAQ

ROC (Read Out Controller) board
FPGA Xilinx R Virtex 4



- Actually the ROC board has 32 LVDS outputs and 32 LVDS inputs
- The new front-end electronics configurations need a new board with at least 40 inputs and 18 outputs

#### Two possible solutions:

- Replace some output with some input: we need to replace at least one LVDS transmitter with a receiver
- Adding a small multiplexer LVDS board for the input signals

With the actual board the first solution is simplest but we will obtain only 16 output (48 input)!!! We are working on it.

### Future prototype: mechanical structure

#### **Single layer examples**

- In the future prototype the kapton cables will be welding with photodiodes and will be connected to the mechanical structure of the single layer
- No bend for the kapton cables
- The link between the HIDRA board an the kapton cables consist of flexible cables



### Future prototype: mechanical structure

- General mechanical structure: "chest of drawers"
- The single layers are the drawers
- The HIDRA board will remain out of the man box
- The prototype assembly should be not so difficult
- It will be easy to disassemble the electronic boards
- We would like to develop a small mechanical structure for the single layer test.

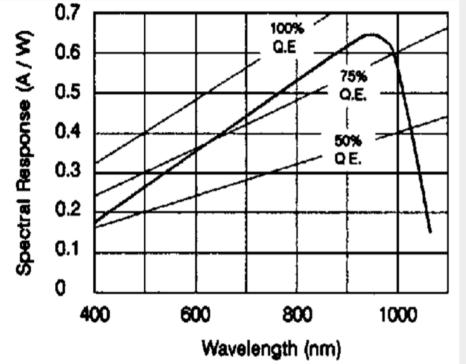


The distance between the layers will be > 0.4mm !!

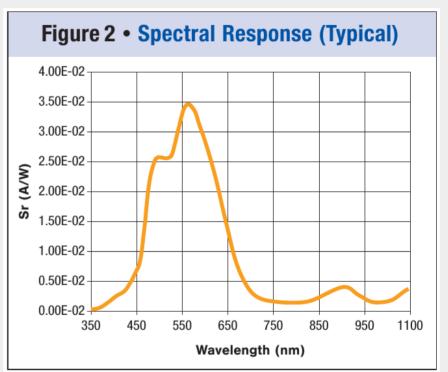


# **Future photo-diodes**

Big photo-diode: VTH2090 active area 84.64 mm<sup>2</sup>



Small photo-diode: VTH9812 active area 1.6 mm<sup>2</sup>, black package!!



#### **Expected ratio of signals ~ 1000**

Single crystal max energy With big PD: ~ 30 GeV With small PD: ~ 30TeV Expected saturation of the front-end electronic with small PD for electron > 150TeV



### Conclusion

- The future prototype completely contain the electromagnetic shower (39  $X_0$ )  $\rightarrow$  good energy resolution (<2% for electron @ 1TeV)
- The increase of the number of interaction ( 1.95  $\lambda_l$ ) length allow measurements protons and nuclei energy (resolution ~ 35% proton @ 1TeV).
- The assembly and test of the calorimeter will be simpler thanks to the new mechanical and electronic configuration

#### **Open topics**

Precise measurement of Big/Small PD ratio of signal.

Modify the ROC board for the new front-end electronic configuration.

Select the layers distance in order to preserve a good resolution for electrons.