CAM with Pipelined Hierarchical Search Scheme

Report no. 2

October, 27th, 2015

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Outline
Summary

- Introduction
- Match-Line Single Layer
  - Single-Bit CAM Cell
  - Match-Line Sense Amplifier
- Low-Swing Receiver
- Simulation Results
  - 8 Match-Line Layers Simulation Results
- Conclusions, Status and Future Activities

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Introduction

Specifications

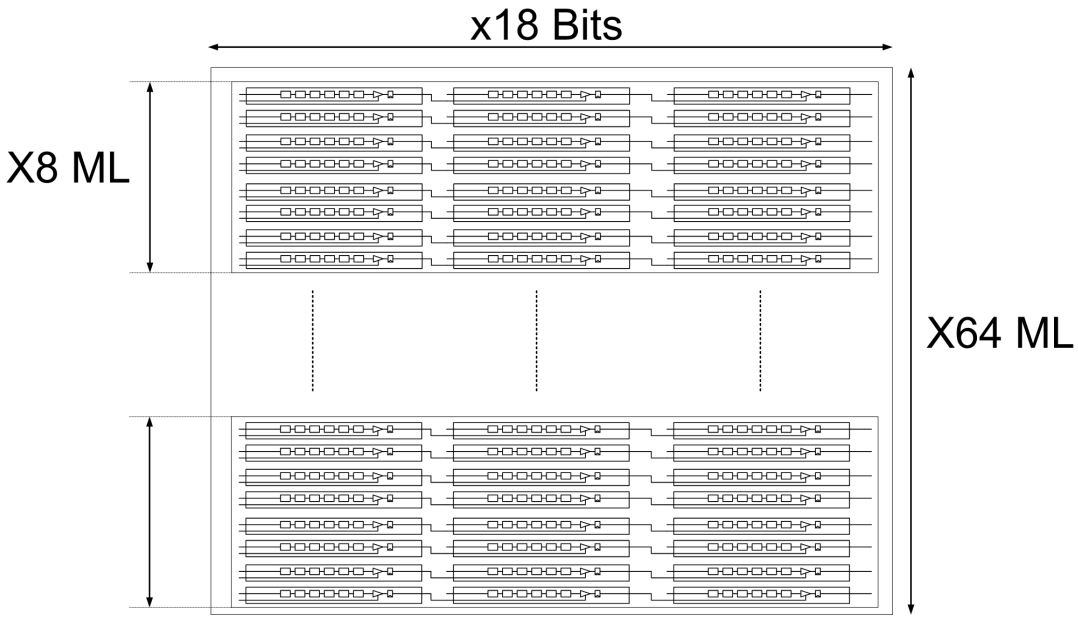

Fig. 1 – Generic Top-View of the 18x64 Bits CAM Block.

Resolution	18 SL x 64 ML
Pipelined Match-Line	3x6 Cells
Hierarchical Search-Line	8x8 Cells
VDD	0.9 V
CMOS	28nm
Clock	100/200 MHz

- CAM Block Bits Resolution is 18x64.
- 18 Bits Search-Line
- 64 Bits Match-Line
- 18x64=1152 CAM Cells
- Saving Power by Pipeline Scheme (3 stages of 6 bits for each Match-Line).

[1] k. Pagiamtzis et al. “Content-Addressable Memory (CAM) Circuits and Architectures: A Tutorial and Survey”. IEEE Journal of Solid-State Circuits, VOL. 41, NO. 3, March 2006.

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Match-Line Single Layer

CAM Functional Block Scheme

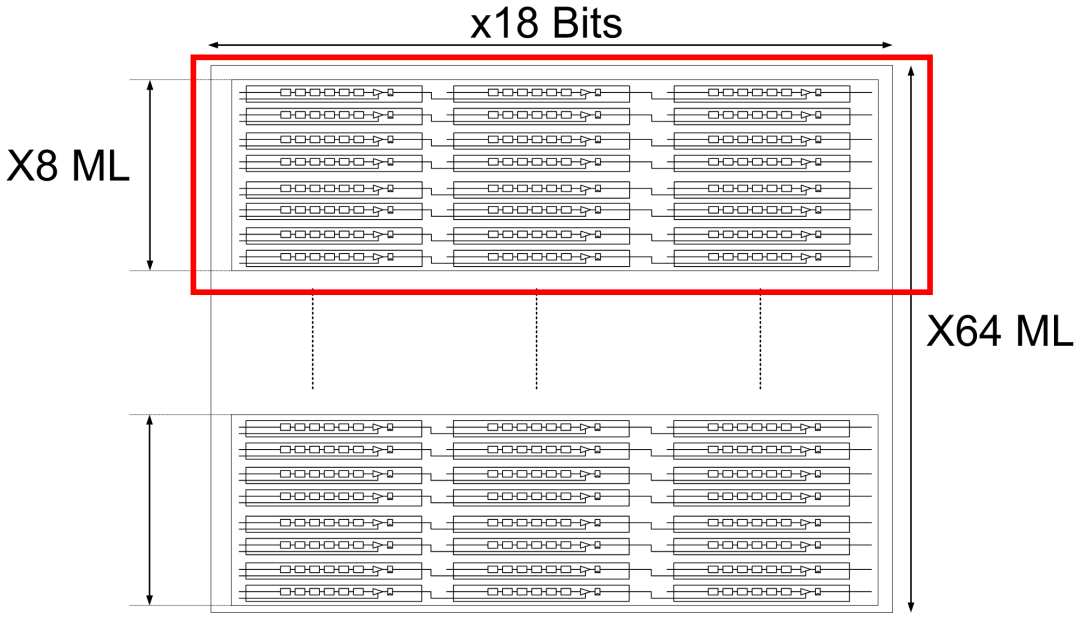

Fig. 2 – Generic Top-View of the 18x64 Bits CAM Block.

Resolution	18 SL x 64 ML
Pipelined Match-Line	3x6 Cells
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CMOS	28nm
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- 18x8ML Block.
- Power Consumption Minimization is under evaluation.

Match-Line Single Layer
CAM Functional Block Scheme

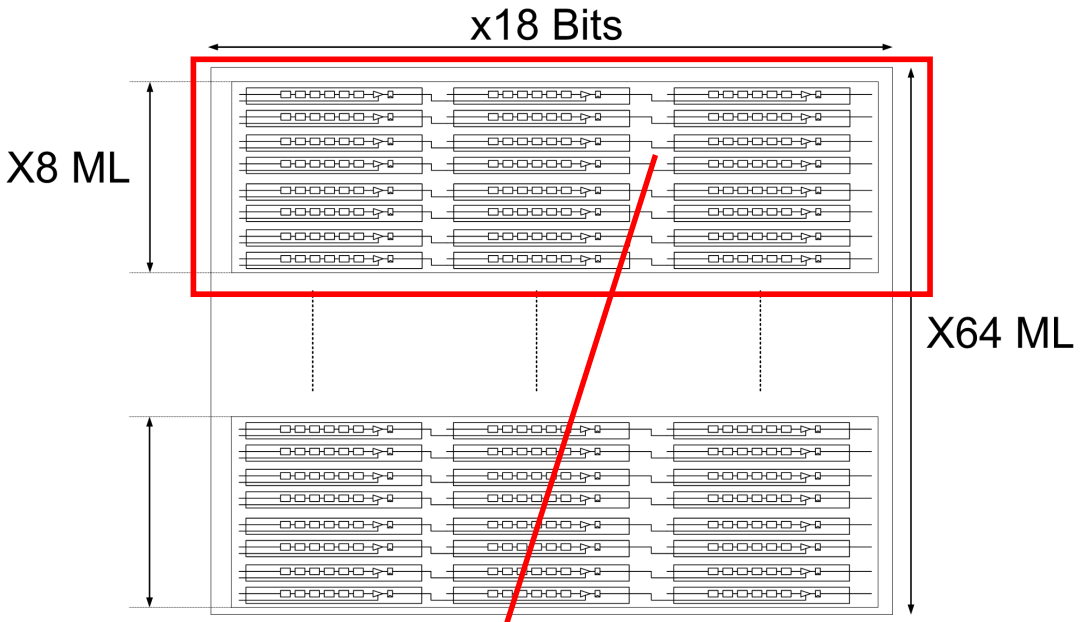


Fig. 3 – Generic Top-View of the 18x64 Bits CAM Block.

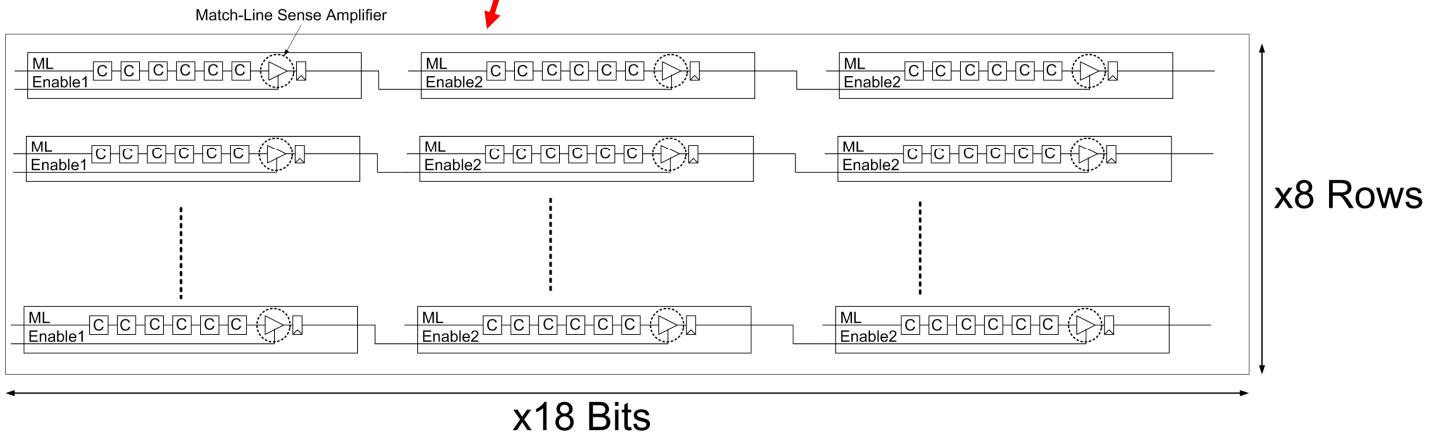


Fig. 4 – Generic Top-View of the 18x8ML Bits CAM Block.

Match-Line Single Layer
CAM Functional Block Scheme

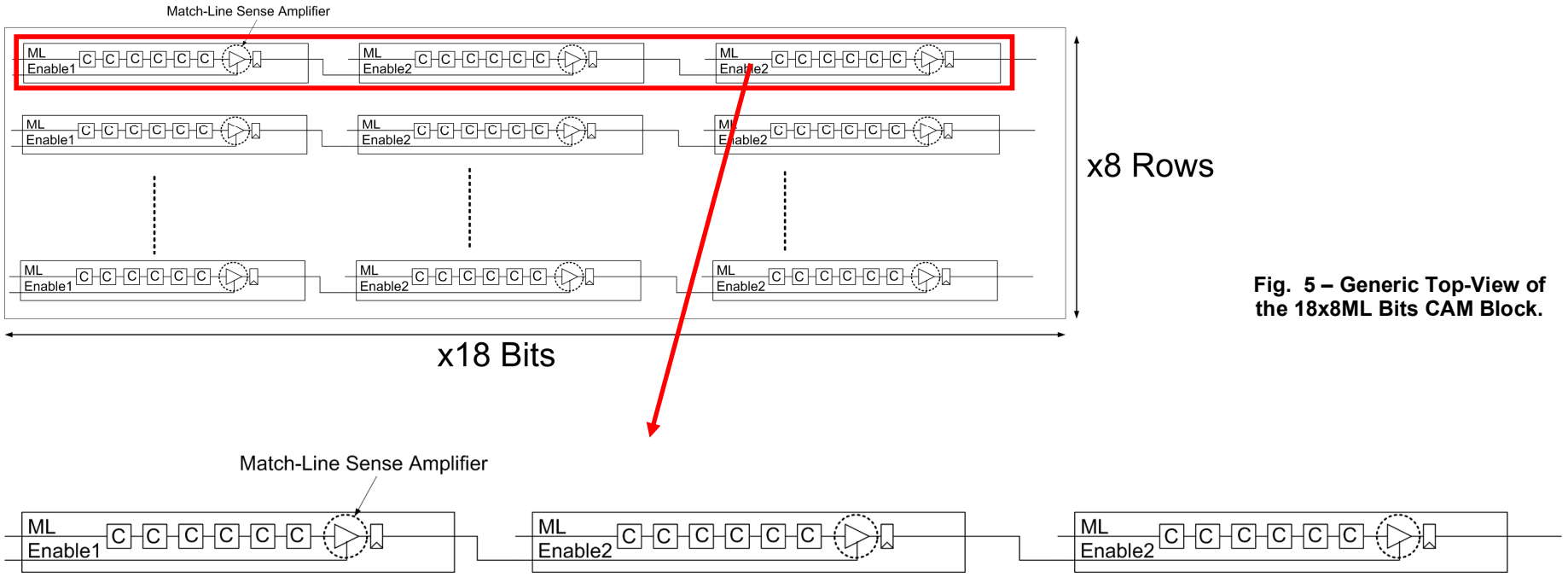


Fig. 5 – Generic Top-View of the 18x8ML Bits CAM Block.

- Each Match-Line Layer is composed by 3-Stages of 6 bits.
- Each Stage is pipelined with the following
  - Example: If the Stage1 does not match, then the Stage 2 is not activated (Enable2='0')
- Each Stage is composed by:
  - 6 CAM Cells (i.e. 6 bits)
  - 1 Match-Line Sense Amplifier (for buffering)
  - 1 D-Flip-Flop (for synchronization with the reference clock =200MHz)

Match-Line Single Layer

Single Bit CAM Layer

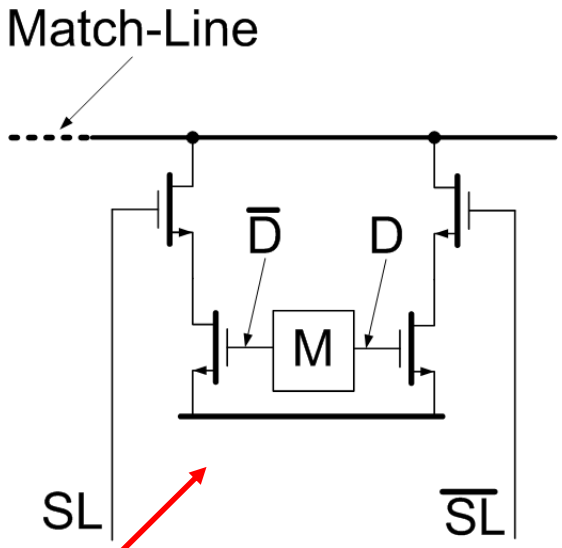
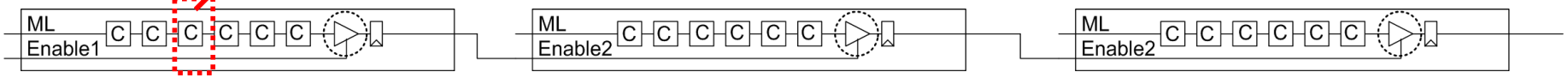


Fig. 6 – NOR CAM Cell.

SL	D		ML	CAM Cell Operation	
0	0		1	High-Impedance	MATCH
0	1		0	Ground	MISS
1	0		0	Ground	MISS
1	1		1	High-Impedance	MATCH



- Single CAM Cell is based on a NOR scheme.
- Match-Line is ground in case of a MISS.
- Match-Line is 1 (pre-charged) in case of a MATCH.

Match-Line Single Layer

Single Bit CAM Layer

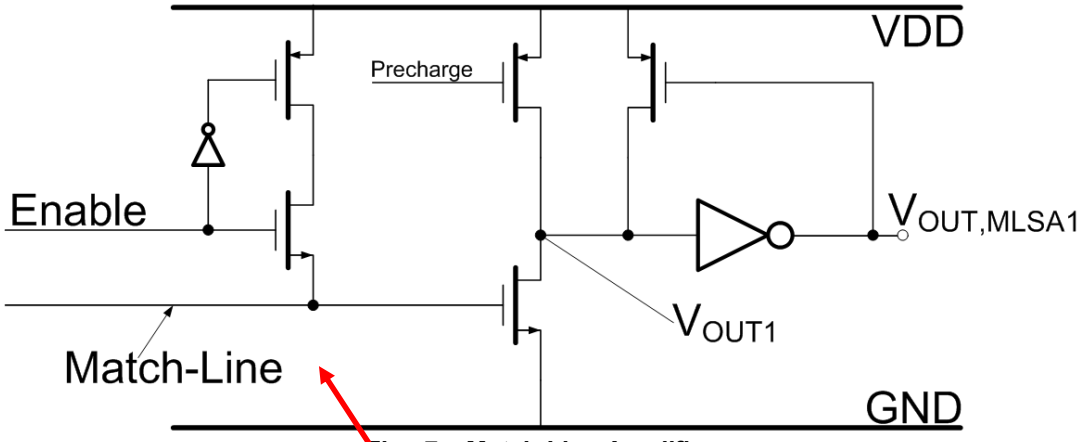
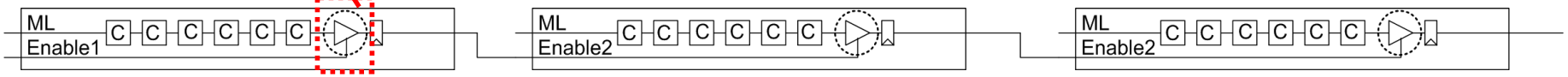


Fig. 7 – Match-Line Amplifier.



- Enable is ‘1’ when the previous stages have provided a MATCH.
- Match-Line is pre-charged to ‘1’.
- During The PreCharge (active low) Phase, $V_{OUT,MLSA1}$ is at ‘0’.

Match-Line Single Layer

Single Bit CAM Layer

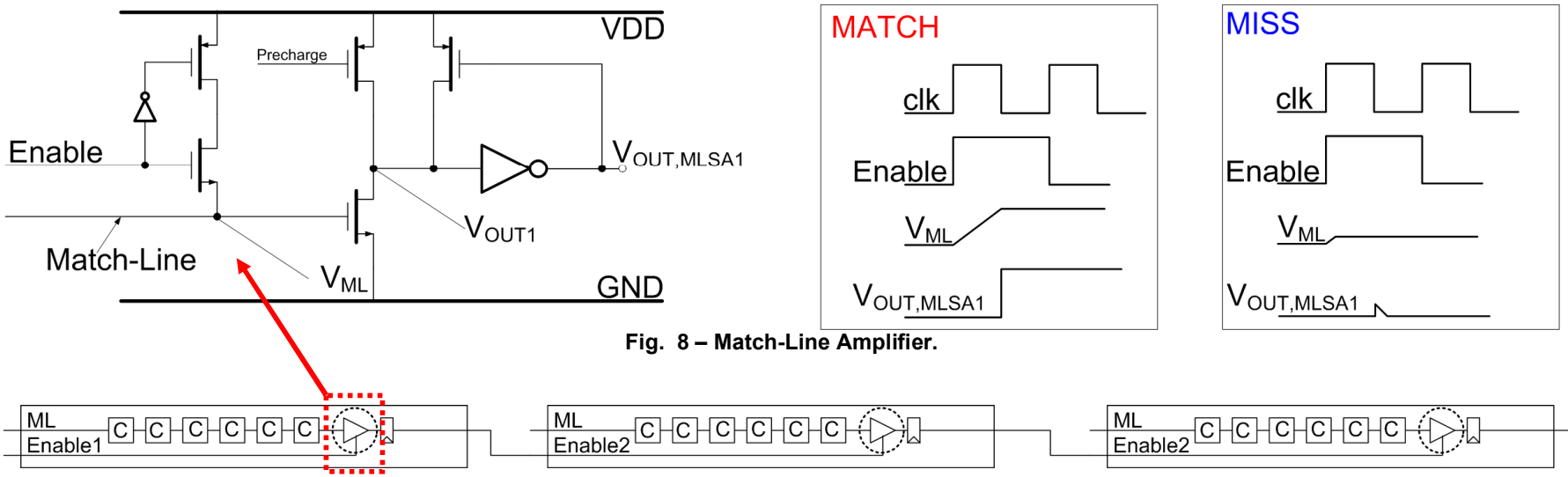


Fig. 8 – Match-Line Amplifier.

- If ML='0' and Enable='1' then
  $V_{OUT,MLSA1}$ is '0'.
- If ML='1' and Enable='1' then
  $V_{OUT,MLSA1}$ is '1'.

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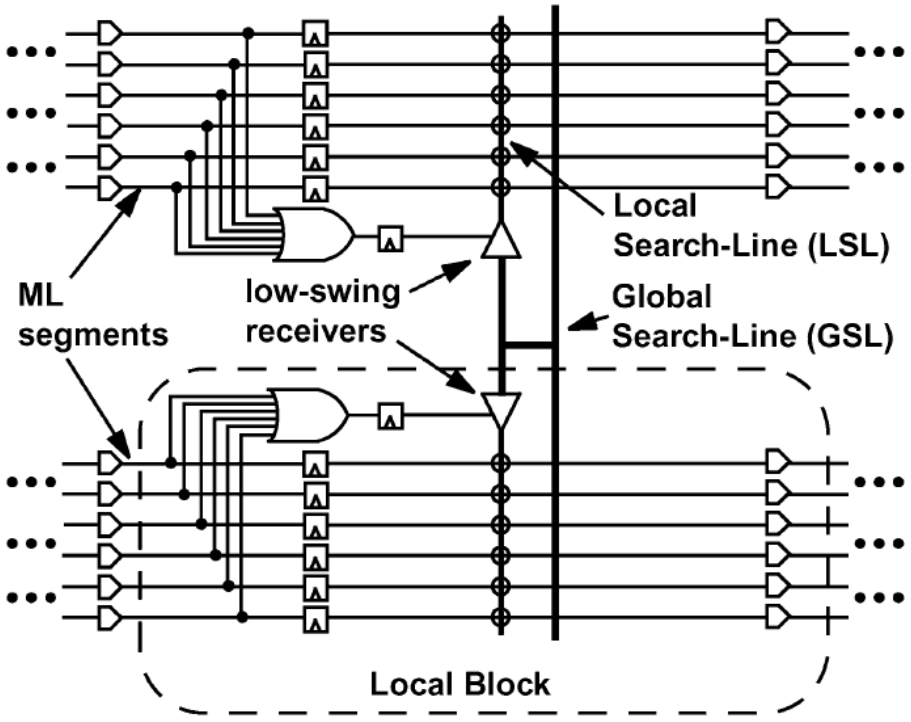
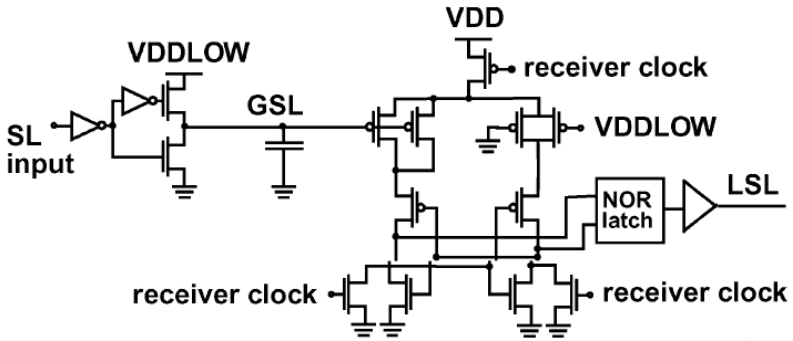
Low-Swing Receiver

Top-View





- A specific Low-Swing Receiver has been designed for driving local search-line
- Global search-line is biased at VDD_{LOW}=0.5V (Standard VDD=0.9V)

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Simulation Results

Test-bench Layer Schematic.

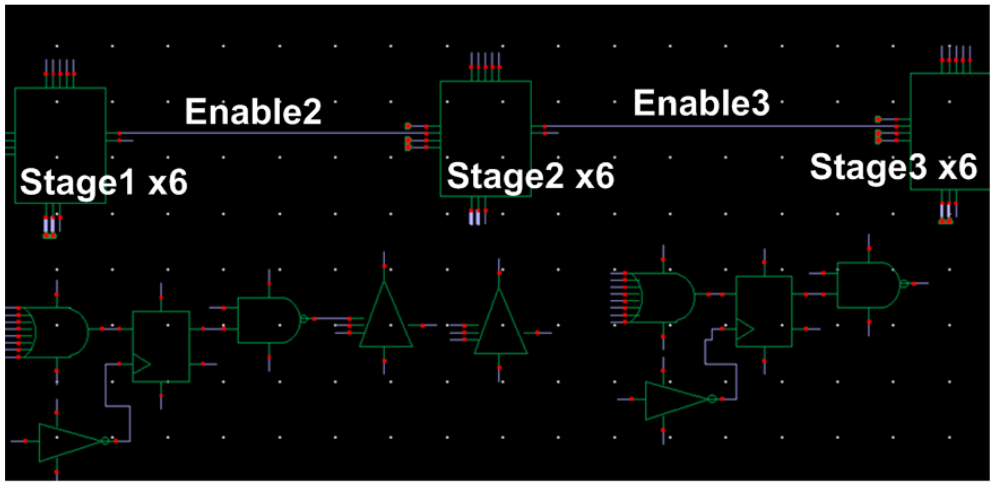


Fig. 9 – Test-Bench Schematic.

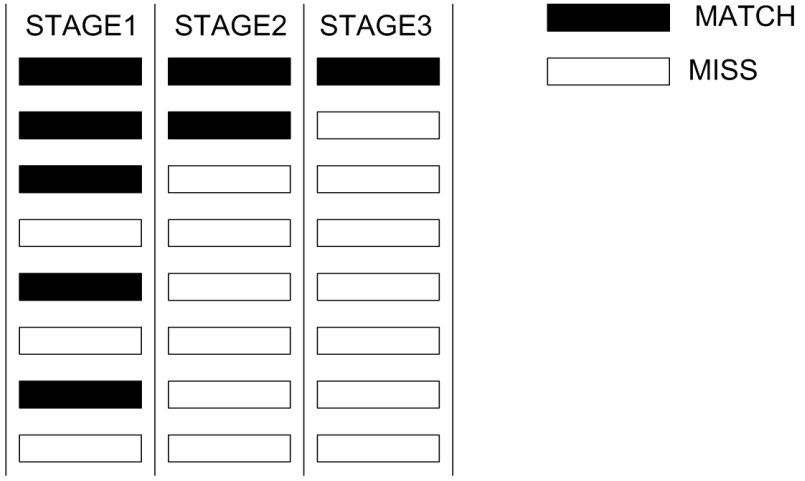
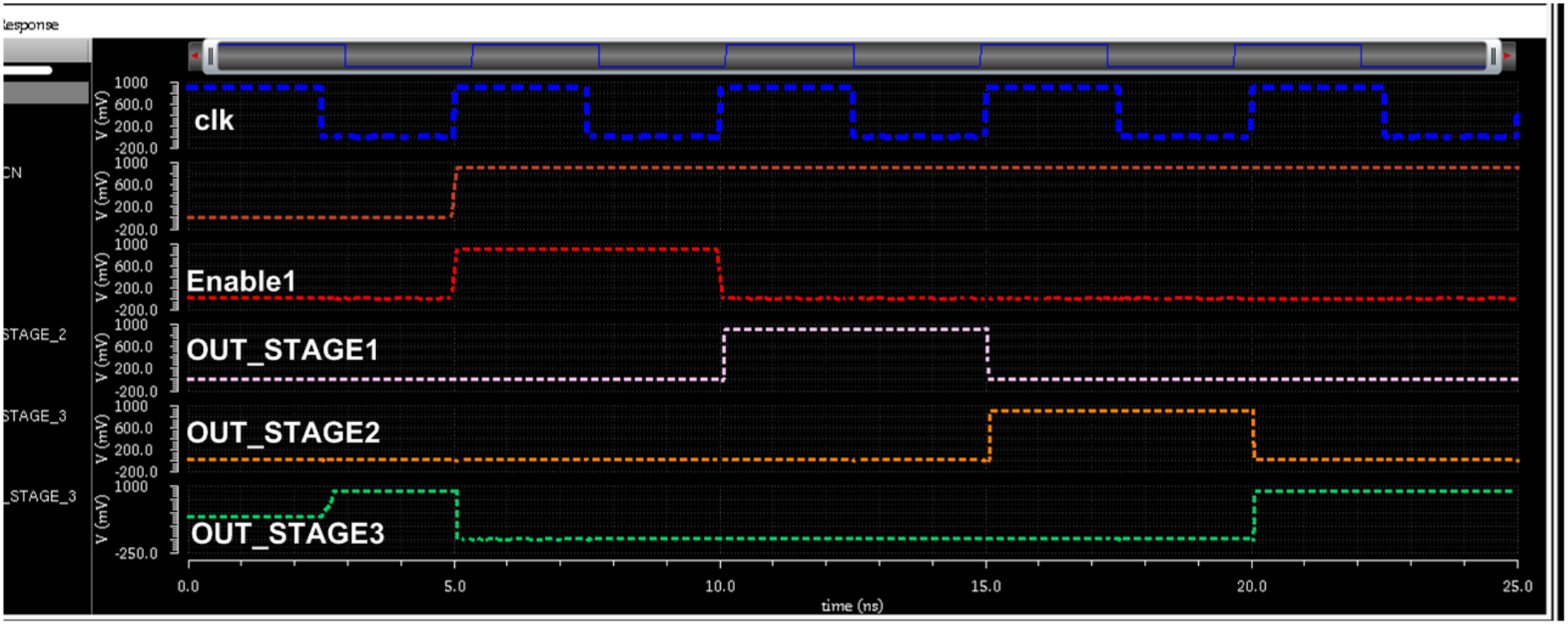


Fig. 10 – Pattern.

- 1 corner with 4 different patterns have been simulated in nominal conditions.
  - o 0,1,2,3 Matches to check the pipeline functionality.
- Every block in the stages (CAM cell, MLSA, Low-Swing Receiver, Control Logic) is transistor-level.

Simulation Results

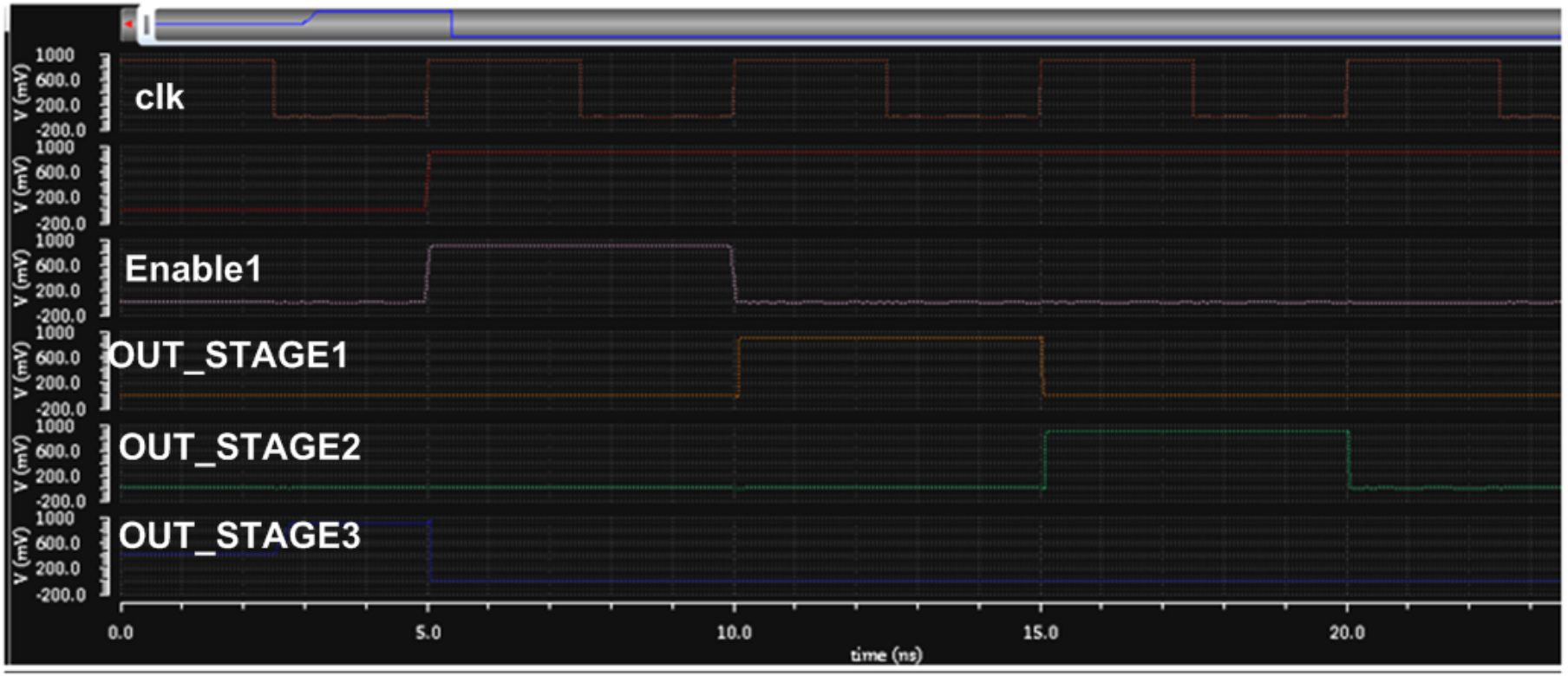
Single Layer Simulation Results. All Matches.



	Stage1	Stage2	Stage3
Match-Line Sense AMPLIFIER POWER	1.8 uA	1.8 uA	1.8 uA
Flip-Flop	1.3 uA	1.3 uA	1.3 uA
POWER per CELL	0.7 uA		
SINGLE Layer TOTAL POWER	**12.7 uA**		

Simulation Results

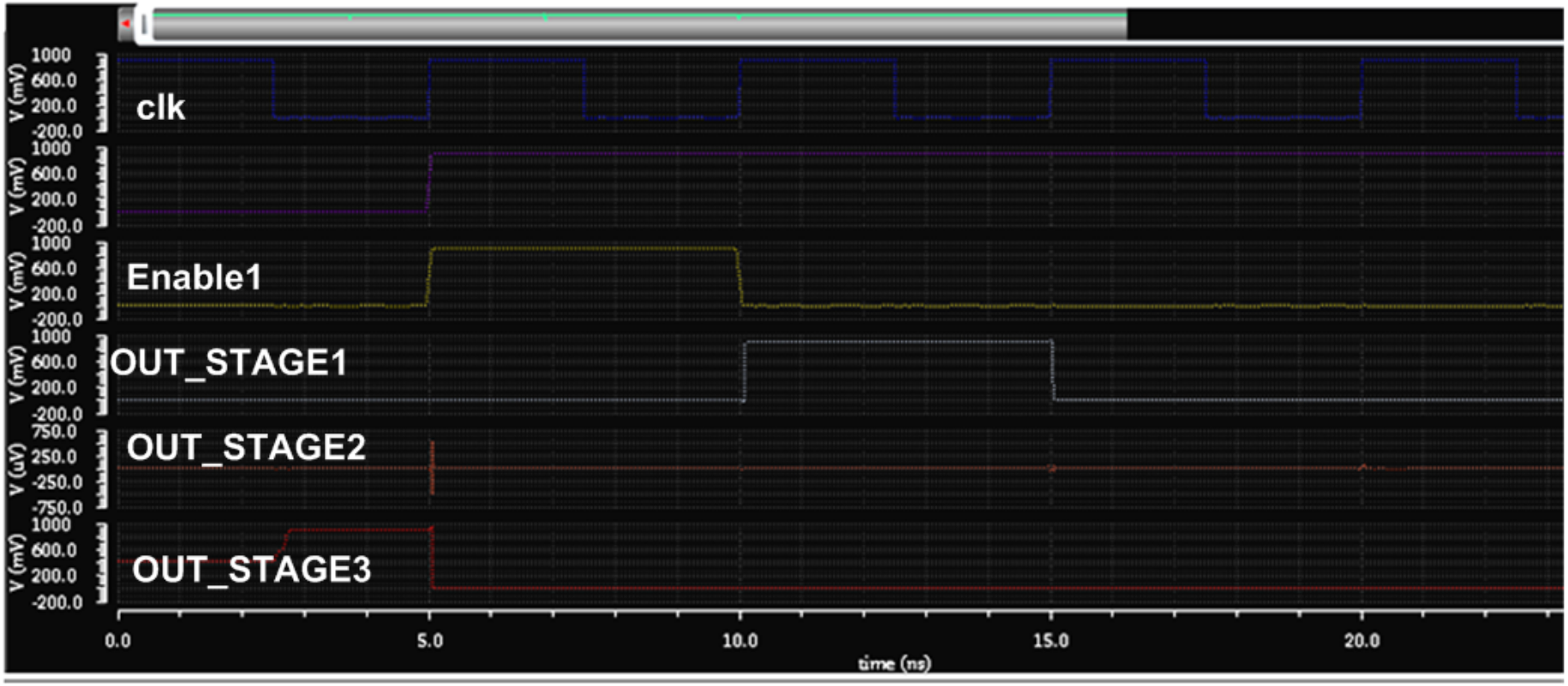
Single Layer Simulation Results. 2 Matches.



	Stage2	Stage3	Stage2
Match-Line Sense AMPLIFIER POWER	1.8 uA	1.8 uA	3.8 uA
Flip-Flop	1.3 uA	1.3 uA	1.3 uA
POWER per CELL	0.78 uA		
SINGLE Layer TOTAL POWER	**14 uA**		

Simulation Results

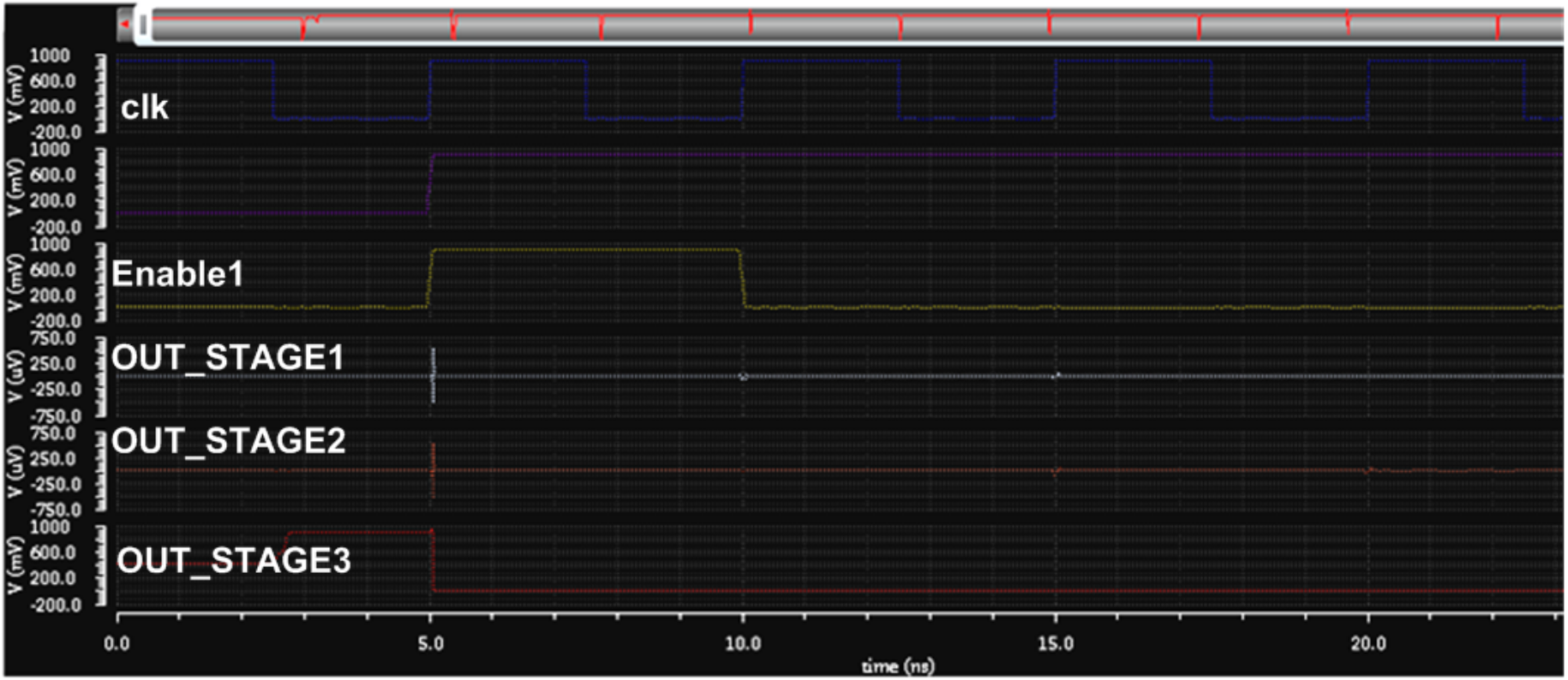
Single Layer Simulation Results. 1 Matches.



	Stage2	Stage3	Stage2
Match-Line Sense AMPLIFIER POWER	1.8 uA	3.8 uA	33 nA
Flip-Flop	1.3 uA	1.3 uA	1.3 uA
POWER per CELL	0.62 uA		
SINGLE Layer TOTAL POWER	**11.2 uA**		

Simulation Results

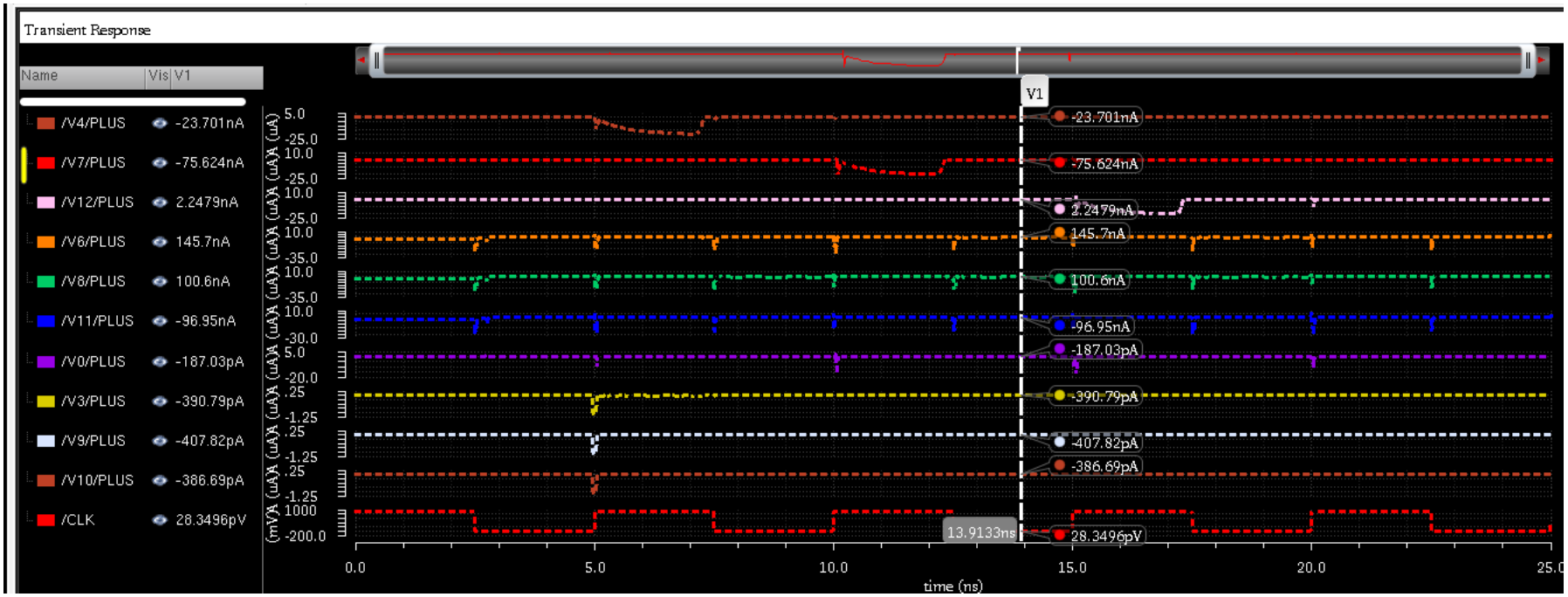
Single Layer Simulation Results. 0 Matches.



	Stage2	Stage3	Stage2
Match-Line Sense AMPLIFIER POWER	3.8 uA	33 nA	33 nA
Flip-Flop	1.3 uA	1.3 uA	1.3 uA
POWER per CELL	0.57 uA		
SINGLE Layer TOTAL POWER	**9.5 uA**		

Simulation Results

Single Layer Simulation Results. 2 Matches.



- Static current is always negligible with respect to the dynamic current.
- The stage are efficiently controlled and switched-off.

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Simulation Results

Conclusions, Status and Future Activities.

Resolution	18 SL x 64 ML
Pipelined Match-Line	3x6 Cells
Hierarchical Search-Line	8x8 Cells
VDD	0.9 V
CMOS	28nm
Clock	200MHz
POWER per CELL	0.544µW
TOTAL POWER (fixed Pattern, 18x8 cells)	78.4µW

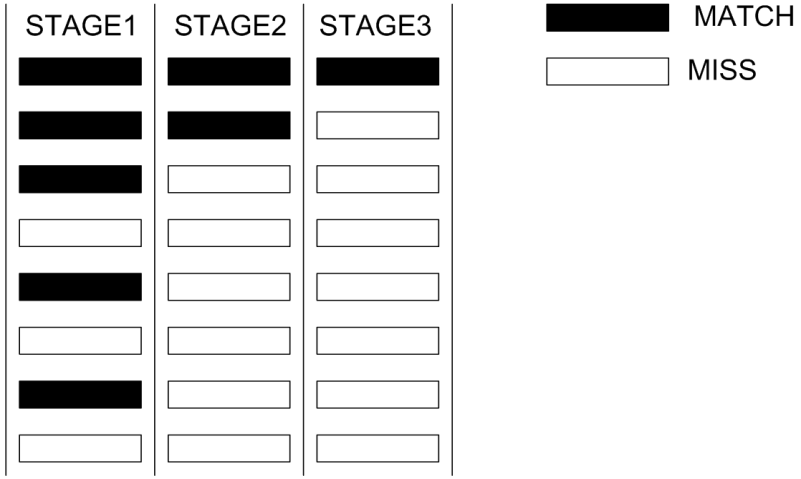

Fig. 11 – Pattern.

- Completing the 18x64 Architecture.
- PVT Simulations.
- Layout.
- Post-Layout Simulations.
- Post-Layout Optimization.

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