New Sensors

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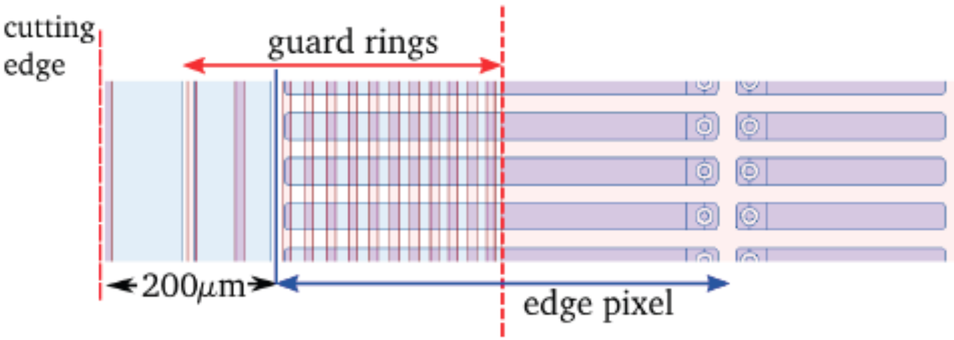
Outline

- Introduction
- CMOS sensors
- LGAD
- 3D and Active Edge
- Conclusion

State of the art in Si hybrid pixels for HEP

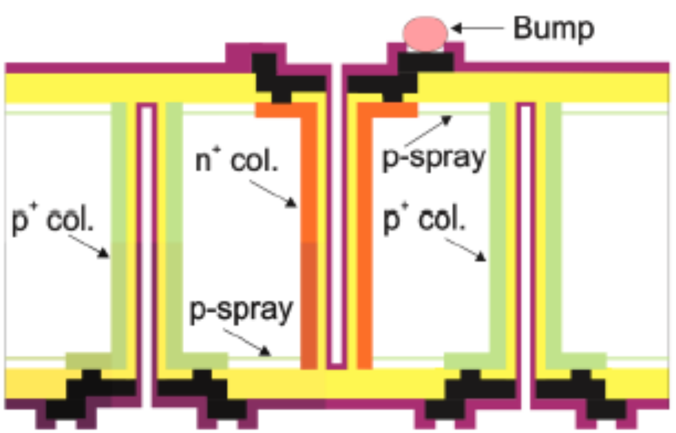
ATLAS IBL pixels

- Planar n-on-n (200 μm thick)



S. Altenheiner et. al. JINST 7 (2012) C02051

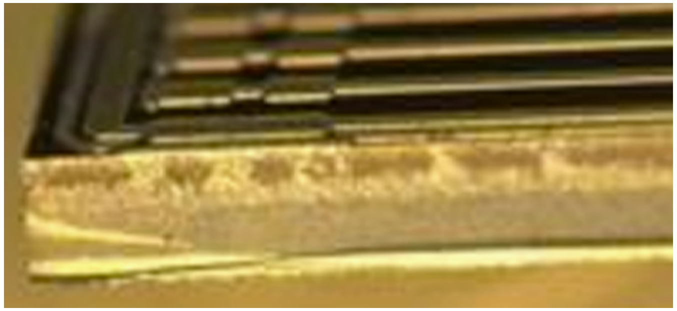
- Double-sided 3D (230 μm thick)



C. Da Via et. al. NIMA 694 (2012), 321

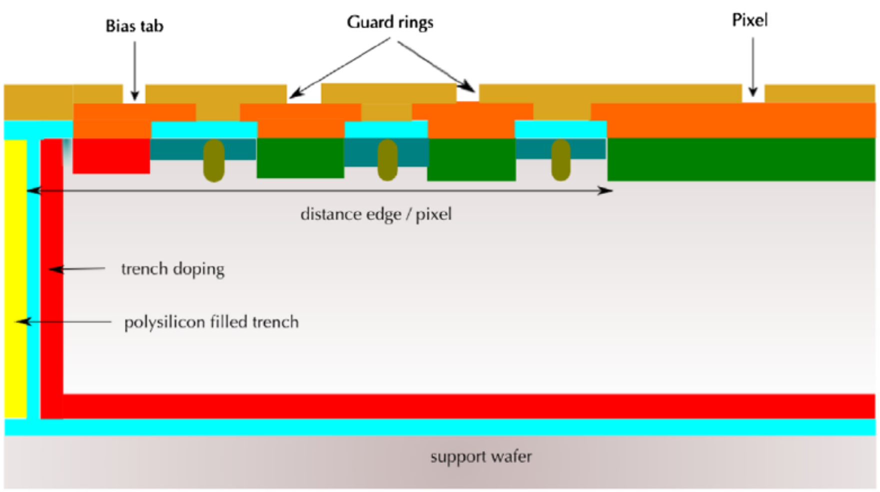
Other emerging technologies

- Thin planar n-on-p
- Slim and active edges



Scribe
Cleave
Passivate

V. Fadeyev et al., NIMA 731 (2013) 260



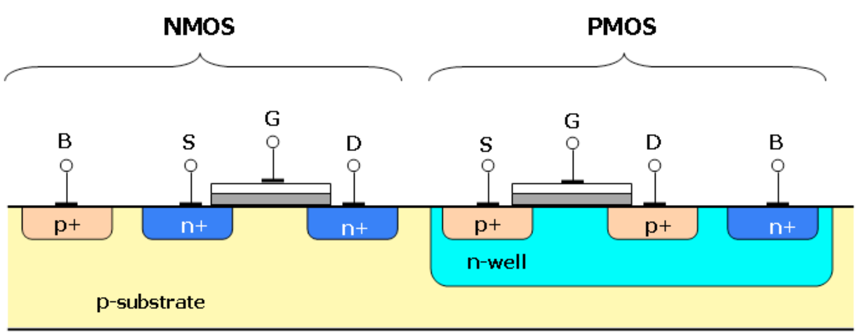
M. Bomben et al., NIMA 730 (2013) 215

An alternative: CMOS sensors

N. Wermes, TALENT ITN Final Conference (CERN 2015)

- Due to many advantages in terms of cost, mass production, reliability, low material, spatial resolution, etc., CMOS sensors have been attracting increasing interest in the recent years
- The ALICE Inner Tracking System upgrade at LHC (~10 m^2) will use monolithic CMOS pixels (Tower Jazz 0.18 um imaging process)
- But CMOS is not favored in terms of sensor performance (active thickness, charge collection, speed, …)
- Need to exploit special technology features to make better detectors:

→ **multiple wells (transistor shielding, competing electrodes …)**
→ **High Voltage capabilities**
→ **some (thin) depletion layer**
→ **wafer thinning**
→ **backside contacts**
→ **…**



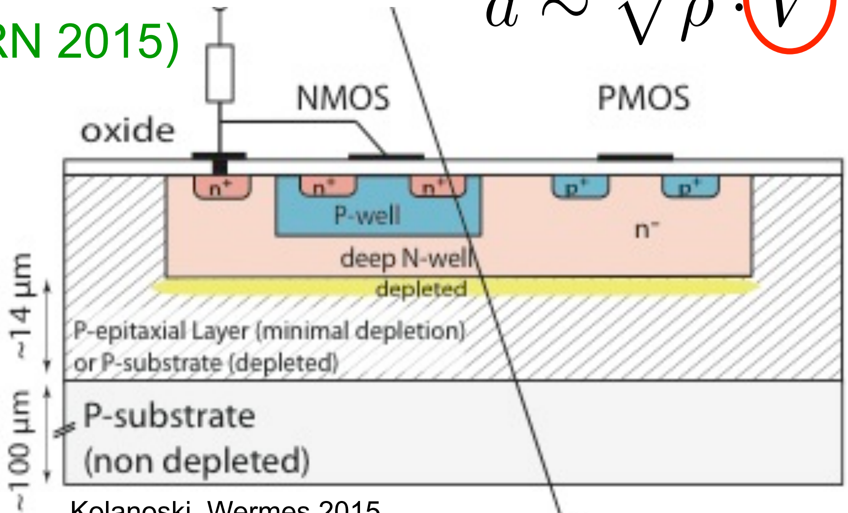
Current approaches (1): HV-CMOS

$$d \sim \sqrt{\rho \cdot V}$$

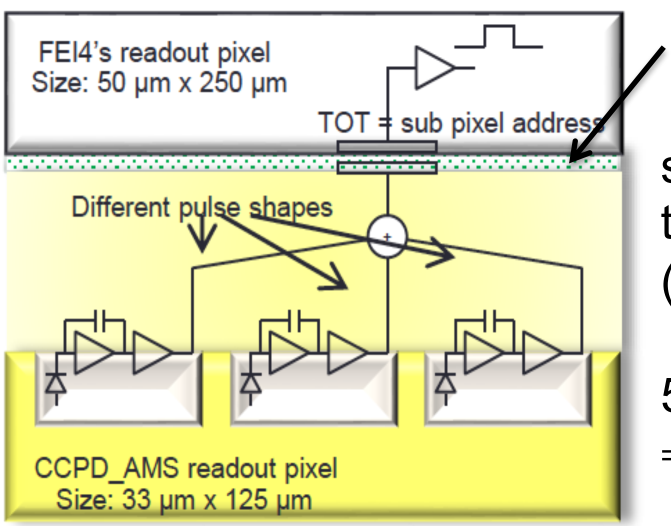
N. Wermes, TALENT ITN Final Conference (CERN 2015)

I. Peric et al. NIMA 582 (2007) 876-885
NIMA 765 (2014) 172-176

- AMS 350 nm and 180 nm HV process (p-bulk) ... 60-100 V
- deep n-well to put nMOS (in extra p-well) and pMOS (limitation)
- ~ 10 - 15 μm depletion depth → 1-2 ke signal
- various pixel sizes (~20 x 20 to 50 x 125 μm^2)
- full 1 cm^2 "demonstrator" matrix sub. 10/15



Kolanoski, Wermes 2015

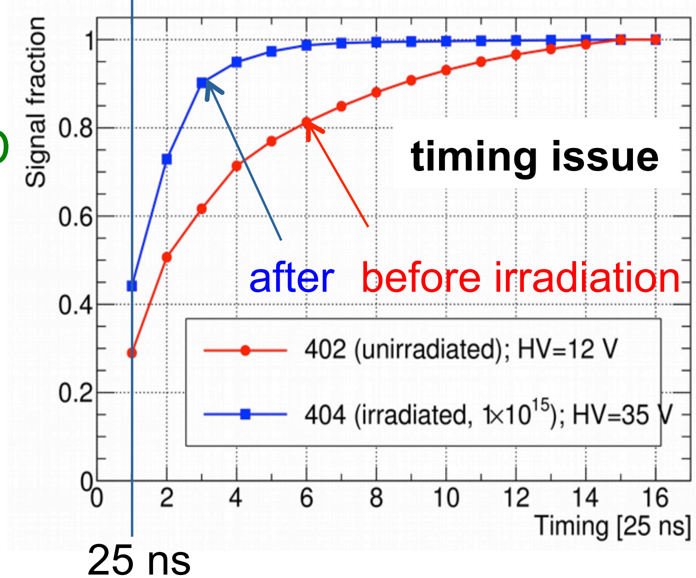


Glue (CCPD)
CNS5 HVR-CCPD

sub-pixel decoding through pulse shape (TOT => sub-address)

$50 \times 250\ \mu m^2$
$\Rightarrow 33 \times 125\ \mu m^2$ effectively

test beam

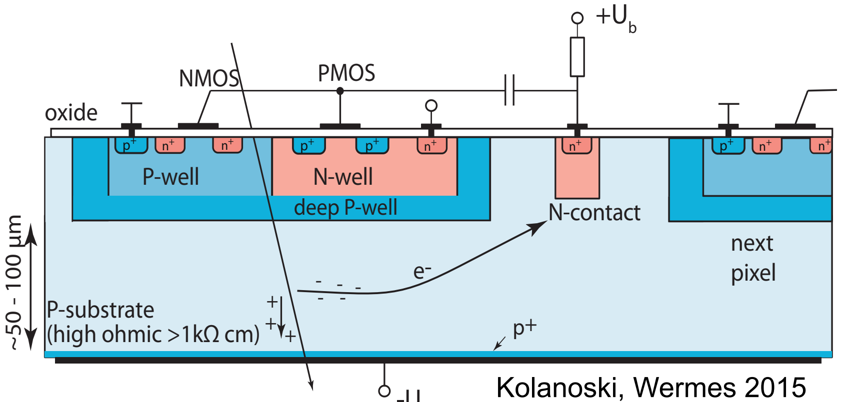


Current approaches (2): HR-CMOS

$$d \sim \sqrt{\rho \cdot V}$$

N. Wermes, TALENT ITN Final Conference (CERN 2015)

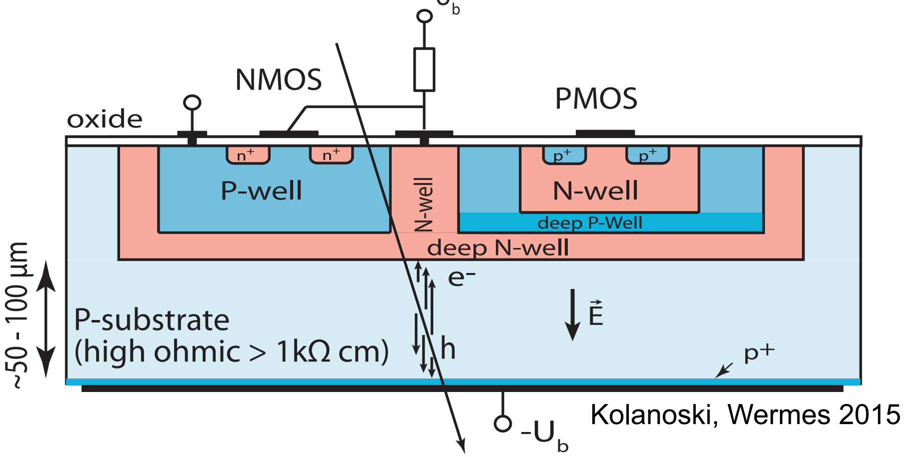
Mattiazzo, S,. W. Snoeys et al., NIM A718 (2013) 288-291
Havranek, Hemperek, Krüger, Wermes et al., JINST 10 (2015) 02, P02013



Kolanoski, Wermes 2015

- (D)MAPS like configuration but w/ depleted bulk
- small collection node
- long drift path

⇒ **smaller C, more trapping**



Kolanoski, Wermes 2015

- deep n and deep p wells
- large collection node
- short drift path

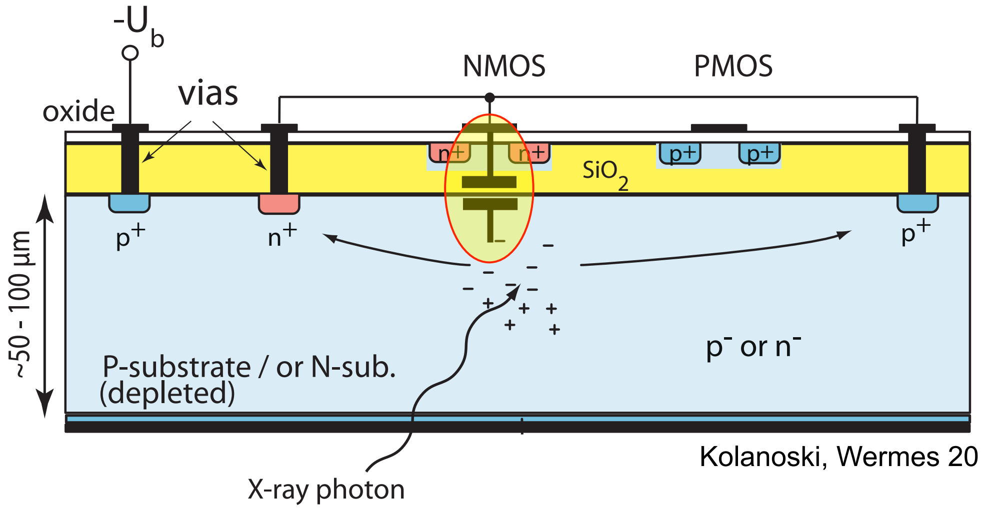
⇒ **larger C, less trapping**

CSN5
SEED project

Promising results from LFoundry and ESPROS prototypes (150 nm)

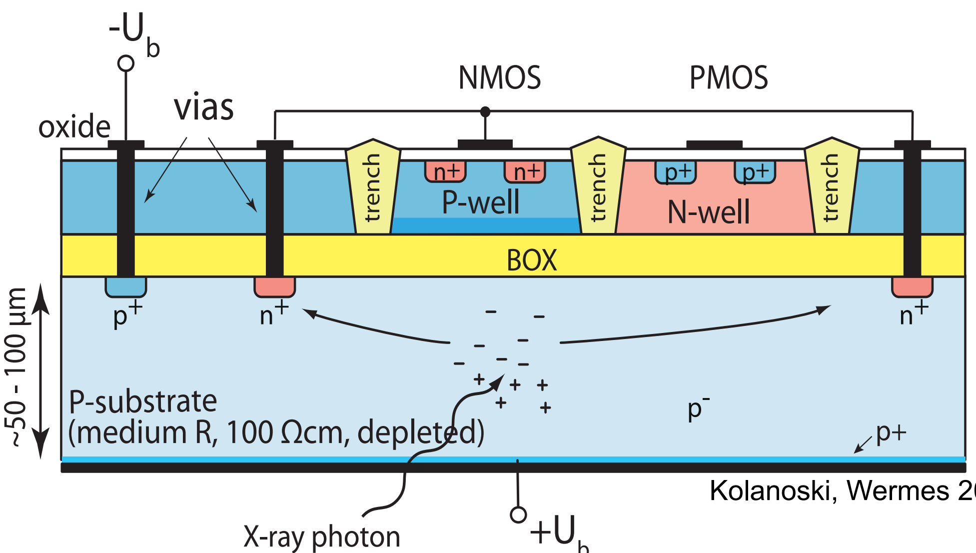
Current approaches (3): HV-SOI

N. Wermes, TALENT ITN Final Conference (CERN 2015)



Kolanoski, Wermes 2015

- **FD-SOI**
- OKI/LAPIS/KEK
  Y. Arai et al.
- issues
  - back gate effect
  - radiation issues due to BOX
- cures invented in recent years
- Not suited for high radiation hardness

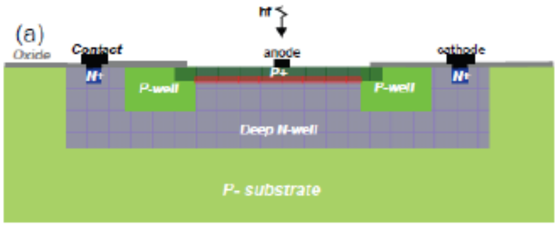


Kolanoski, Wermes 2015

- **HV-SOI (thick film)**
- Hemperek, Kishishita, Krüger, NW
  doi:10.1016/j.nima.2015.02.052
- a promising alternative
- doped, non-depleted P- and N-wells prevent back gate effect and increase the radiation tolerance
  (Vth shift < 100mV @1Grad)

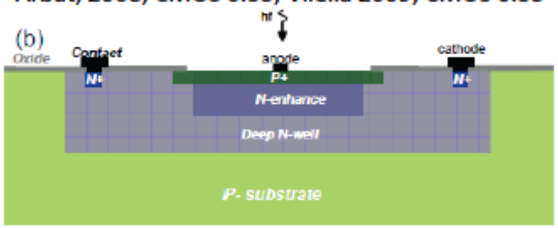
SPAD in CMOS Technology

(a)



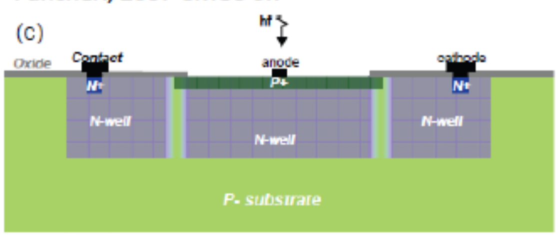
Goetzberger, 1963; Cova,1981; Kindt, 1994; custom
Rochas, 2002, CMOS 0.8; Niclass, 2007, CMOS 0.13;
Arbat, 2008, CMOS 0.35, Vilella 2009, CMOS 0.35

(b)



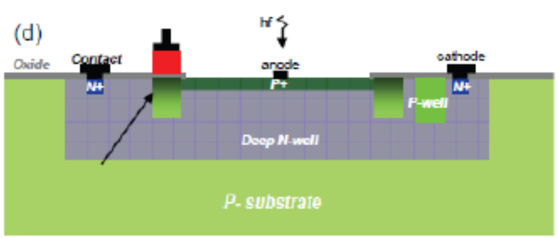
Petrillo, 1984; Ghioni, 1988, Lacaita, 1989, custom
Pancheri, 2007 CMOS 0.7

(c)



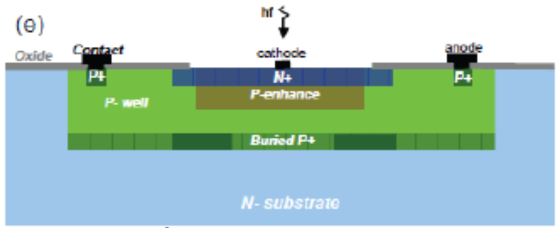
Pauchard, 2000; custom
Rochas, 2001, CMOS 0.8

(d)



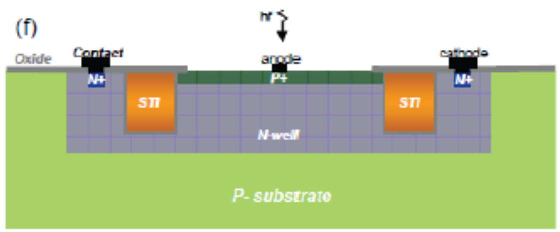
Rochas, 2003, CMOS 0.8; Xiao, 2007, CMOS 0.35

(e)

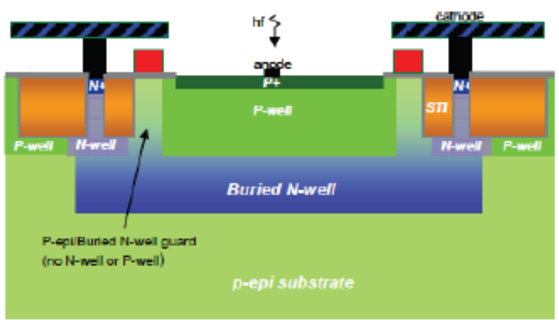


Cova, 1981; Ghioni, 1988, Lacaita, 1989; custom

(f)



Finkelstein , 2006,CMOS 0.18; Hsu, 2009, CMOS 0.18;
Niclass, 2007, CMOS 0.13; Gersback, 2008, CMOS 0.13,
Arbat, 2008, CMOS 0.13

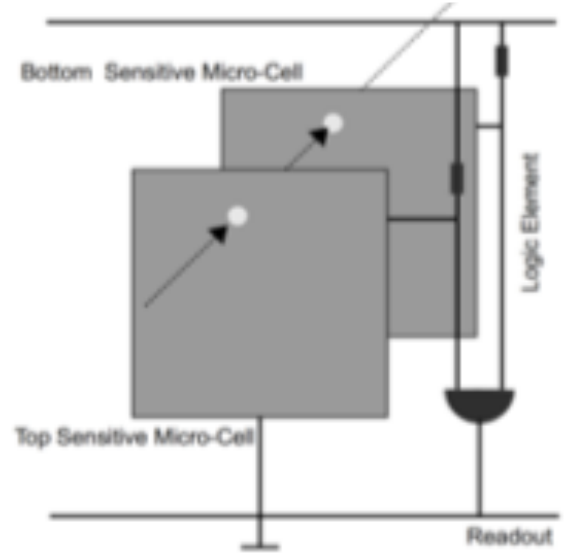


Richardson, 2009, CMOS 0.13, Webster, 2012, CMOS 0.09

G.-F. Dalla Betta et al., "Avalanche Photodiodes in Submicron CMOS Technologies for High-Sensitivity Imaging", in "Advances in Photodiodes", Intech House, 2011

SPAD based tracking sensors

V. Saveliev, SILC Meeting



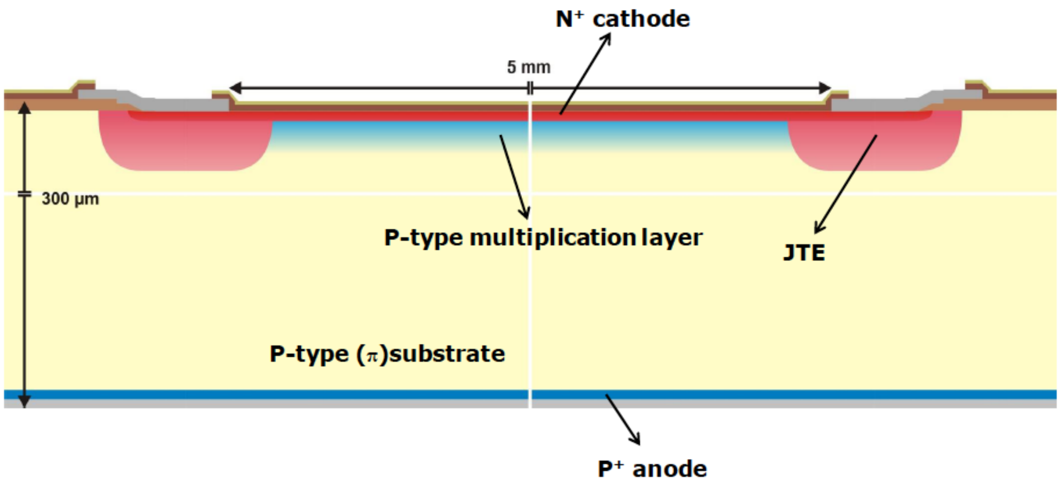
- CMOS SPAD cells for charged particle detection
- Coincidence between vertically aligned cell pairs can dramatically reduce dark count rate (DCR)
- Very thin sensors are possible
- Intrinsically digital output → Simpler electronics
- On-chip electronics → reduced system complexity and power consumption

Questions to answer:

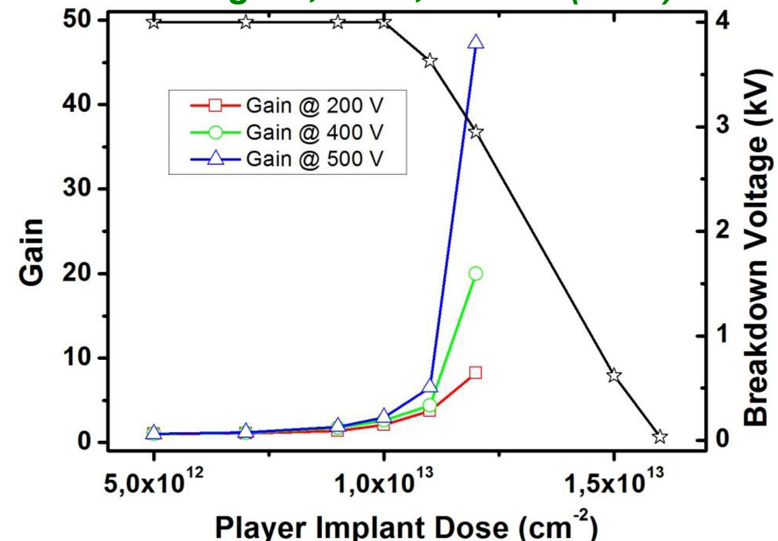
- Sensitivity: with very thin (~1μm) active volume, will SPADs detect all particles?
- Fill factor: is it possible to achieve a low geometrical inefficiency ?
- Noise: is DCR low enough (with standard CMOS process) ?
  What about optical cross-talk ?
- Radiation hardness ?

A. Dieguez, VERTEX 2013
P.S. Marrocchesi, et al., INFN CSN5 APIX2 project

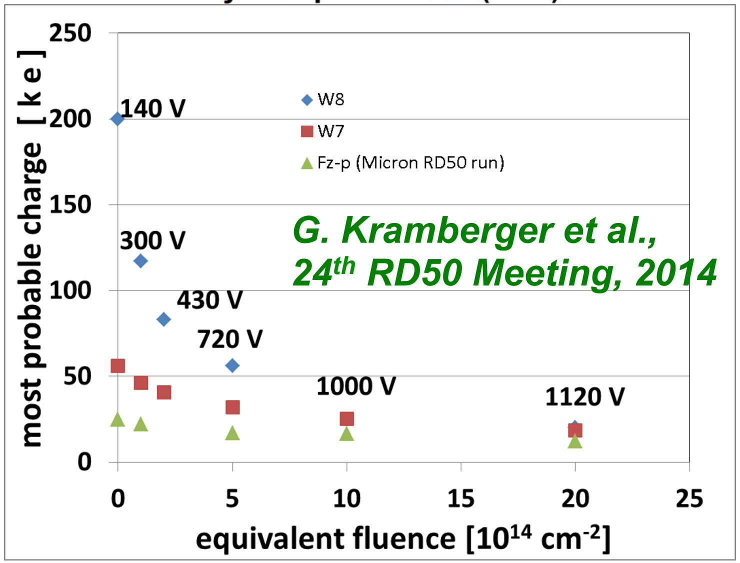
Low Gain Avalanche Detector (LGAD)



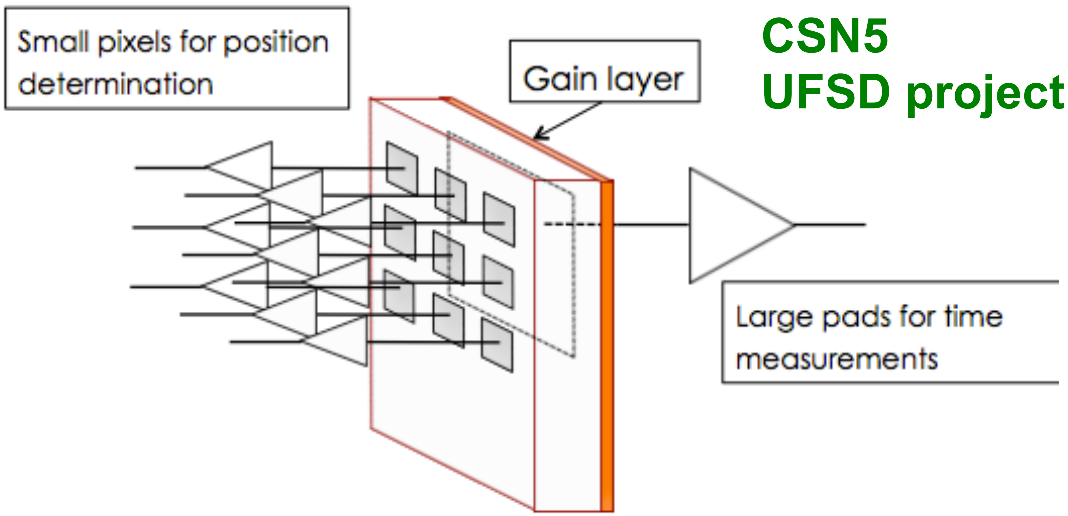
G. Pellegrini, et al., HSTD9 (2013)



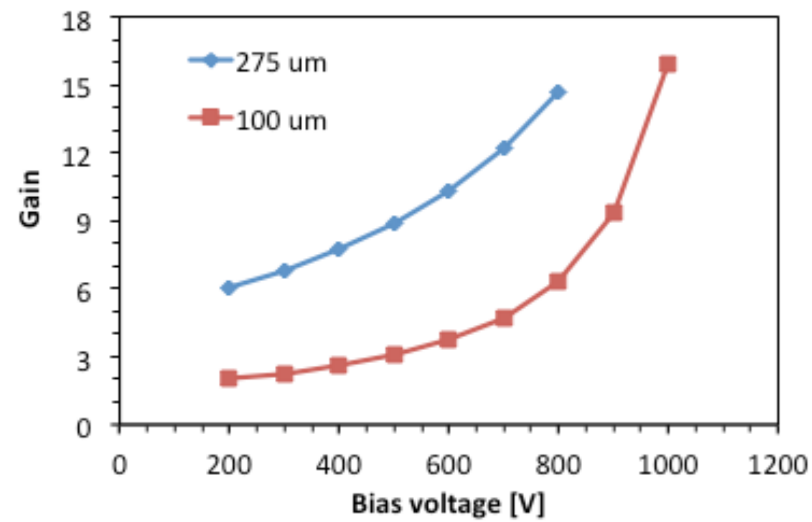
- Revisiting APDs for ionizing particles
- Gain vs breakdown voltage trade-off
- High sensitivity to the implant dose of the p-type multiplication layer
- JTE to prevent from edge breakdown
- Promising results, but gain vanishes with radiation …



LGAD Pixels

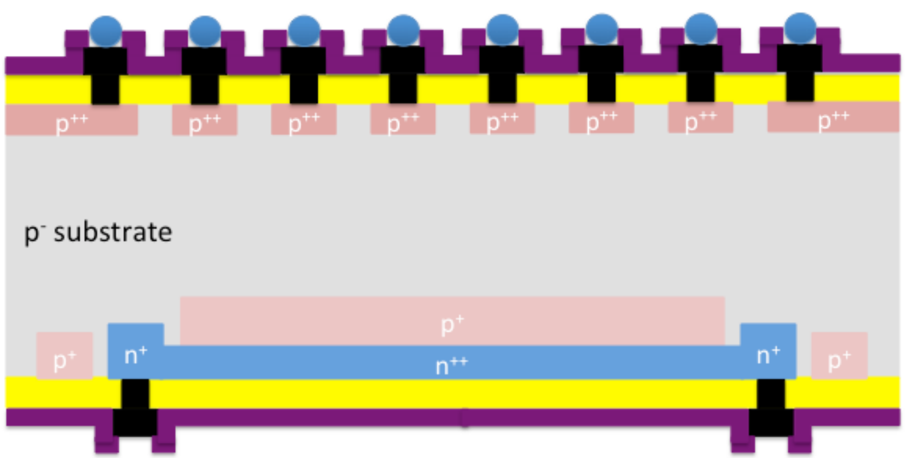


CSN5 UFSD project

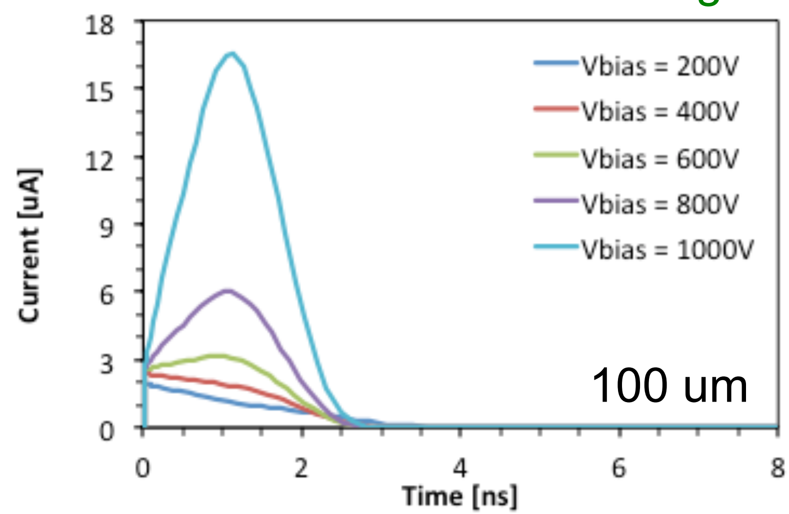


Aiming at 20ps time resolution with thin sensors …

G.-F. Dalla Betta et al. RESMDD 2014

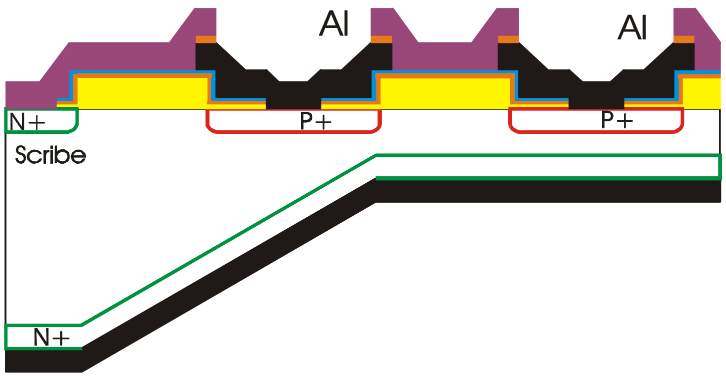


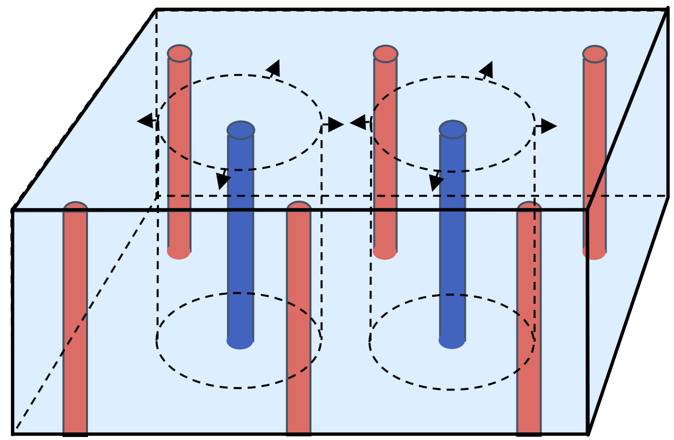
More on talk from N. Cartiglia

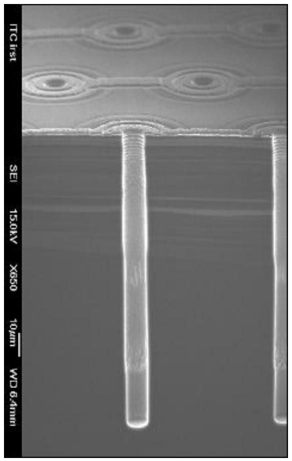


MEMS radiation sensors

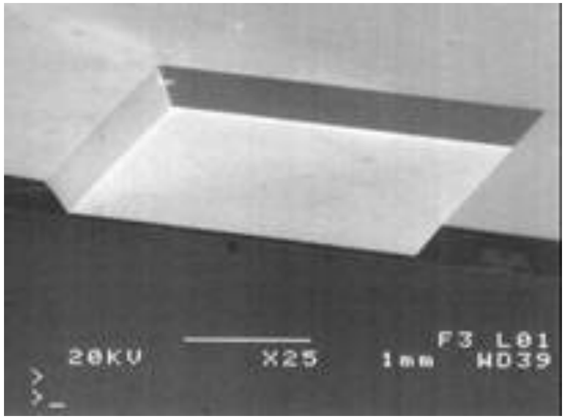
Use Si bulk etching to exploit third dimension in silicon

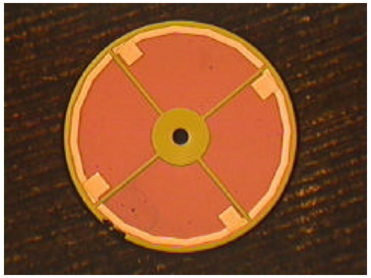




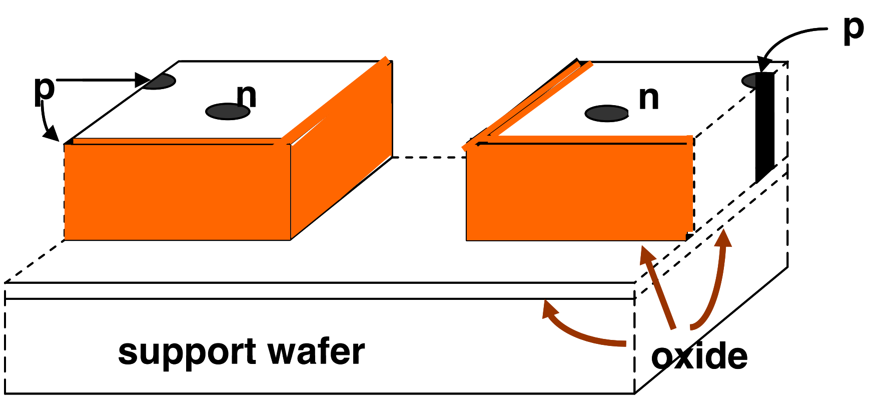


Thinned detectors



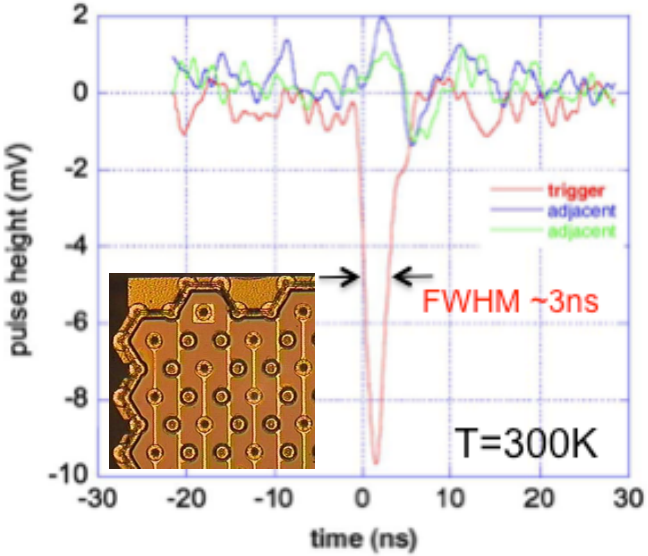


3D and active edge detectors

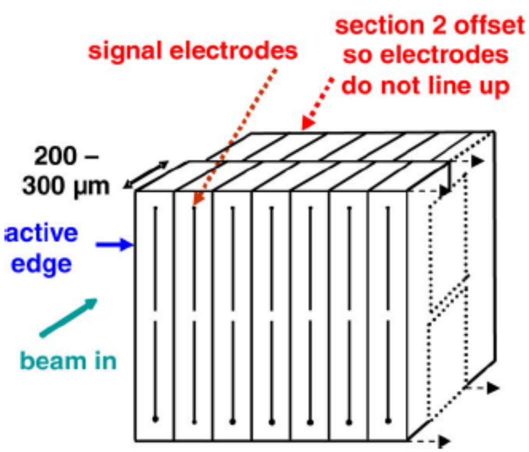


Speed with 3D

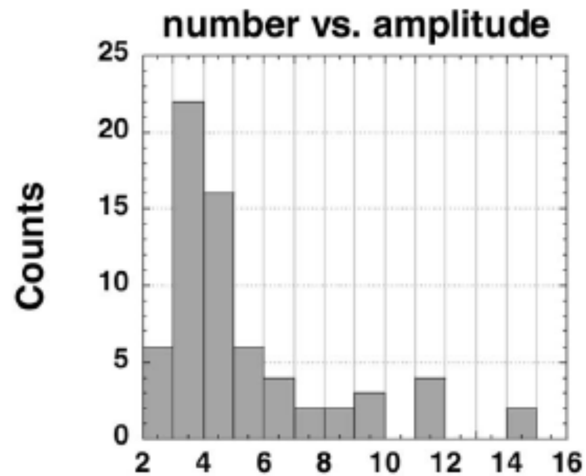
So far tested with hex-cell 3D's (L=50μm) & fast current amplifier

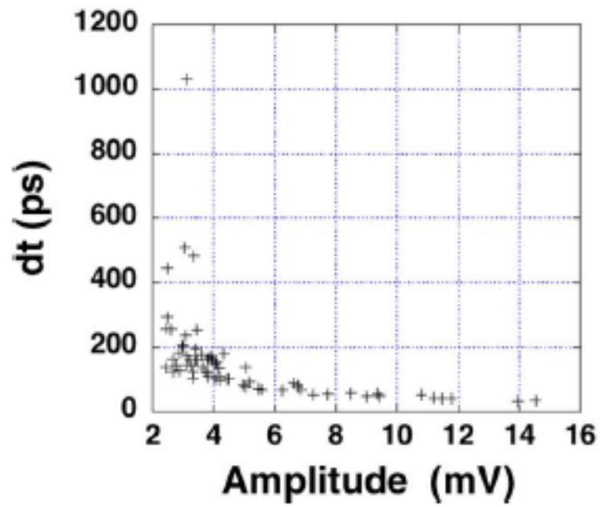


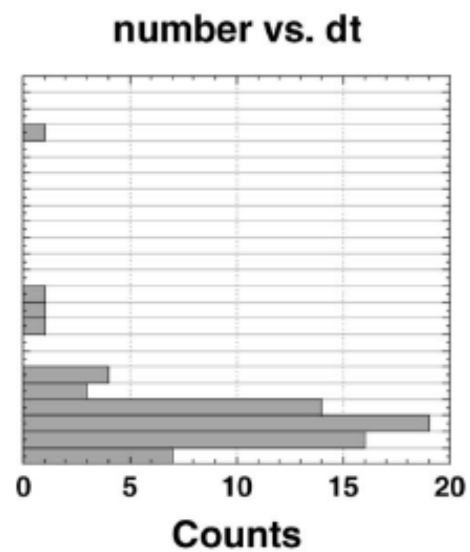
Best choice: trenched detectors



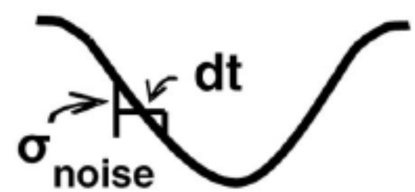
S. Parker et al. IEEE TNS 58(2) (2011) 404







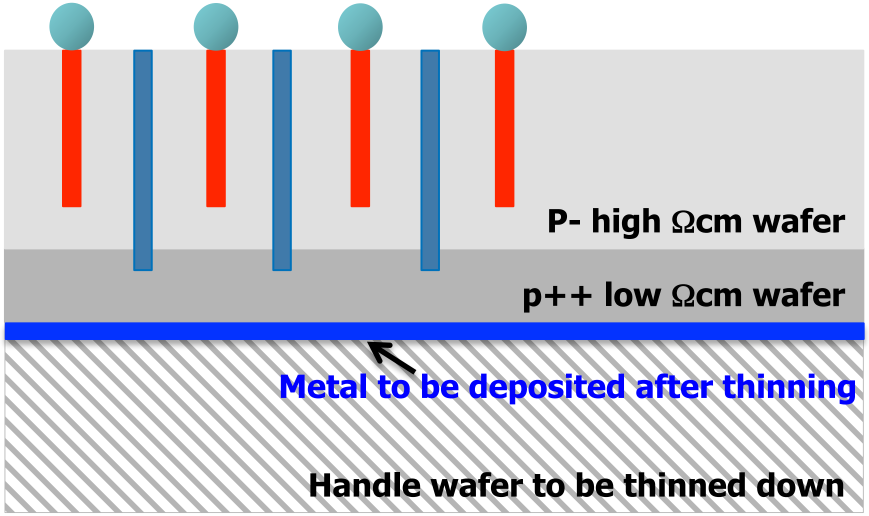
- Off-line analysis of recorded waveforms
- Timing resolution from 177 ps to 31ps
- Limited by front-end noise

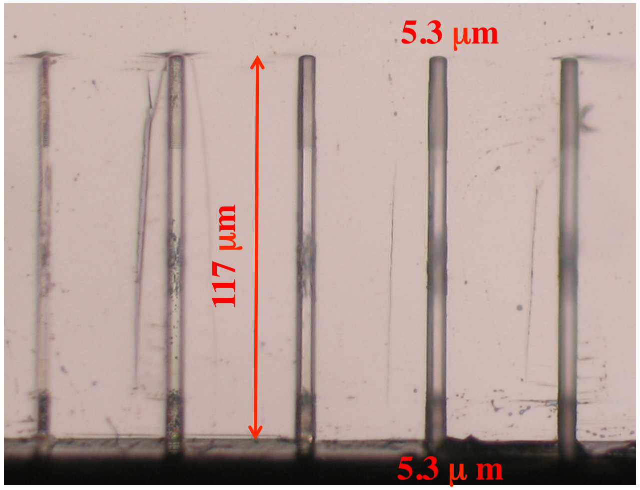


New "down scaled" 3D pixels for HL-LHC

Double-sided process not favoured for thin sensors, especially on 6" wafers

G.-F. Dalla Betta et al., Pisa Meeting 2015

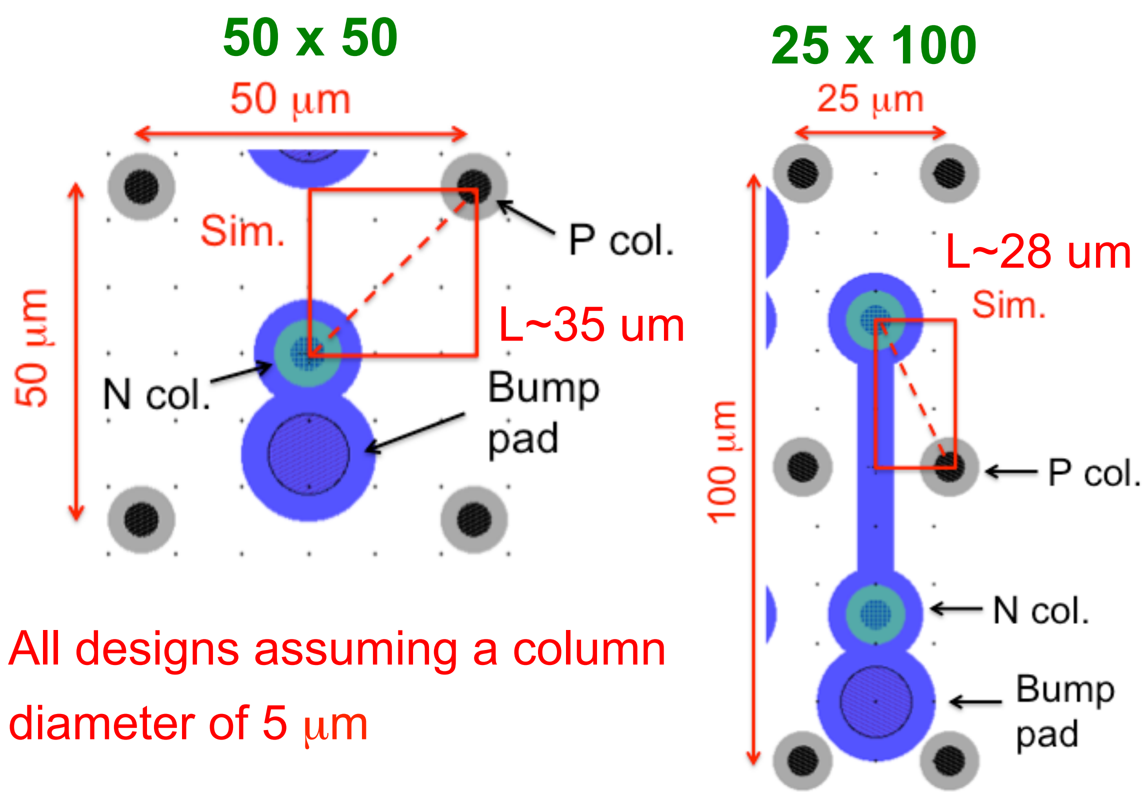




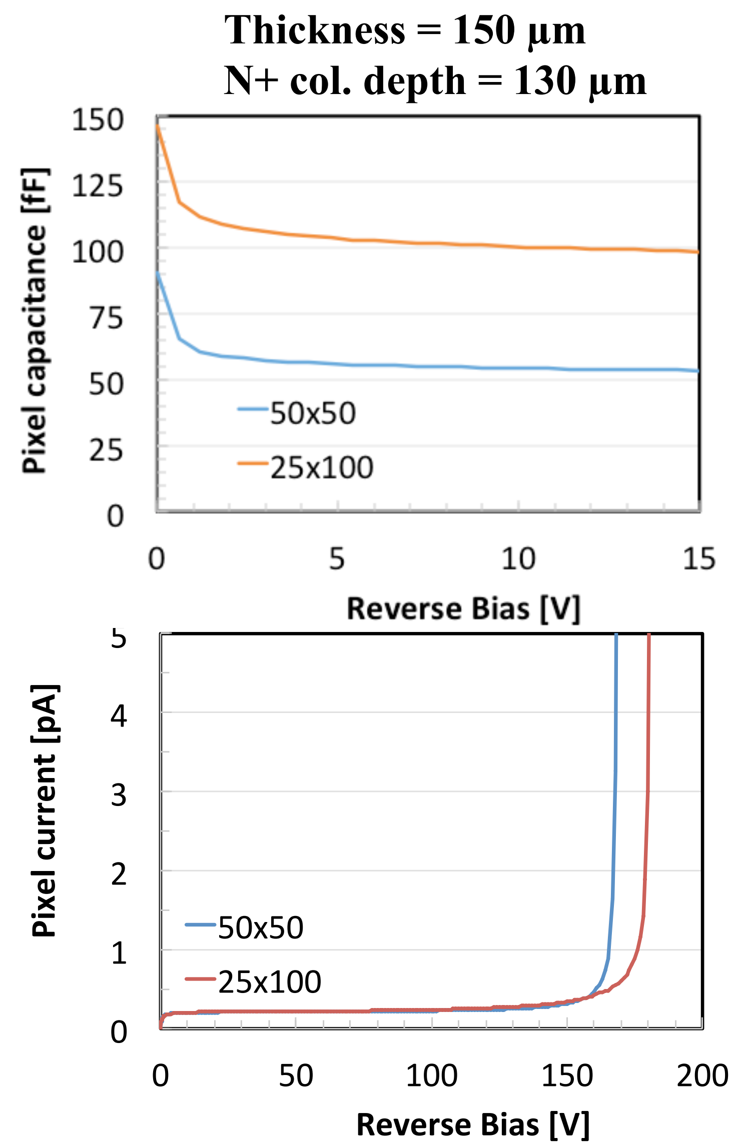
- Single-sided process with support wafer
- Ohmic columns/trenches depth > active layer depth (for bias)
- Junction columns depth < active layer depth (for high V_{bd})
- Reduction of hole diameters to ~5 um
- Holes (at least partially) filled with poly-Si

CSN1 RD_FASE2 project

New 3D pixels: design and simulations

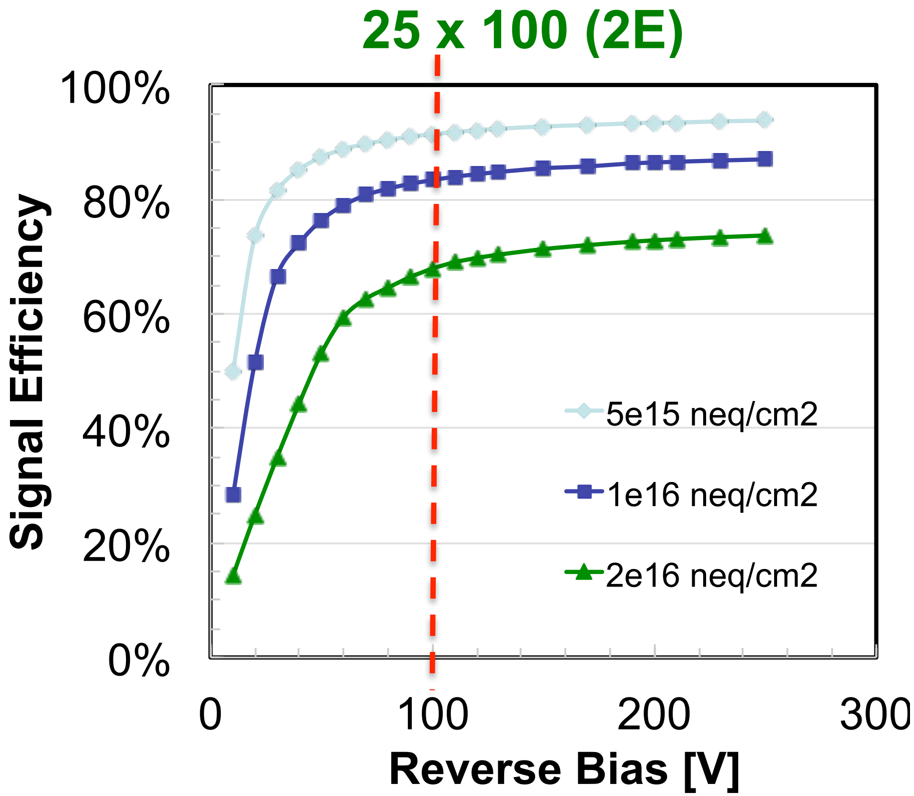


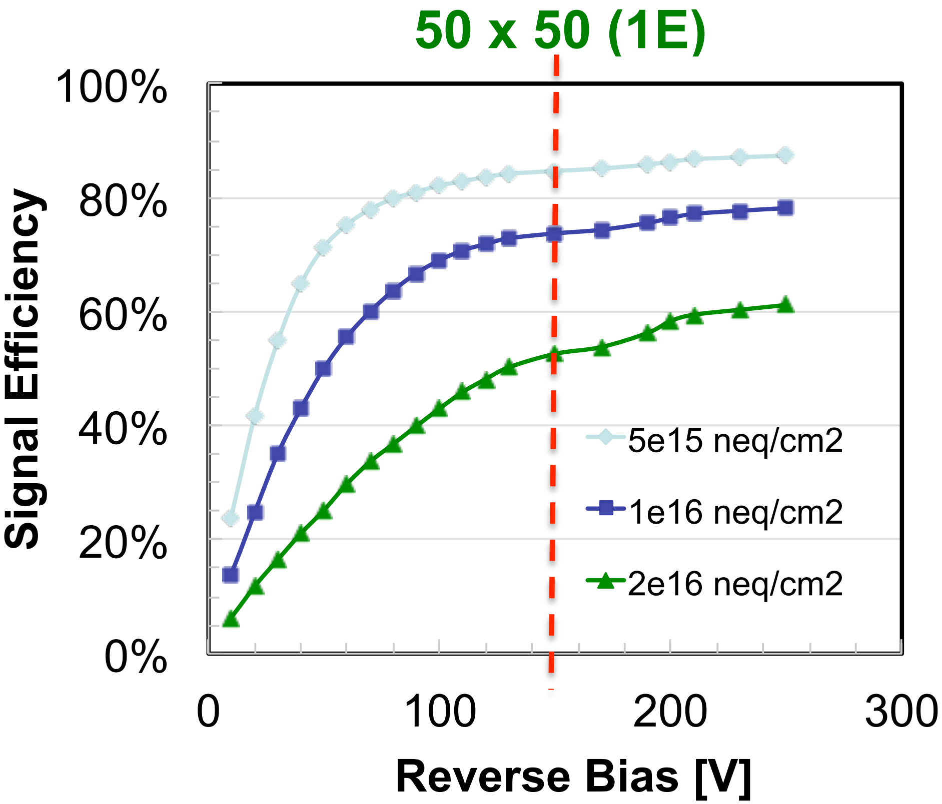
All designs assuming a column diameter of 5 µm



- 50x50 design safe, 25x100 is difficult … too little clearances (new ideas for bump pad to be tested)
- Capacitance compatible with RD53 specs
- Initial breakdown voltage high enough

Simulated signal efficiency (preliminary)

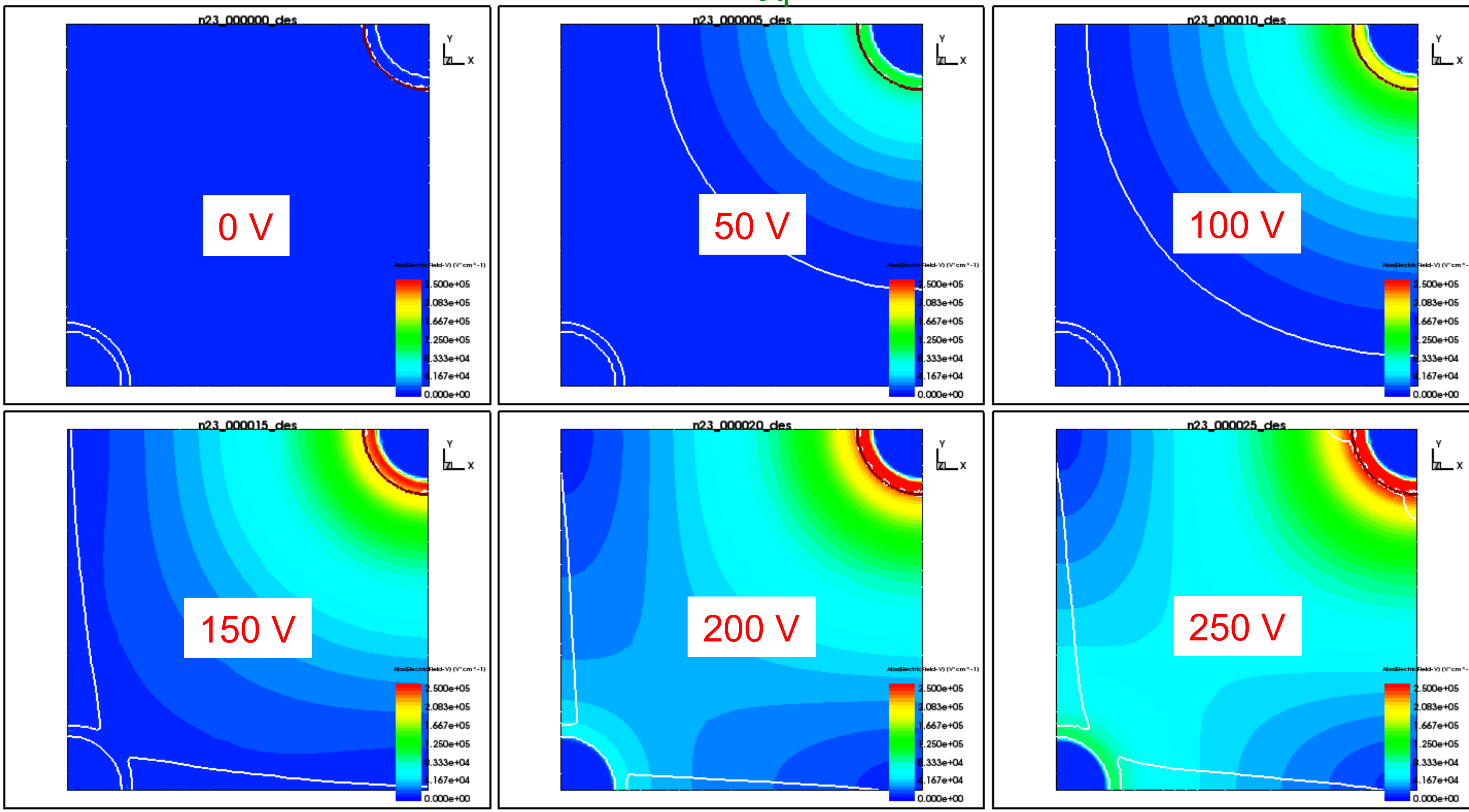




- New 3-trap level "Perugia" model D. Passeri et al. (doi:10.1016/j.nima.2015.08.039)
- 1 μm thick (~2d) slice, with MIP vertical hits at many different points
- 20-ns integration of current signals → normalization to injected charge → average
- Higher Signal Efficiency at lower V_{bias} in 25x100 (2E), as expected due to smaller L

50x50: electric field 2d (preliminary)

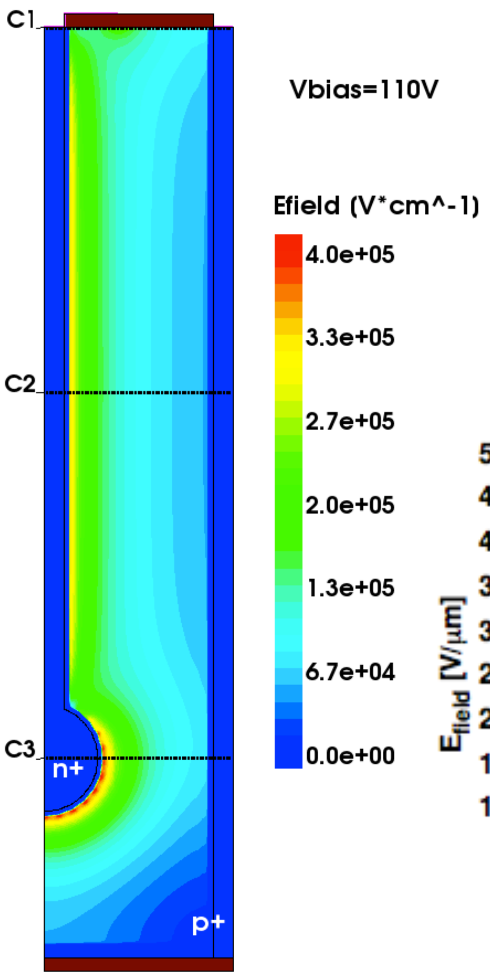
$2\times10^{16}\ n_{eq}/cm^2$

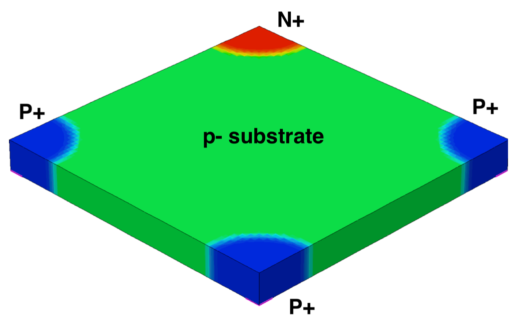


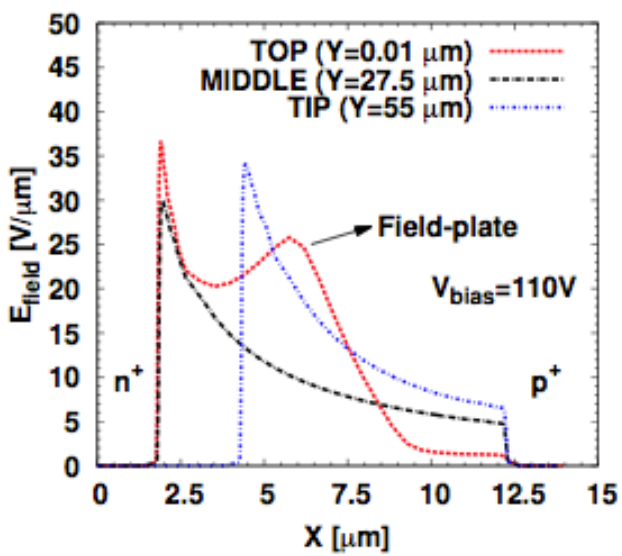
Charge multiplication by design in 3D sensors

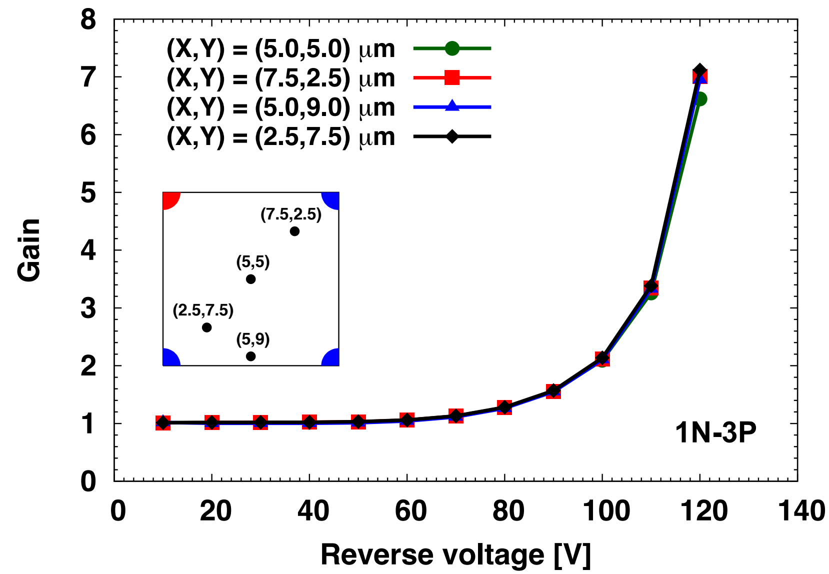
Exploiting high fields in thin 3D structures with small inter-electrode spacing

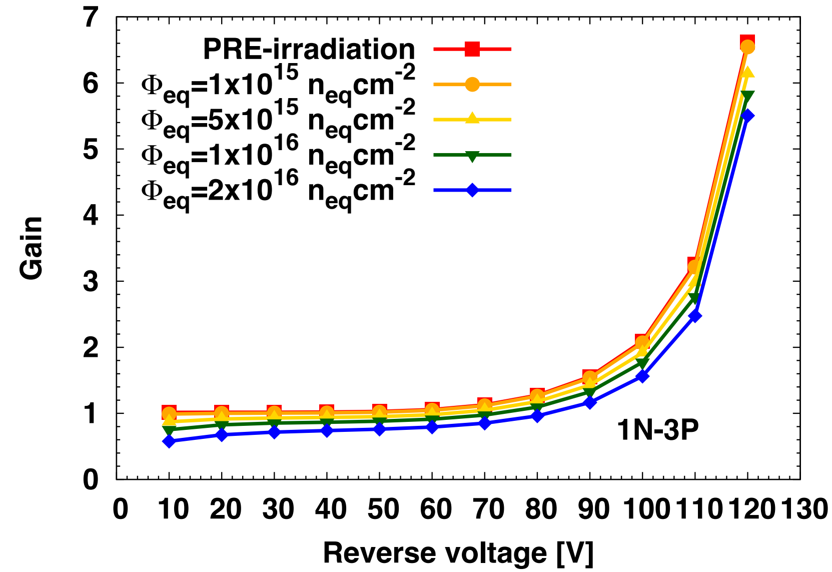
M. Povoli et. al., To be published



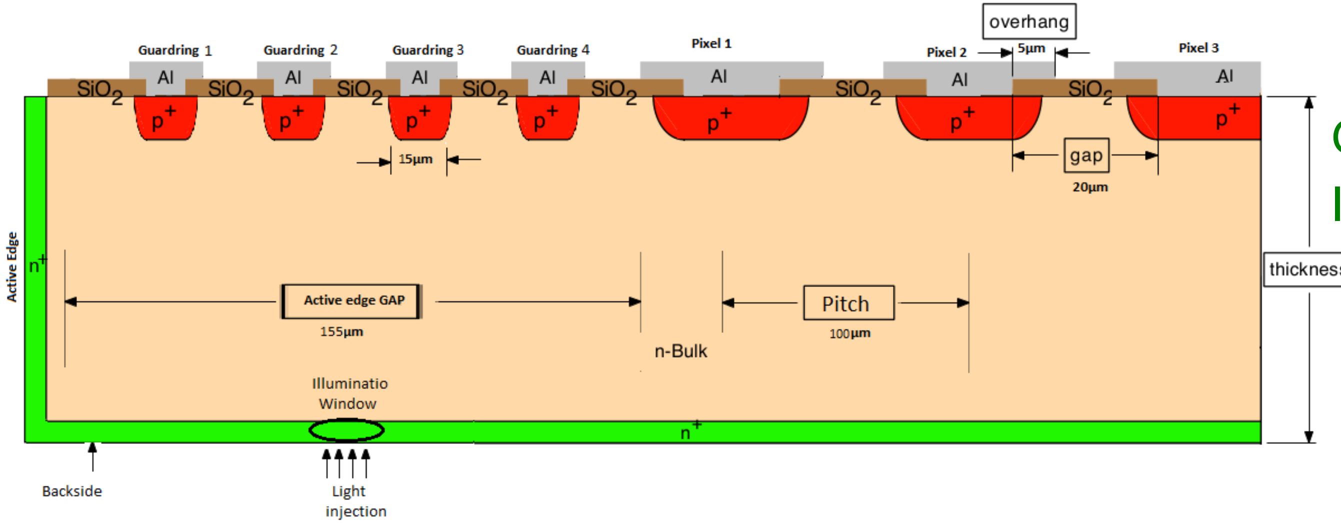








Planar active edge sensors



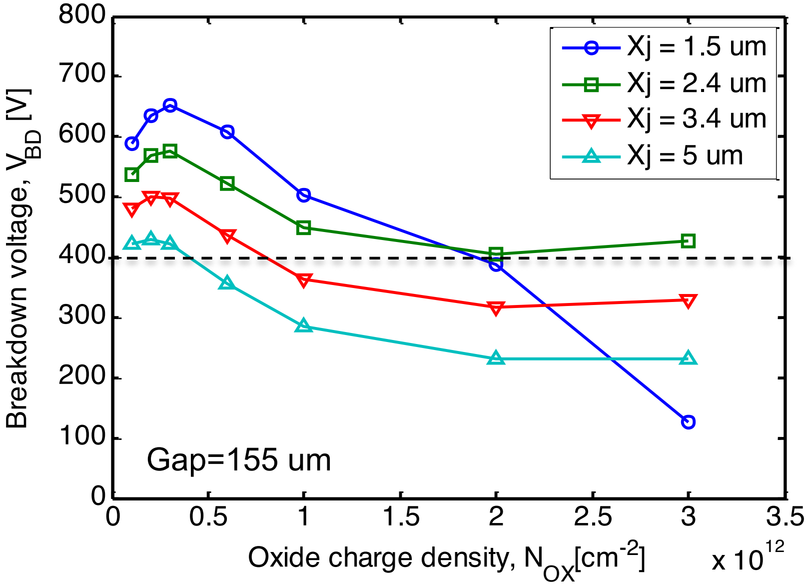
G.-F. Dalla Betta et al., IEEE NSS 2014

CSN5 PixFEL project

- Technological complexity increases as sensor thickness is increased (e.g., for efficiency in X-ray detection)
- Design trade-off: minimization of dead area vs high voltage capability

→ For radiation hardness in HEP

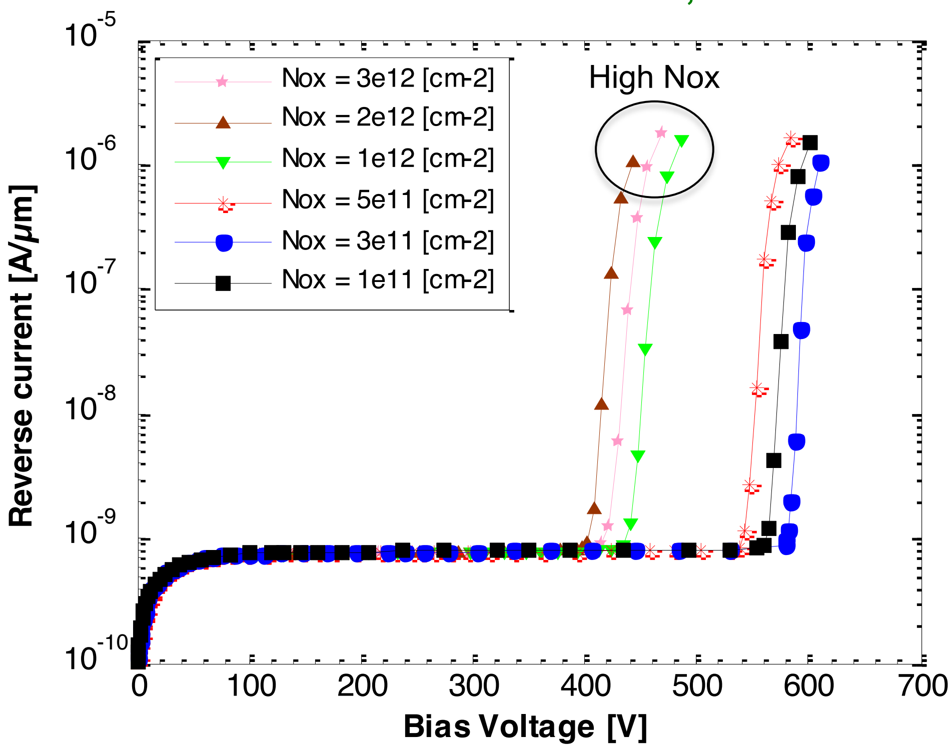
→ For plasma effects in FELs

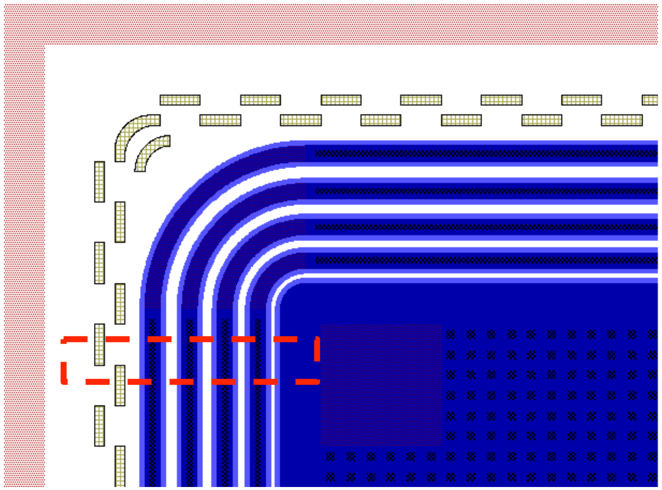


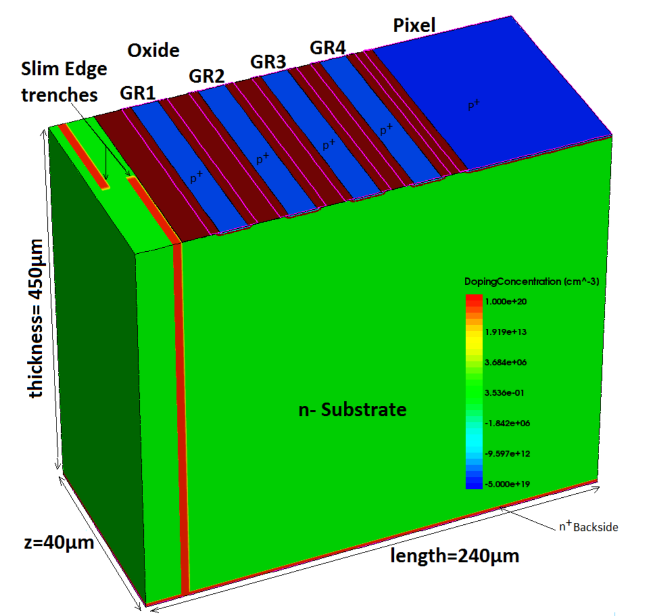
Planar slim edge sensors

- If trench is "dashed", there's no need to use a support wafer and the sensor back-side can be optimized for X-ray entrance window
- Will it work at high voltage ?

G.-F. Dalla Betta et al., Pisa Meeting 2015







Conclusions

• HV/HR CMOS sensors are emerging as a possible alternative to hybrid sensors in many applications.

→ R&D profits from the rapid progress in micro electronics

→ Still wide room for improving the sensor behavior

• For the most demanding performance (e.g., HL-LHC inner-most tracking layers) advanced hybrid pixels are still favored and can further be improved for:

→ Very high speed

→ Extreme radiation tolerance

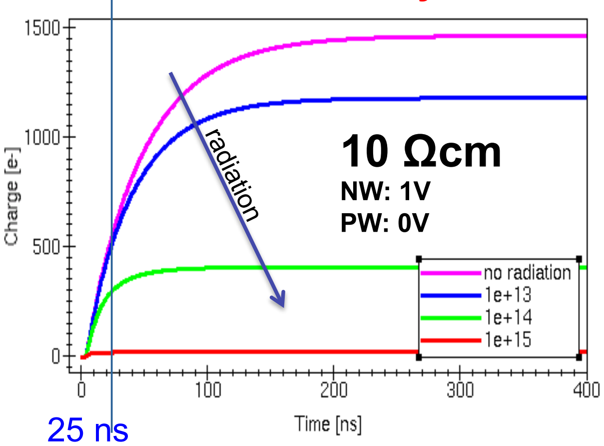
→ Special features (e.g., very slim edges)

Back-Up Slides

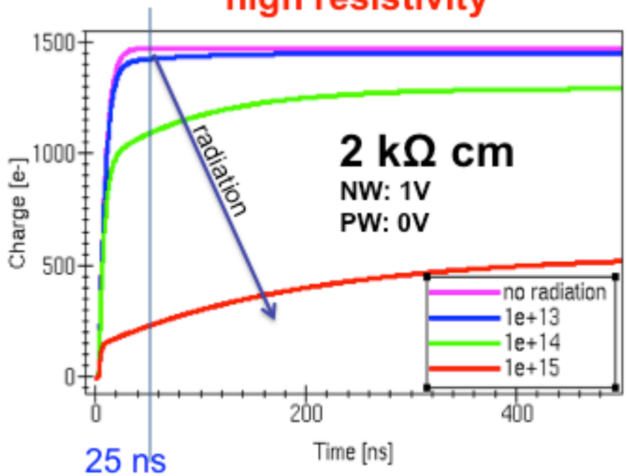
How to improve CMOS sensors ?

N. Wermes, TALENT ITN Final Conference (CERN 2015)

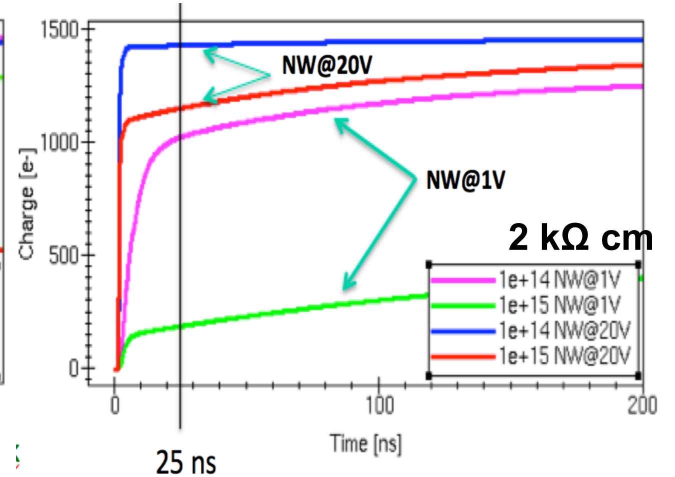
low resistivity



high resistivity



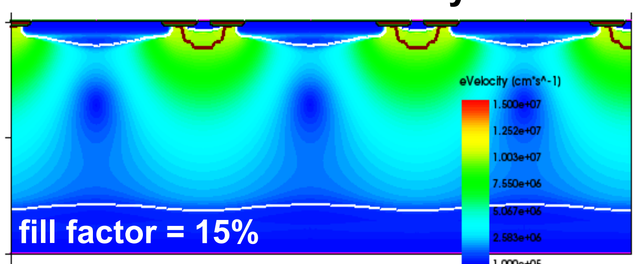
HR plus (high) voltage

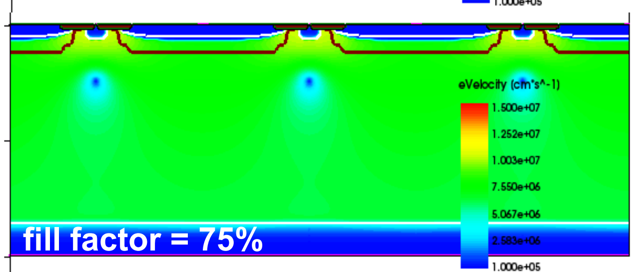


Substrate: 10 Ωcm – 2kΩ cm
Nwell: 1V – 20 V
Pwell: 0V

Simulations from Tomasz Hemperek

Electron Velocity





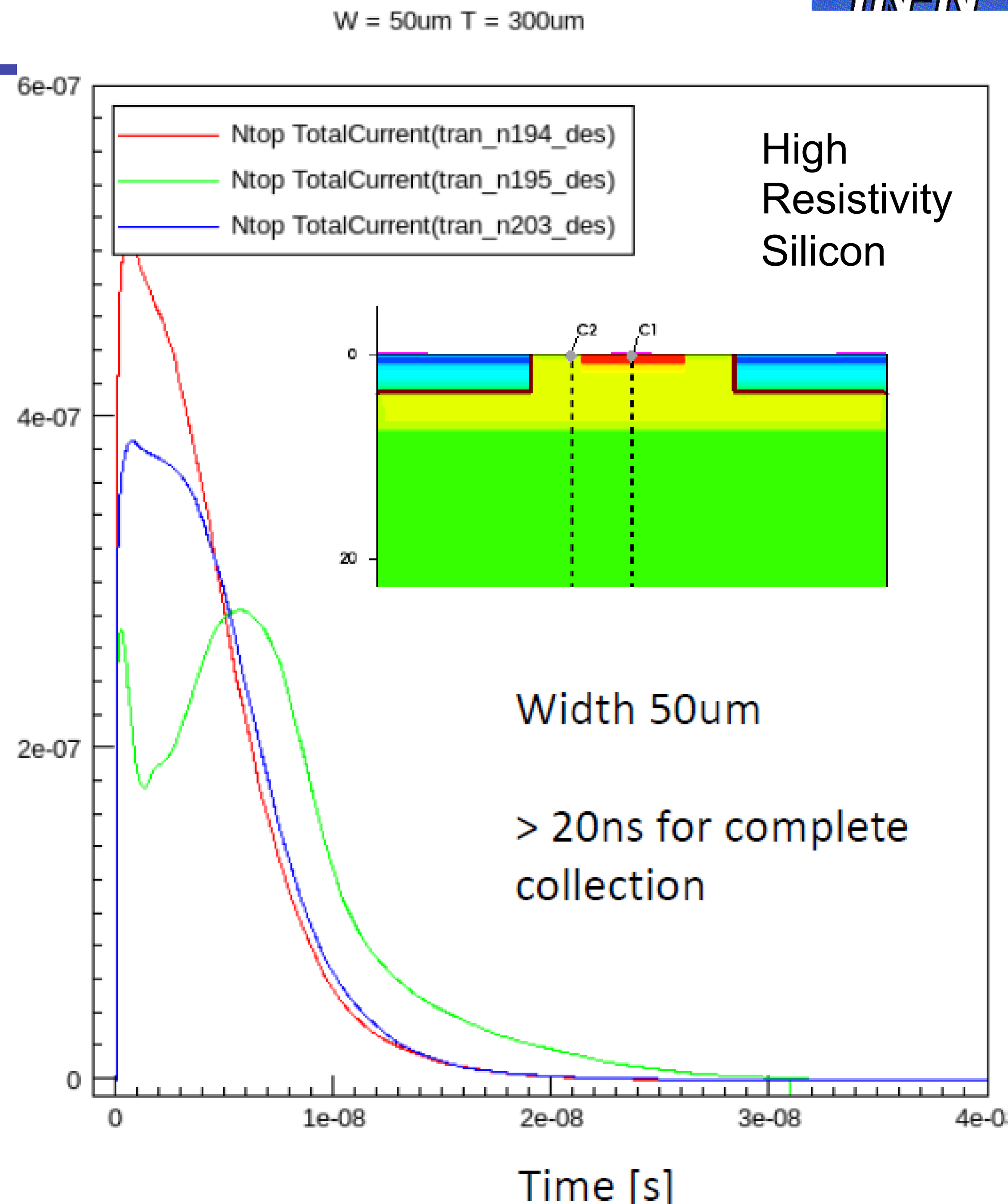
NW: 20V
PW: 0V
Substrate: 2kΩ cm
Dose: 10^{15} n_{eq}/cm^2

Resistivity + Voltage + Fill factor ⇨ Increased speed, efficiency, radiation hardness

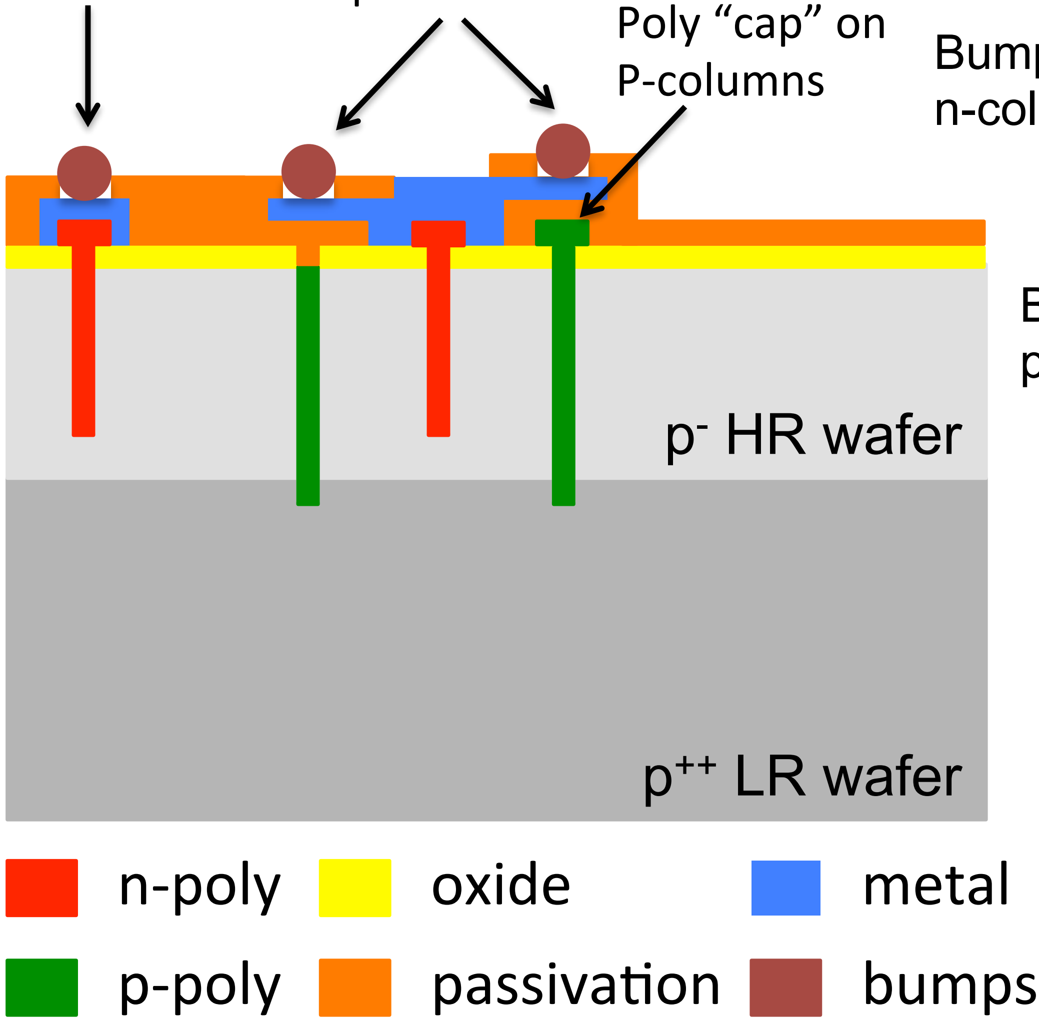
G.-F. Dalla Betta

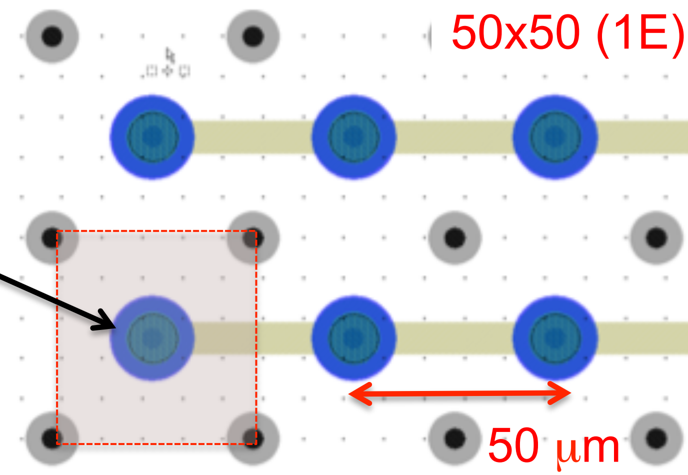
SEED Project

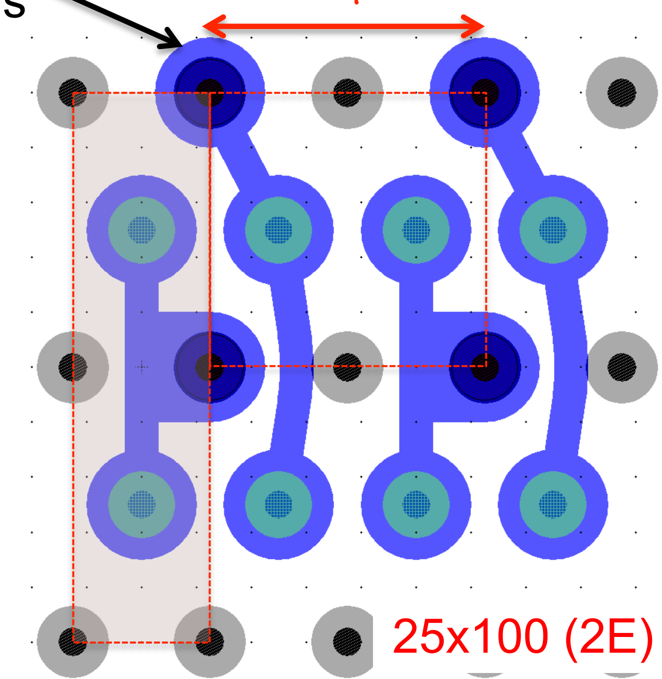
- INFN-LFoundry partnership
- Monolithic HR-CMOS pixels (fully depleted)
- CMOS layers are not modified (this sets some limits to operation voltage)
- Bulk thickness/resistivity and back-side processing can be chosen
- First chip being designed, submission by early 2016



Bumps on columns



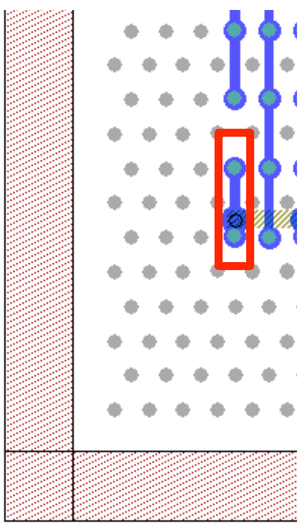


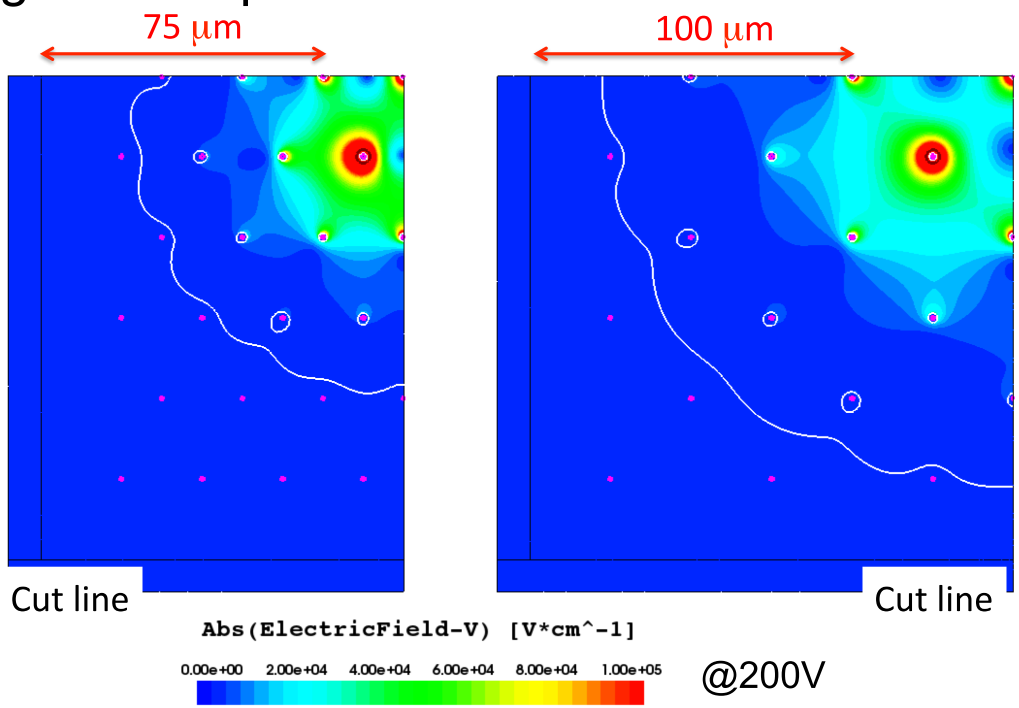


Slim edges

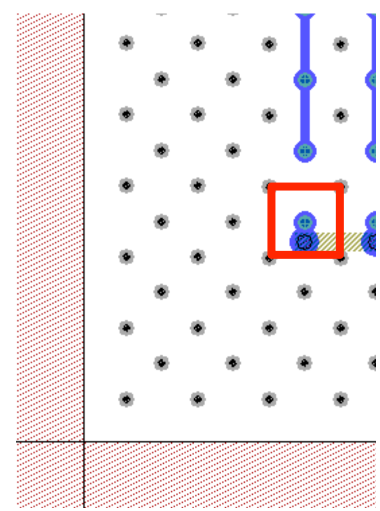
- Slim edge concept based on multiple ohmic columns termination developed for IBL (~200 μm) M. Povoli et al., JINST 7 (2012) C01015
- Here it can be made slimmer by reduced inter-electrode spacing (safely 75 - 100 μm, more aggressively down to ~50 μm)
- 3D guard rings also implemented with similar dead area

25x100 (2E)

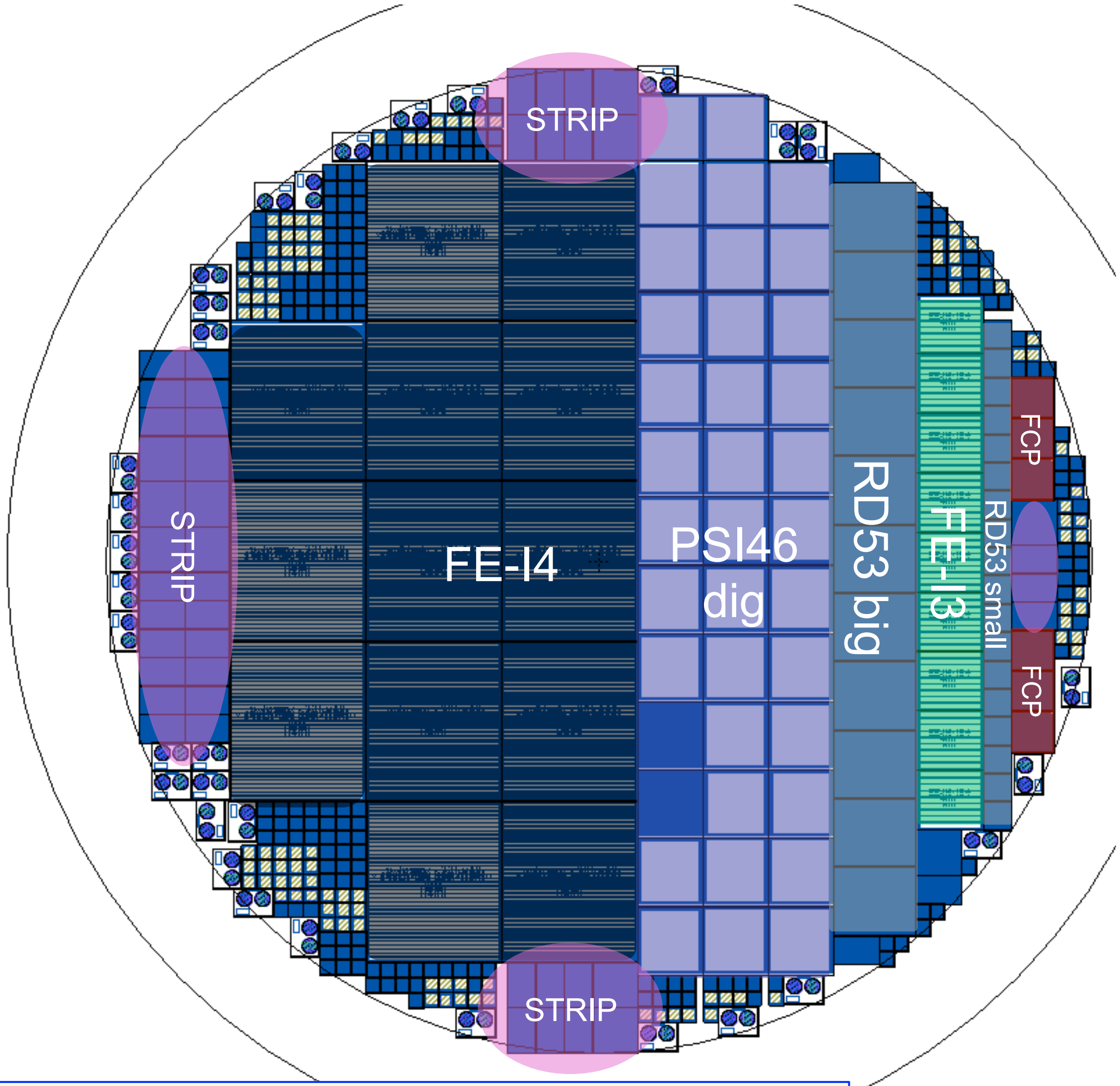




50x50 (1E)



3D Pixel Wafer Layout



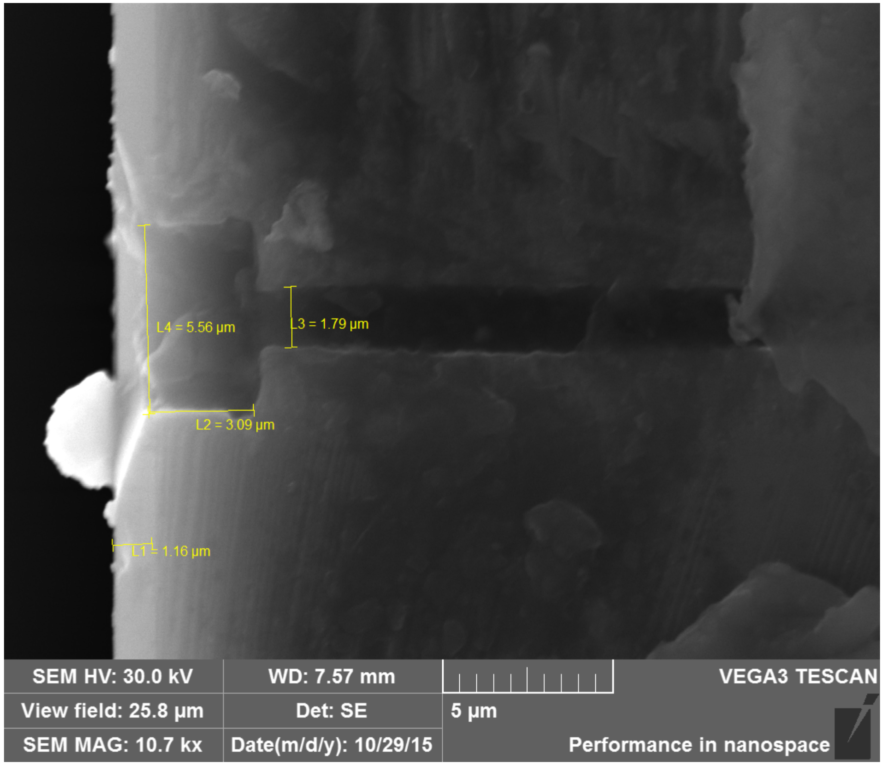
+ Test structures (strip, diodes, etc)

Many different pixel geometries and pitch variations:

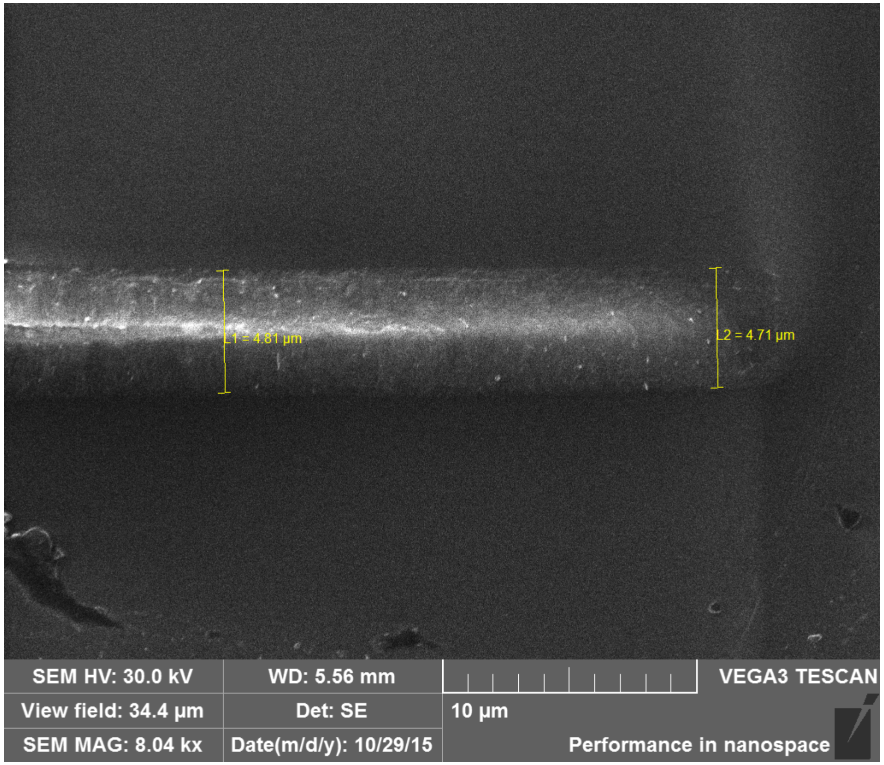
- FE-I4
  - 50 x 250 (2E) std
  - 50 x 50 (1E)
  - 25 x 100 (1E and 2E)
  - 25 x 500 (1E)
- FE-I3
  - 50 x 50 (1E)
  - 25 x 100 (1E and 2E)
- PSI46dig
  - 100 x 150 (2E and 3E) std
  - 50 x 50 (1E and 2E)
  - 50 x 100, 100 x 100 (2E + 4E)
  - 50 x 100, 100 X 150 (2E + 6E)
  - 25 x 100 (1E and 2E)
- FCP
  - 30 x 100 (1E)
- RD53
  - 50 x 50 (1E)
  - 25 x 100 (1E)
  - 25 x 100 (2E)

New 3D fabrication at FBK

G.-F. Dalla Betta et al., IEEE NSS 2015



Column opening



Column end

New Trenched-3D pixels for speed