New needs and directions in microelectronics and ultra-fast electronics

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INFN -Sezione di Torino

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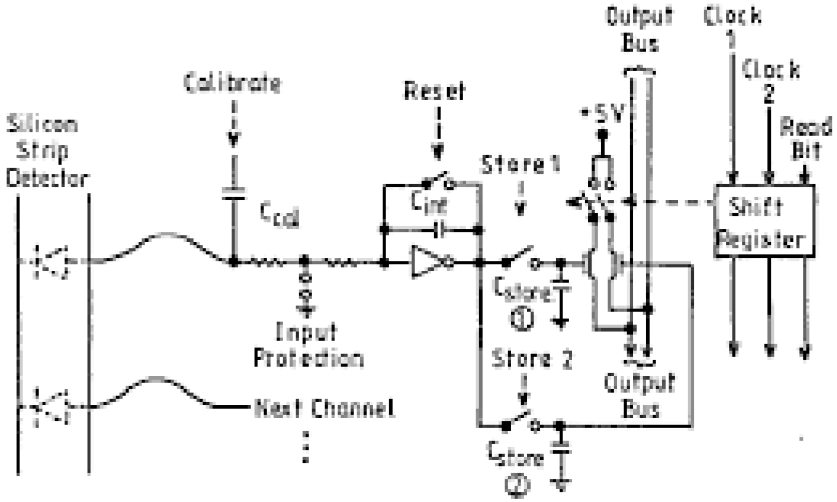
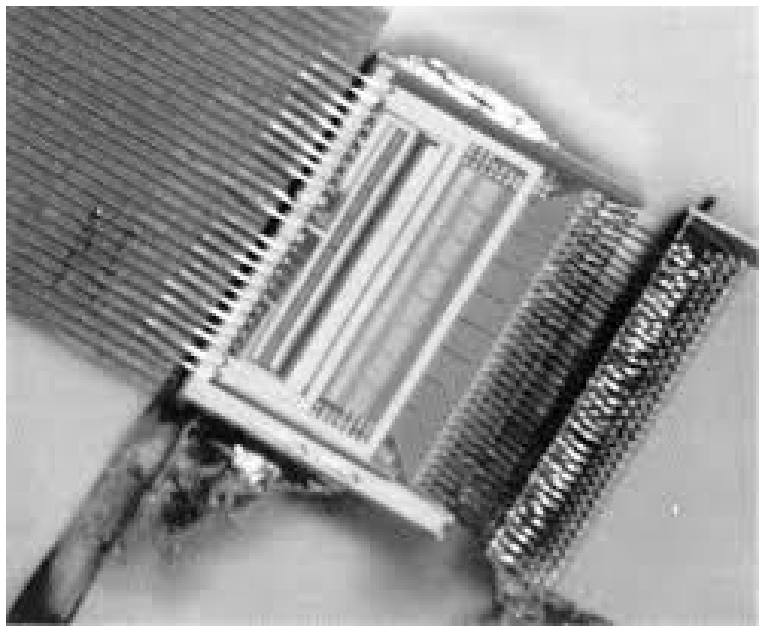
Agenda

1. Introduction
2. The industry: where it is, where it is going
3. Detector electronics: where it is, where it is going
4. Conclusions

Microelectronics for detectors: 30 years of history

- Systematic design of IC for radiation sensors started in 1984
- Strong boost from LEP and LHC
- ASICs are today an enabling technology in many domains:
  - ⋆ Colliders
  - ⋆ Astrophysics (both ground-based and space-born)
  - ⋆ XFEL facilities
  - ⋆ Medical instrumentations
  - ⋆ others...

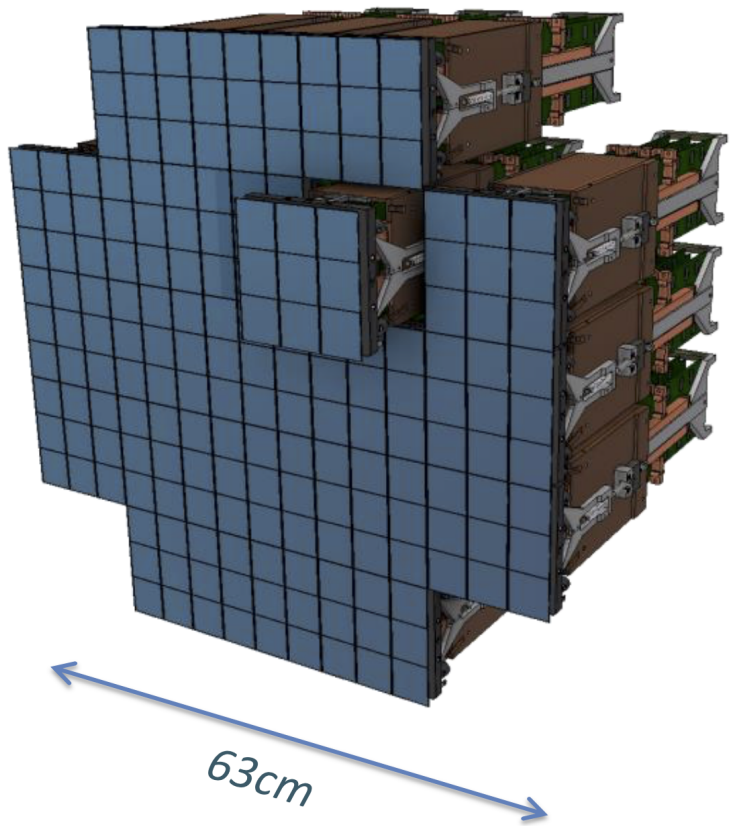




Not only HEP: LSST

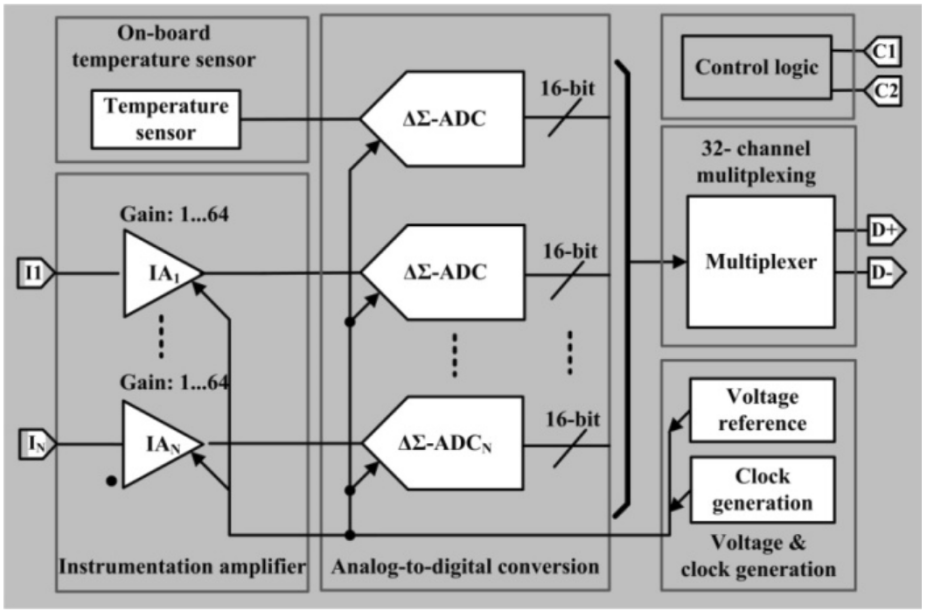
The Large Synoptic Survey Telescope

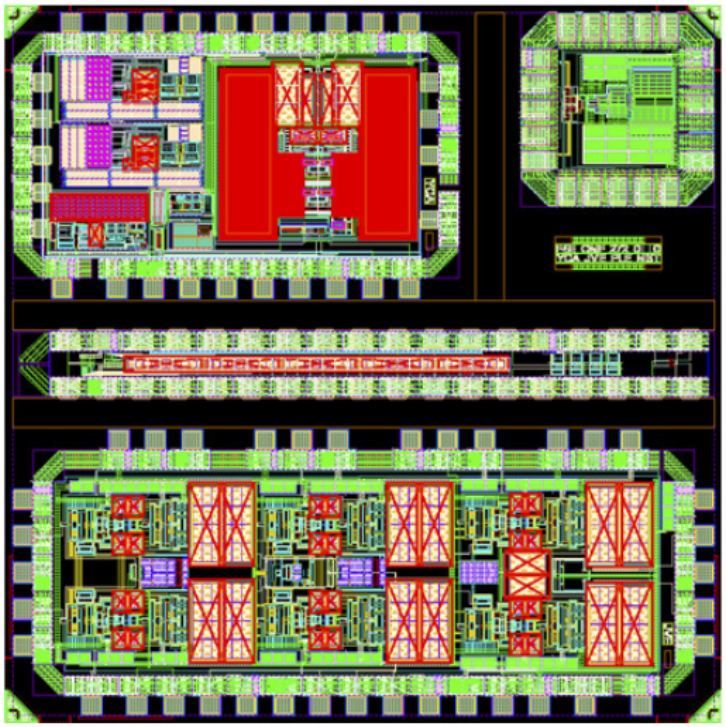
- 8-m class telescope
- Fast optical transient
- 800 images per night
- 1000 times the same sky region
- Dark matter mapping
- Dark energy
- Neo's
- Fast 3.2 Gpixel camera
- 4 k×4 k CDD operating at -100° C
- Two ASICs, one for CCD control and one for CDD readout



Not only HEP: fusion reactors

J. Verbeeck et al. Qualification method for a 1 MGy-tolerant front-end chip designed in 65 nm CMOS for the read-out of remotely operated sensors and actuators during maintenance in ITER





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Moore's law: the first 50 years

G. Moore Cramming more components onto integrated circuits
Electronics Magazine, vol. 8, n. 38, April 19, 1965

Statements for the 1965 paper:

- The future of integrated electronics is the future of electronics itself
- Integrated circuits will lead to such wonders as home computers, automatic controls for automobiles, and personal portable communication equipments
- The electronics wristwatch needs only a display to be feasible today
- But the biggest potential lies in the production of large systems

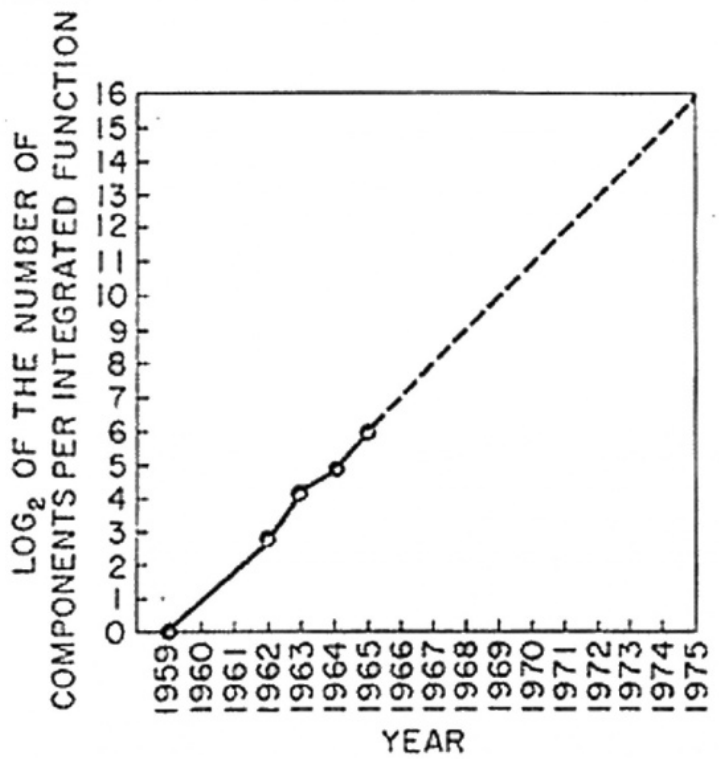
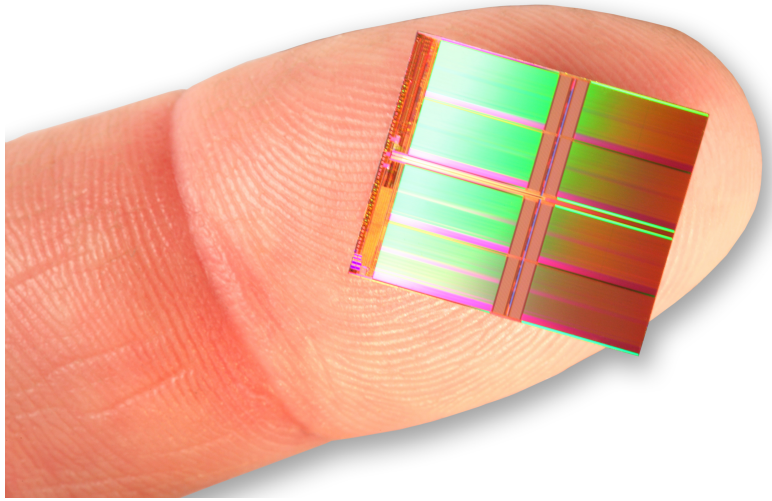


Fig. 2 Number of components per integrated function for minimum cost per component extrapolated vs time.

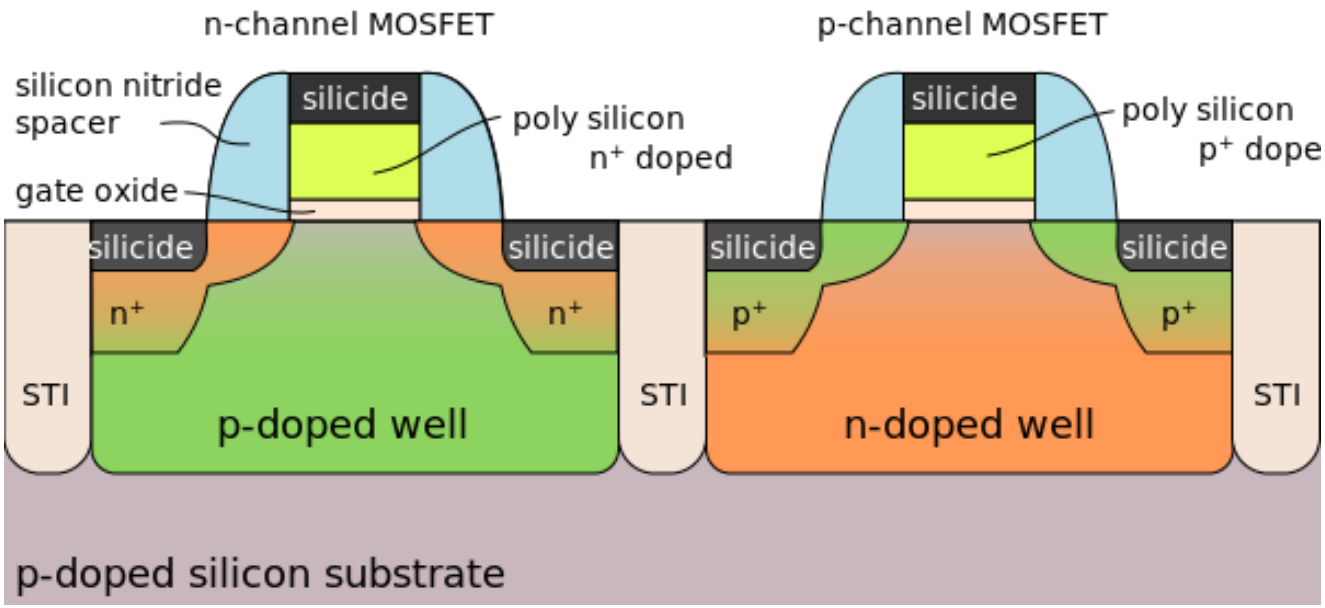
Moore's law at play

5 MB, 1956

16 GB, 2011



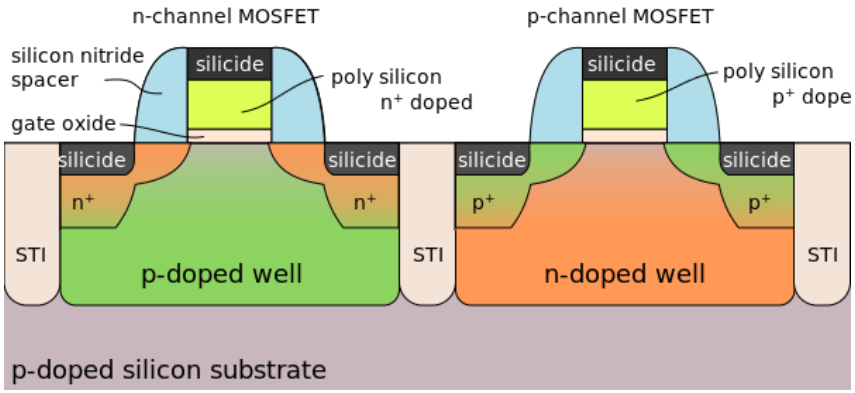
The electronics revolution workshorse

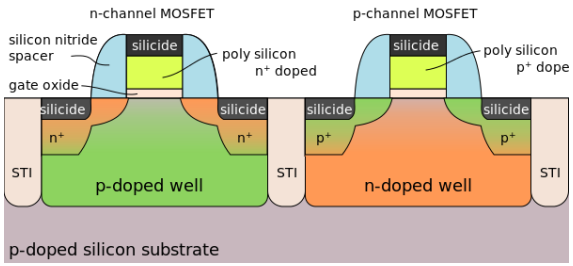


- Two complementary devices with almost equivalent performance
- Logic gates with minimal static power
- Good analog circuits

Dennard's scaling

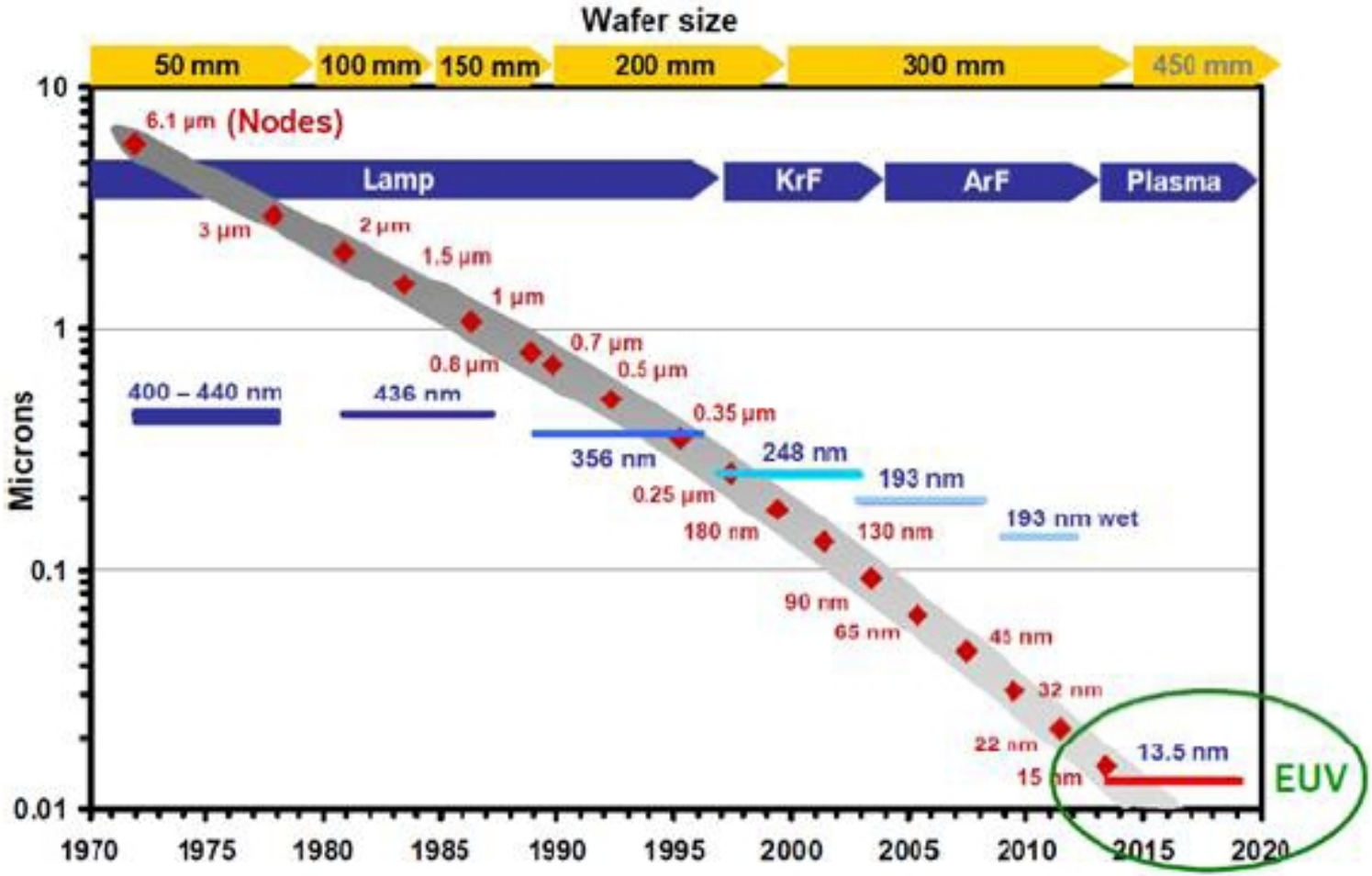
R. H. Dennard et al. Design of Ion-Implanted MOSFET's with Very Small Physical Dimensions
IEEE Journal of Solid-State Circuits, vol. SC-9, no. 5, Oct. 1974





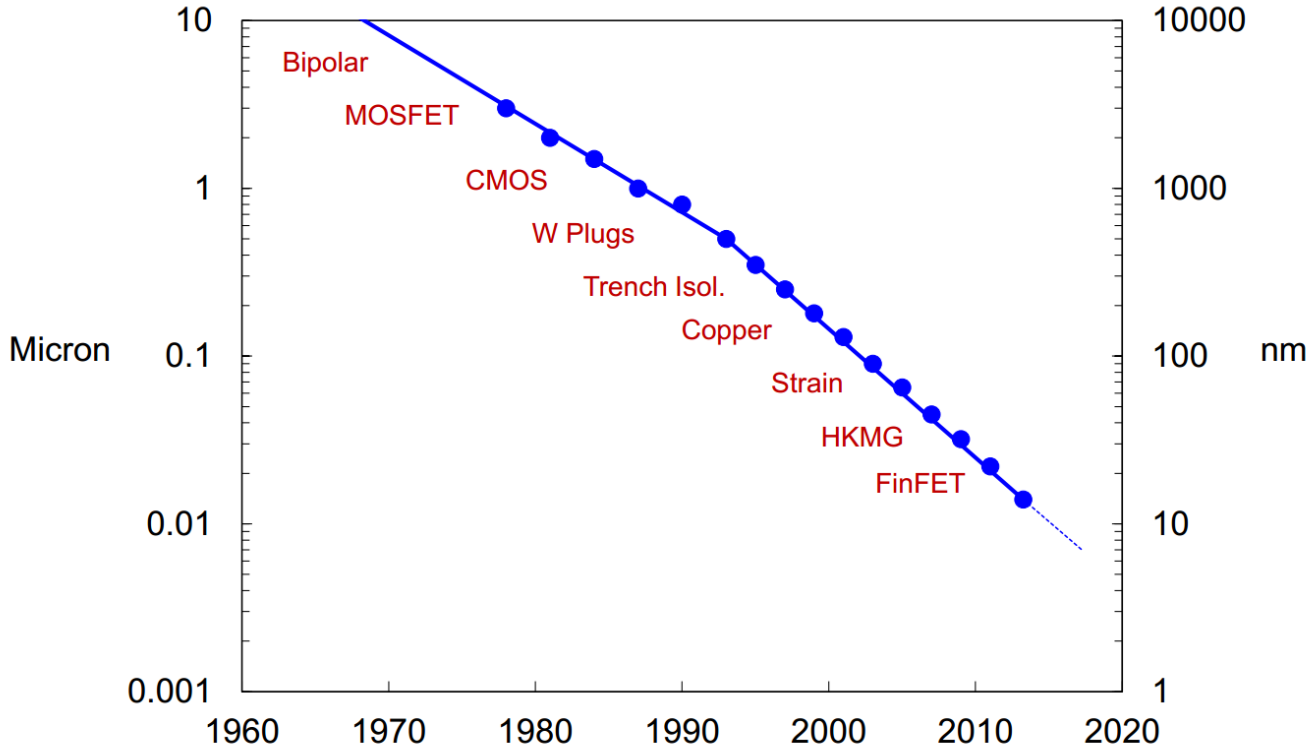
Device or Circuit Parameter	*Scaling Factor*
Device dimension t_{ox}, L, W	$1/k$
Doping concentration N_a	k
Voltage V	$1/k$
Current I	$1/k$
Capacitance eA/t	$1/k$
Delay time per circuit VC/I	$1/k$
Power dissipation per circuit VI	$1/k^2$
Power density VI/A	1

Fifty years of scaling



Innovations in IC technologies

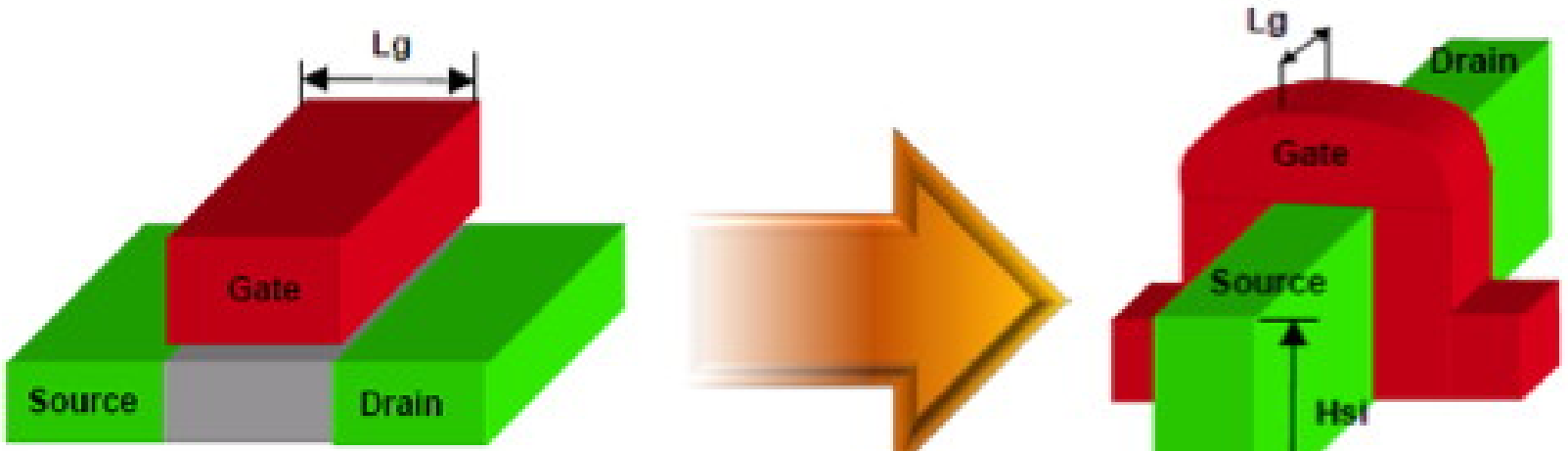
(EP1) Moore's Law Challenges Below 10nm: Technology, Design and Economic Implications



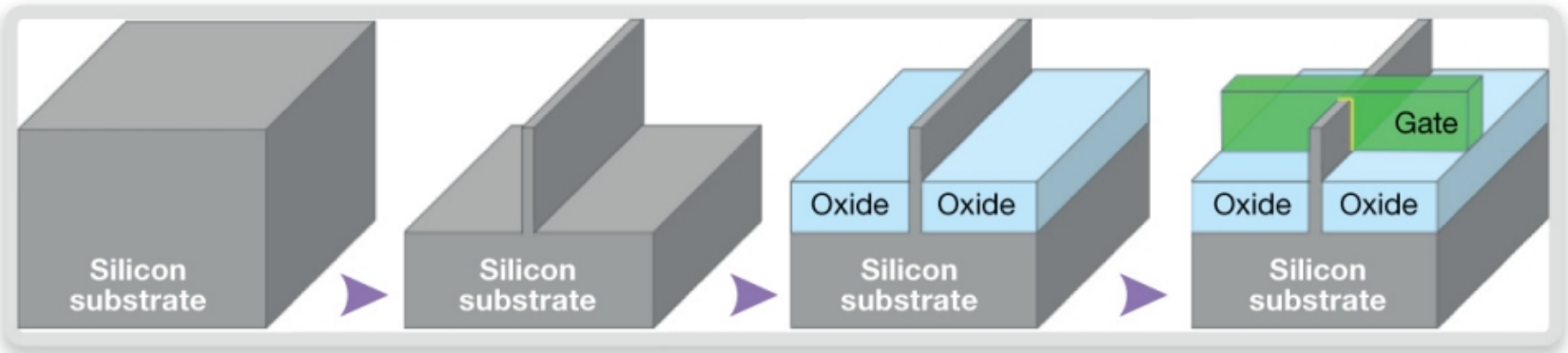
Process/device innovation has always been an indispensable part of scaling

Source: Intel

The FinFET

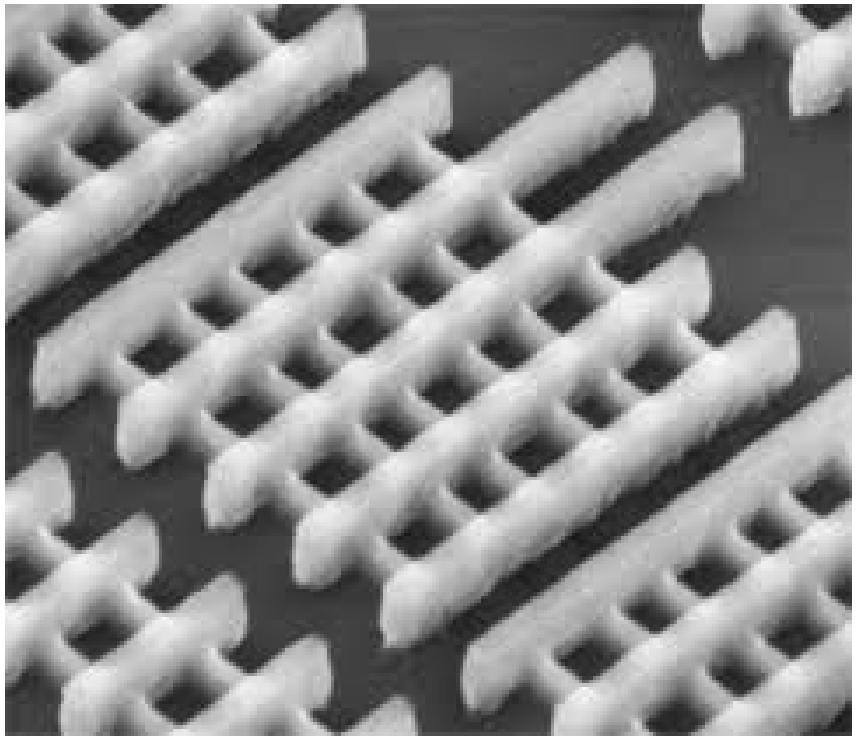


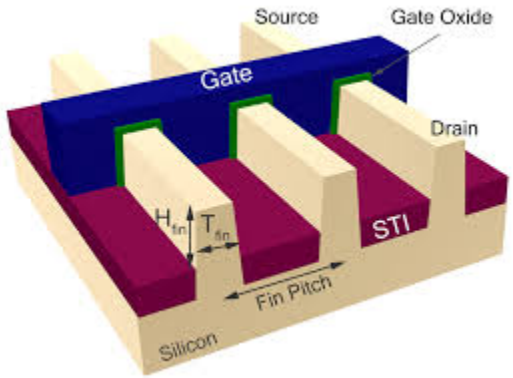
Conventional Planar FET



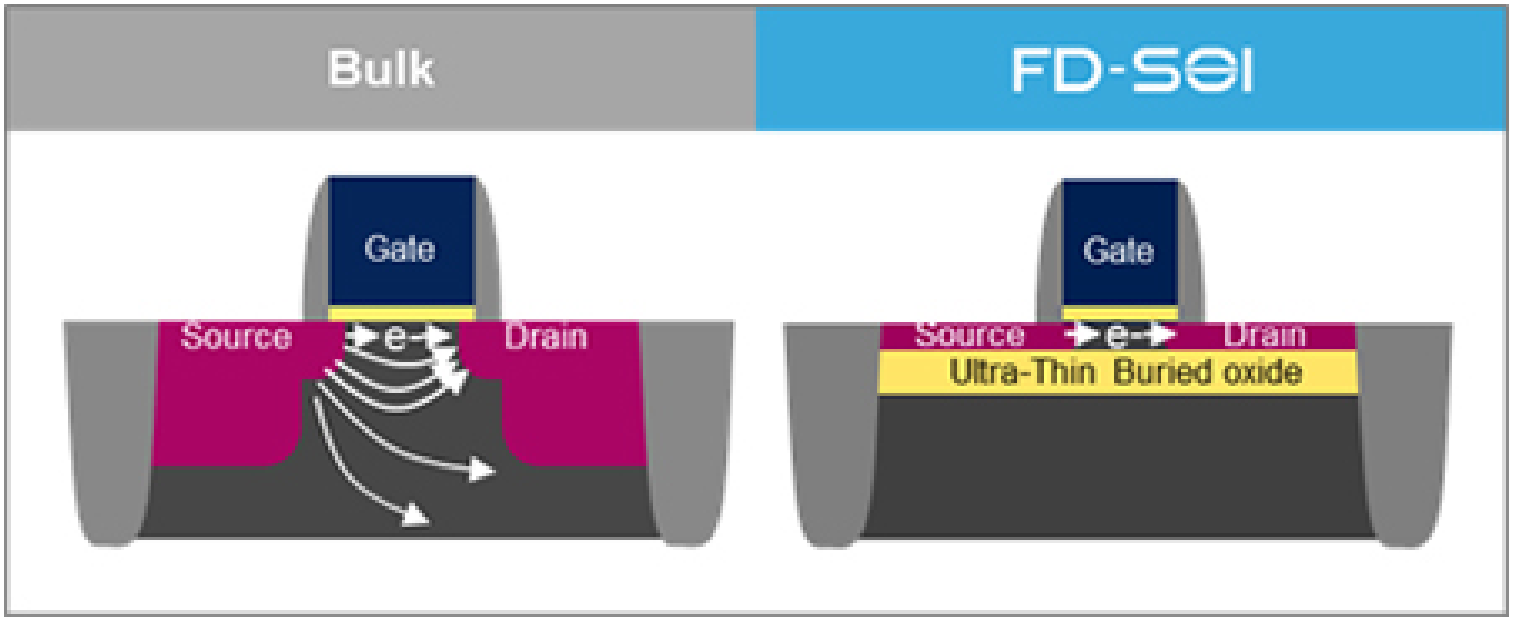
(a) Normal Wafer: FinFETs on regular wafers rely on a timed etch to form the fins

FinFETs in Silicon





Fully Depleted SOI



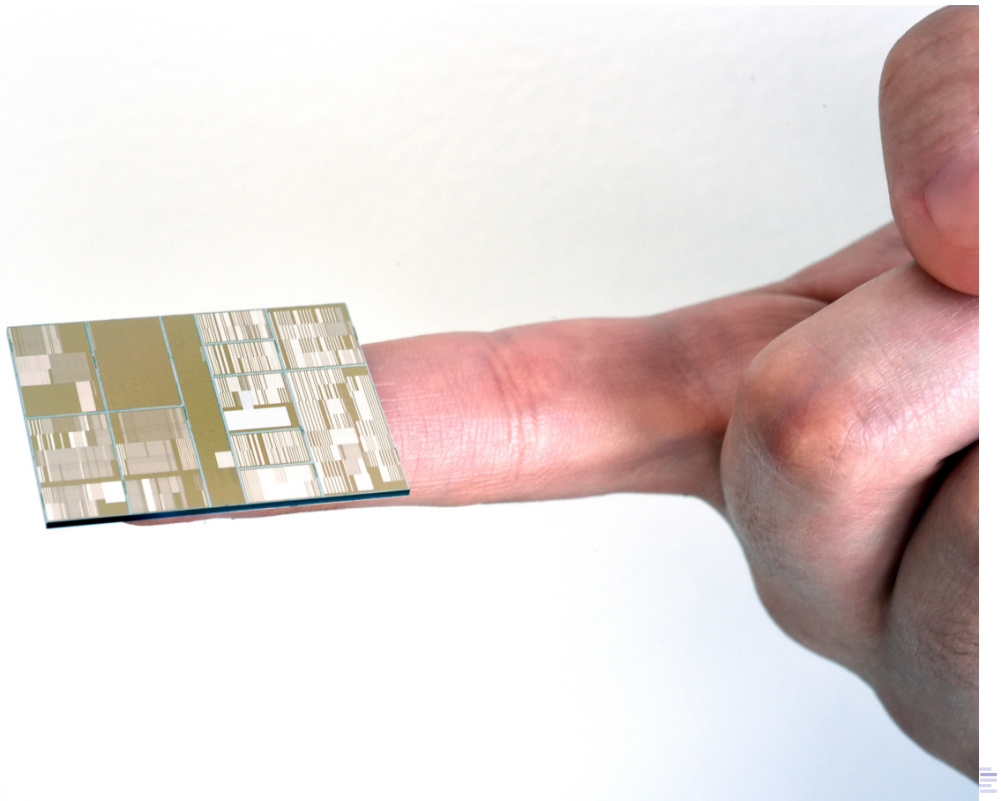
Source: STM

- Advantages of UTB-FD-SOI
  - → Fast switching speed
  - → Low leakage currents
  - → Dynamic control
  - → "Simpler" process
  - → Scalable at leat to 10 nm

Towards 5 nm

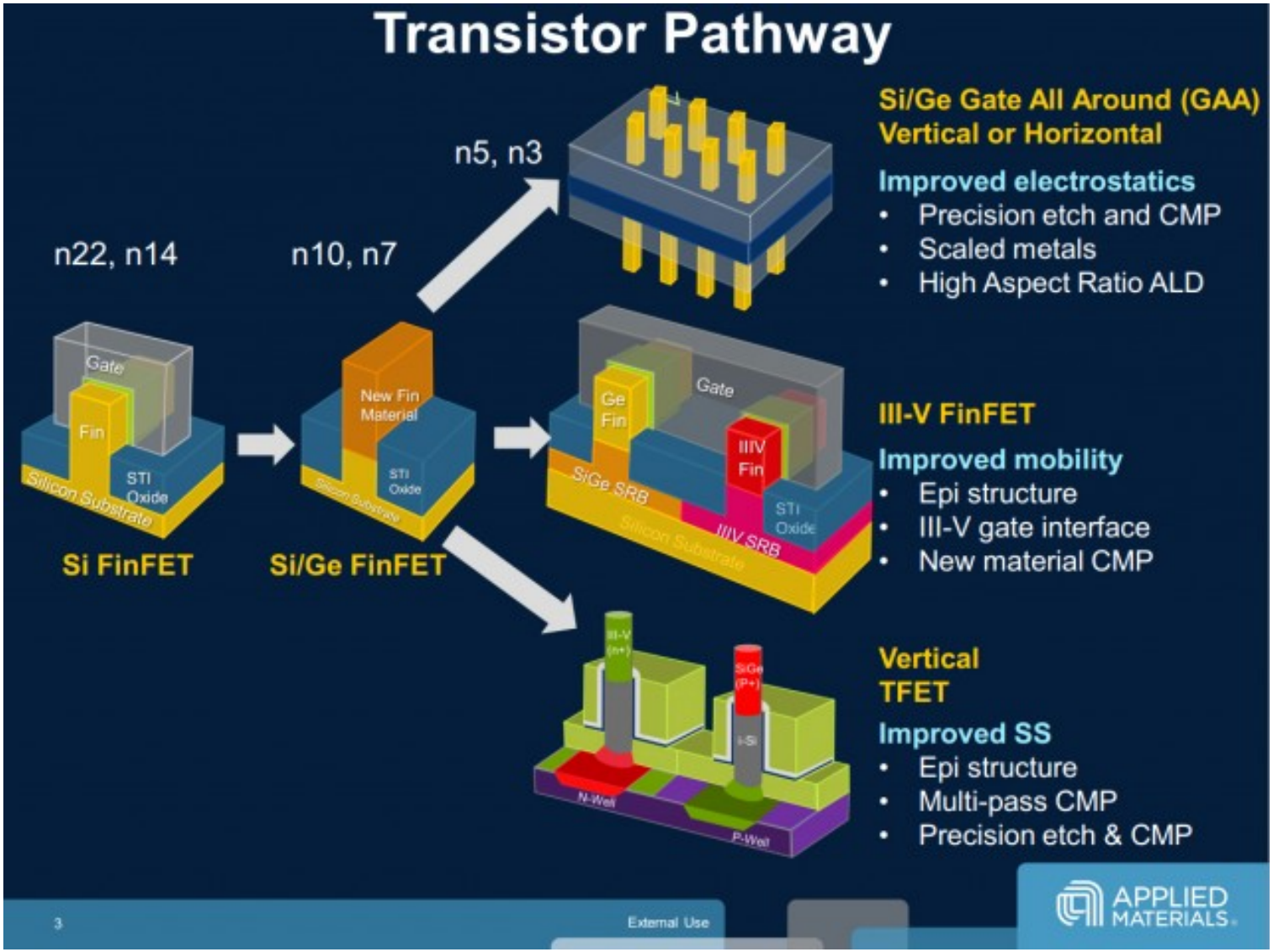
- CMOS scaling will likely continue down to 5 nm (2021-2028)
- '3D transistors: FinFET, gate all-arounde devices
- Non-silicon channel materials: SiGe, III-V compounds (e.g. InGaAs)

http://arstechnica.com/gadgets/2015/07/ibm-unveils-industrys-first-7nm-chip-moving-beyond-silicon/



SiGe channel and EUV lithography

New devices


Transistor Pathway
n22, n14
n10, n7
n5, n3
Gate
Fin
STI Oxide
Silicon Substrate
Si FinFET
New Fin Material
STI Oxide
Si/Ge FinFET
Gate
Ge Fin
SiGe SRB
III/V Fin
III/V SRB
STI Oxide
Si/Ge Gate All Around (GAA)
Vertical or Horizontal
Improved electrostatics
• Precision etch and CMP
• Scaled metals
• High Aspect Ratio ALD
III-V FinFET
Improved mobility
• Epi structure
• III-V gate interface
• New material CMP
N-Well
P-Well
Vertical
TFET
Improved SS
• Epi structure
• Multi-pass CMP
• Precision etch & CMP
3
External Use
APPLIED MATERIALS

Scaling: a key consequence

MOS in strong inversion:

$$I_{DS} = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \qquad g_m = \sqrt{2\mu C_{ox}\frac{W}{L}I_{DS}}$$

MOS in weak inversion:

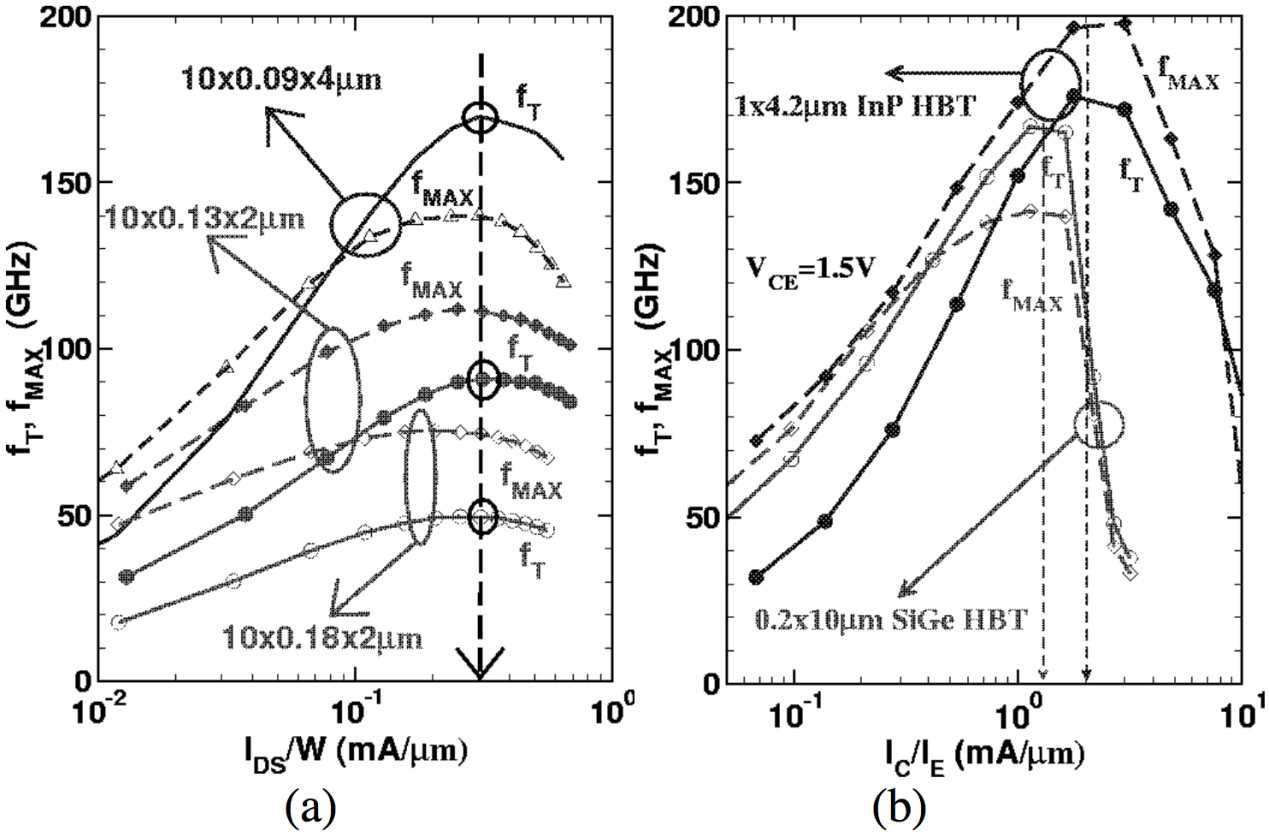
$$I_{DS} = 2n\mu C_{ox}\phi_T^2\frac{W}{L}e^{\frac{V_{GS}-V_{TH}}{n\phi_T}} \qquad g_m = \frac{I_{DS}}{n\phi_T} \qquad I_C = \frac{I_{DS}}{2n\mu C_{ox}\frac{W}{L}\phi_T^2}$$

Bipolar transistors

$$I_C \propto e^{\frac{V_{BE}}{\phi_T}} \qquad g_m \propto \frac{V_{BE}}{\phi_T}$$

As technology shrinks, MOS transistors behave more and more as bipolar

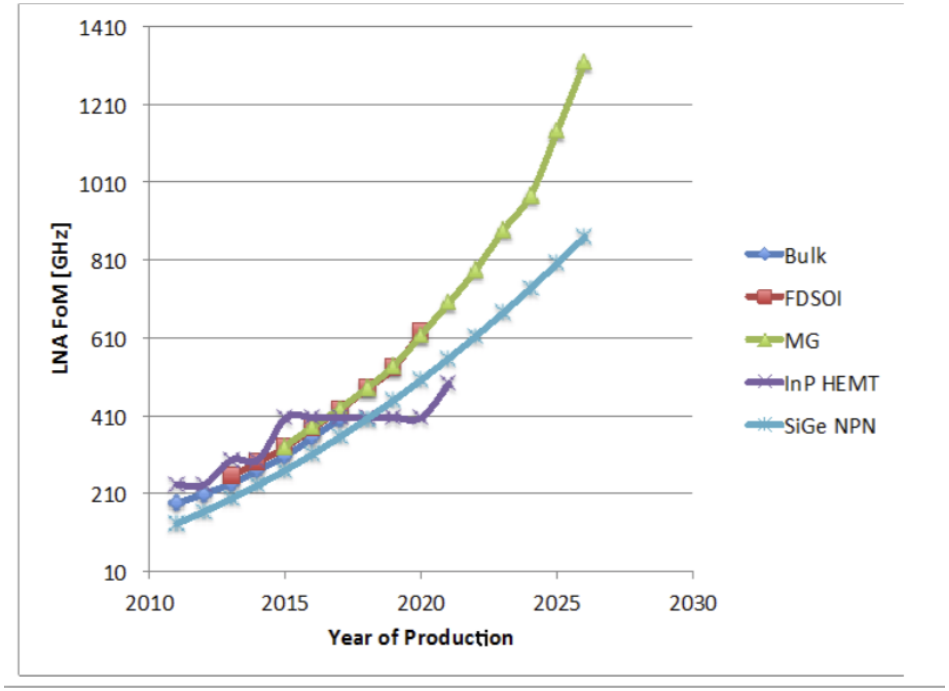
Transistor's speed

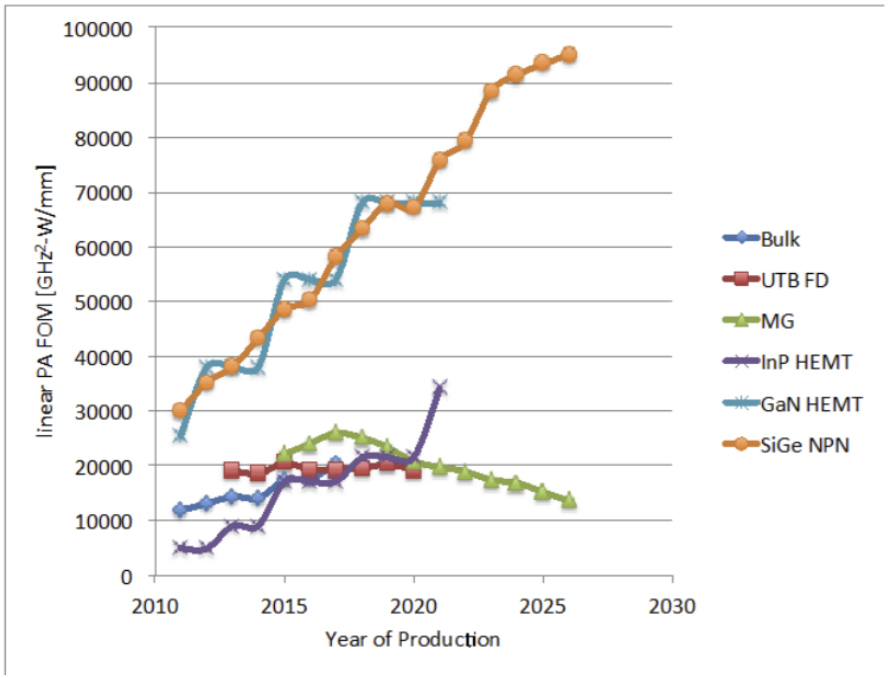


S. P. Voinigescu et al., A Comparison of Silicon and III-V Technology Performance and Building Block Implementations for 10 and 40 Gb/s Optical Networking ICs, IJHSES, Vol.13, No.1, paper 2, March, 2003

The ITRS view

Tables from ITRS 2013





- For RF LNA CMOS is bound to outperform even SiGe transistors
- For RF power amplifiers SiGe bipolar still unbeatable

Back to FinFET's

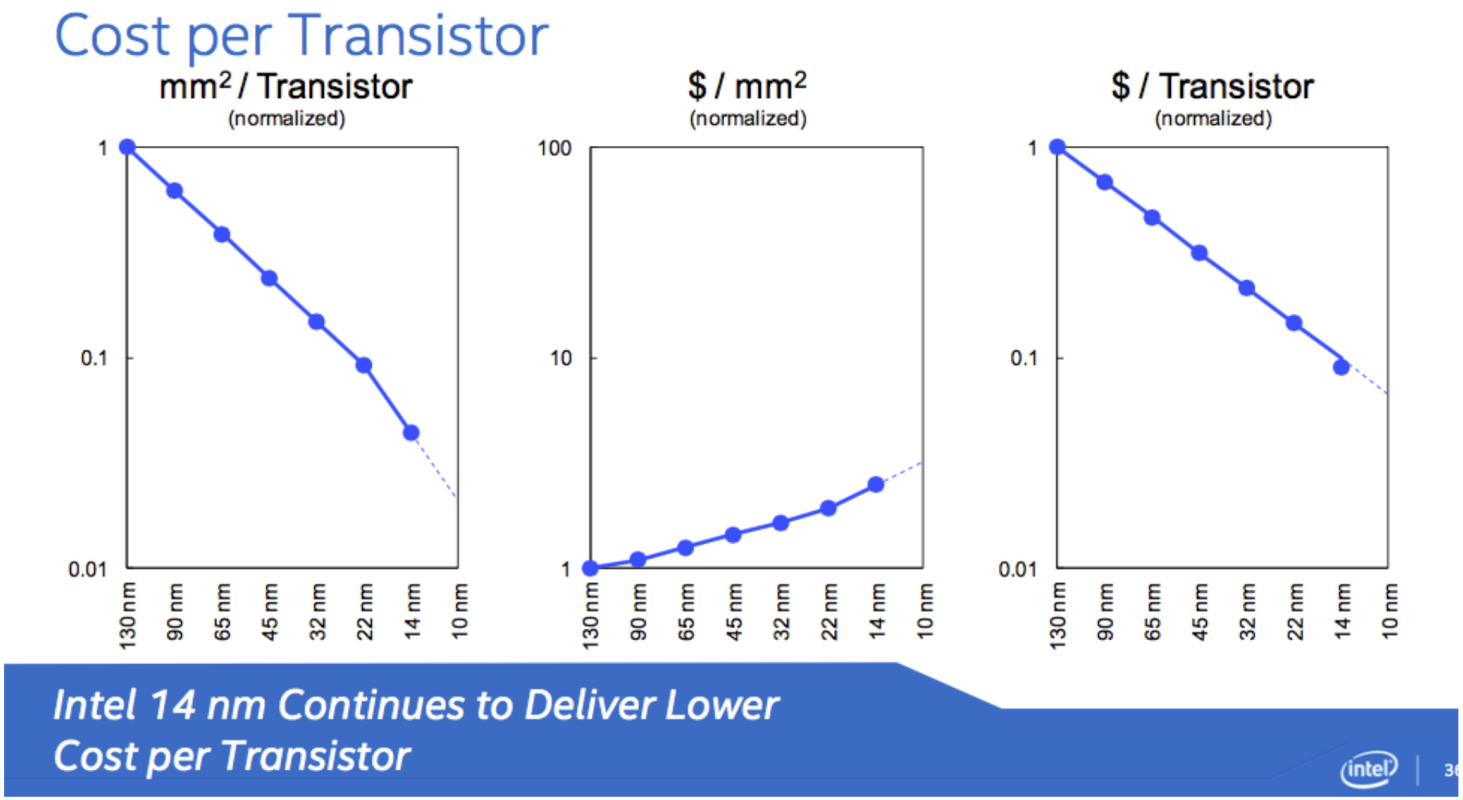
S. Hyun Park et al Performance Comparisons of III-V and strained-Si in Planar FETs and Non-planar FinFETs at Ultra-short Gate Length (12nm)

Structure	Single-gate		Double-gate		Triple-gate	
Material	InGaAs	Si	InGaAs	Si	InGaAs	Si
SS [mV/dec]	97	91	84	75	69	71
$DIBL$ [mV/V]	234	190	91	93	54	59
I_{ON} [μA/μm]	1033	1196	1747	2020	2490	2629
V_{INJ} [cm/s]	3.3×10^{7}	1.1×10^{7}	4.5×10^{7}	9.5×10^{6}	4.7×10^{7}	1.1×10^{7}
N_{INV} [/cm^2]	1.5×10^{12}	5.7×10^{12}	2.1×10^{12}	1.1×10^{13}	3.7×10^{12}	1.8×10^{13}

- Silicon is at the end quite robust
- FinFET's have a better subthreshold slope, this implies closer-to-bipolar g_m/I_D
- Novel devices like TFETs have the perspective of a g_m/I_D even better than bipolar!

A look at economics

Scaling is at the end driven by the dismal science



source: Intel

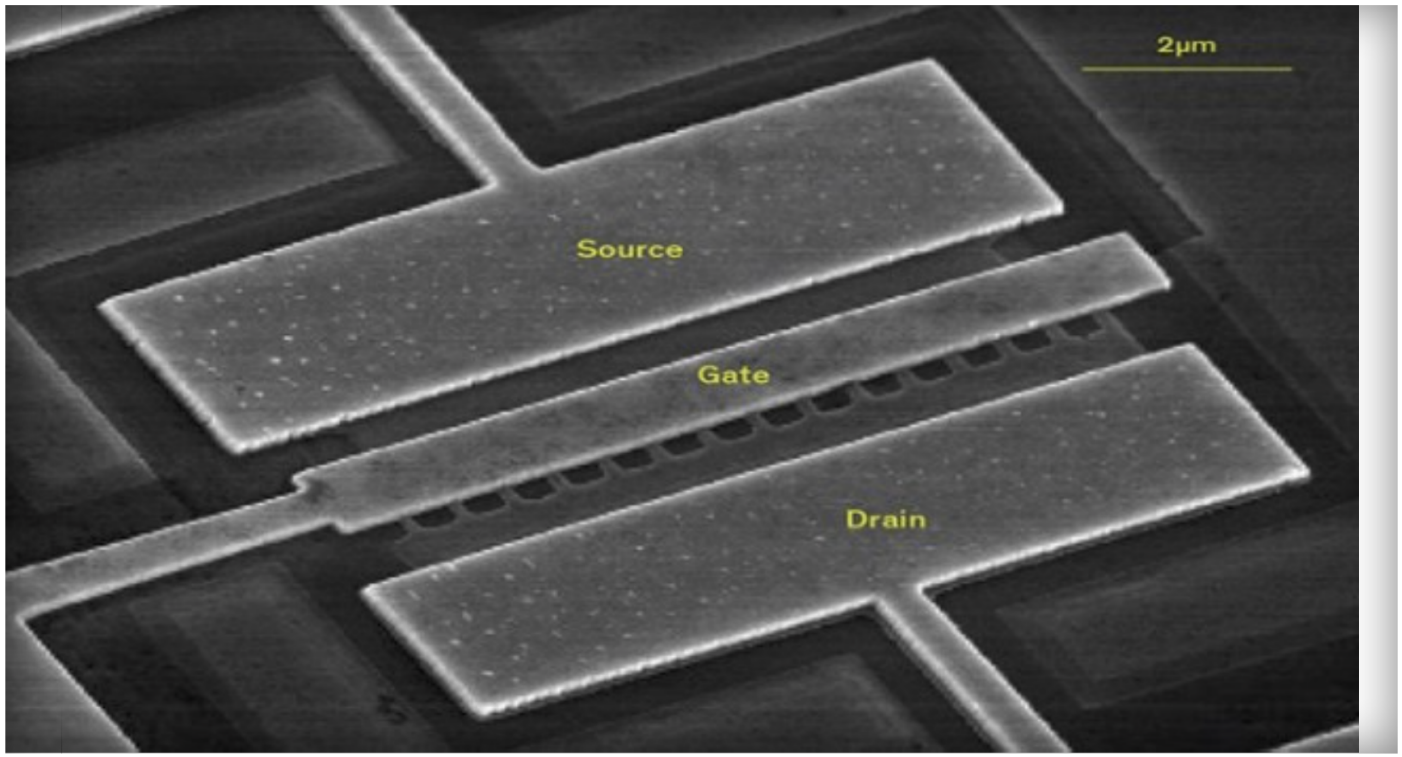
- Scaling has made transistors cheaper and cheaper at each generation
- There is surely limit to CMOS scaling, but other technologies will come to the rescue

TFET on the edge?

HOME (HTTP://WWW.EXTREMETECH.COM) COMPUTING (HTTP://WWW.EXTREMETECH.COM/CATEGORY/COMPUTING)
TOSHIBA WANTS TO RESHAPE THE CHIP INDUSTRY WITH NEW LOW-POWER TUNNEL FETS, $2 BILLION INVESTMENT

Toshiba wants to reshape the chip industry with new low-power tunnel FETs, $2 billion investment

By Joel Hruska (http://www.extremetech.com/author/jhruska) on September 10, 2014 at 2:35 pm
12 Comments (http://www.extremetech.com/computing/189757-toshiba-wants-to-reshape-the-chip-industry-with-new-low-power-tunnel-fets-2-billion-investment#disqus_thread)



TFET may cut digital power consumption by 80%

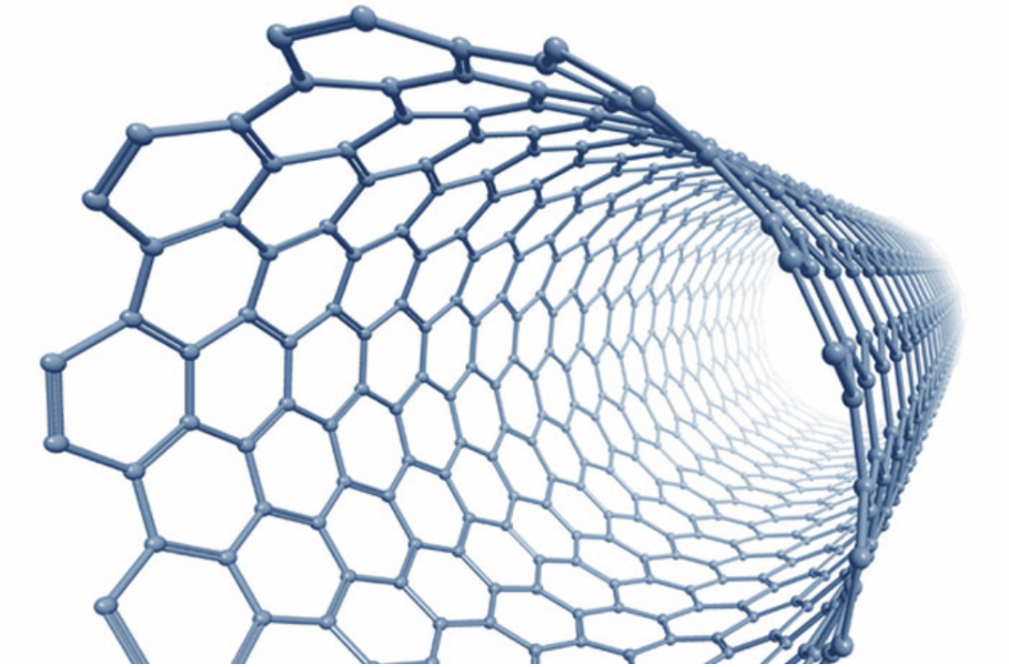
Beyond 5 nm?

IBM carbon nanotube discovery paves way for post-silicon future

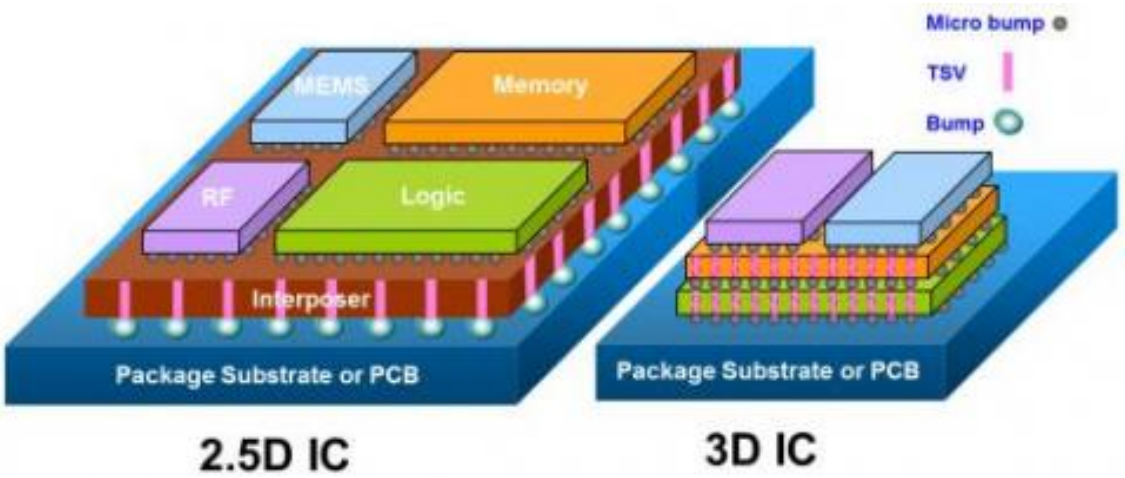
by **Mark Tyson** on 2 October 2015, 13:01

Tags: IBM (NYSE:IBM)
Quick Link: HEXUS.net/qacu4m
Add to My Vault:

IBM says that its scientists have made a major engineering **breakthrough** that could help speed the transition from silicon-based transistors to those constructed from carbon nanotubes. Its new discovery, which concerns the two contacts of a transistor, leads IBM to believe that its carbon nanotube technology could scale all the way down to 1.8nm.



3D Integration



- 3D stack is a way to continue Moore's law
- It is now being more pursued by the industry
- It allows in addition heterogeneous integration
- 3D MPW services now being regularly offered

3D integration at play

TRENDING: Windows 10 cheat sheet (with video!) · Computerworld's holiday gift guide 2015 · Resources/White Papers

COMPUTERWORLD

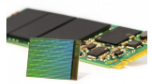
NEWS

Samsung unveils 15TB SSD based on densest flash memory

An exploded view of one of Samsung's 2.5-in SSDs. Credit: Samsung

MORE LIKE THIS

Samsung releases world's first 2TB consumer SSDs



Today's NAND flash has hit a development dead-end

SanDisk, Toshiba double down, announce the world's highest capacity 3D NAND...

on IDG **Answers**

If I buy a Chromebook and can't get to grips with OS can I convert to windows?

Progess in critical blocks: ADC

$$FoM = \frac{P}{2^{ENOB} \cdot F_s}$$

Technology	Architecture	N of bit	Sampling rate (MS/s)	ENOB	Power (mW)	FOM (Fj/step)
90 nm	SAR	9	40	8.23	0.82	68
130 nm	SAR	10	50	9.11	0.82	30
65 nm	SAR	10	100	9.01	1.13	22
90 nm	FLASH+SAR	9	100-200	8.44-8.31	0.75/1.33	34.7
90 nm	SAR	10	50	9.5	0.32	9

- Conversion speed of 100 - 200 Ms/sec can be achieved with 1 mW or less
- SAR and its variant has become a dominant topology
- Almost digital-only approach, amenable to scaling

Ultra-scaled ADCs

26.4 A 3.1mW 8b 1.2GS/s Single-Channel Asynchronous SAR ADC with Alternate Comparators for Enhanced Speed in 32nm Digital SOI CMOS

Lukas Kull[1,2], Thomas Toifl[1], Martin Schmatz[1], Pier Andrea Francese[1], Christian Menolfi[1], Matthias Braendli[1], Marcel Kossel[1], Thomas Morf[1], Toke Meyer Andersen[1], Yusuf Leblebici[2]

[1]IBM Research, Rüschlikon, Switzerland, [2]EPFL, Lausanne, Switzerland

Specifications	[1]	[2]	[3]	[4]	[5]	This work		
Architecture	SAR	Ti-SAR	Ti-SAR	SAR	SAR	SAR		
CMOS Technology (nm)	65	65	65	28	40	32		
Resolution (bits)	8	6	8	8	6	8		
Supply Voltage (V)	1.2	1.2	1.0	1.0	1.0	1.0	1.1	0.9
SNDR near Nyquist (dB)	44.5	31.5	42.75	43.3	30.5	39.3	39.3	38.8
Sampling Speed (GHz)	0.4	1	1	0.75	1.25	1.2	1.3	1.0
Speed per Channel (GHz)	0.4	0.5	0.5	0.75	1.25	1.2	1.3	1.0
Power (mW)	4.0	6.7	3.8	4.5	6.08	3.1	4.2	2.0
FOM (fJ/conf step)	73	210	24	41	178	34	43	28
Area (mm^2)	0.024	0.11	0.013	0.004	0.013	0.0015		
Area for 64GS/s (mm^2)	3.8	7.0	8.3	0.26	0.67	0.080	0.074	0.096

Progress in critical blocks: TDCs

Technology	Architecture	Resolution (ps)	Sampling rate (MS/s)	Range (ns)	Power (mW)	Area
130 nm	GRO	1	50	12	2.2-21	0.04
130 nm	Vernier-ring	8	15	32	7.5	0.26
90 nm	Passive inter.	4.7	180	0.6	3.6	0.02
90 nm	Delay line	20	26	0.64	6.9	0.01
65 nm	2D delay line	4.8	50	< 0.6	1.7	0.02
90	Time Amp.	1.25	10	0.64	3	0.6
90	Vernier+GRO	3.2	25-100	40	3.6-4.5	0.027

- TDCs are now hitting sub-ps resolutions
- They are now compact and low-power blocks
- A variety of architectures
- Mostly digital blocks $\rightarrow$ improve with scaling

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The needs

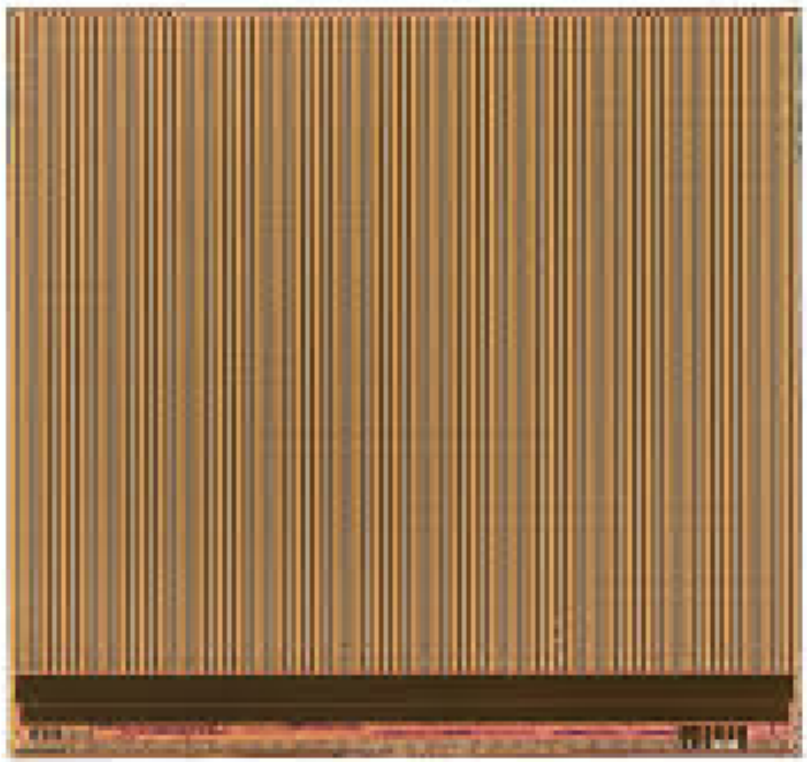
- Specs are vastly different from applications to applications
- In general, we want more with less
- Better space resolution
- Better time resolution
- More data bandwith
- More in situ processing
- ....

Hybrid pixel electronics

FEI-4 for ATLAS hybrid pixels

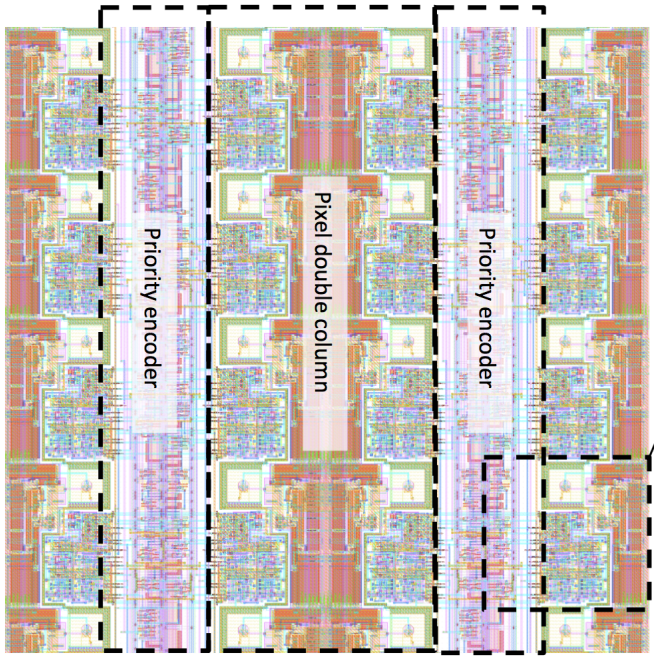
- Full reticle chip
- Shared-logic between pixels
- Digital-only outputs
- CMOS 130 nm

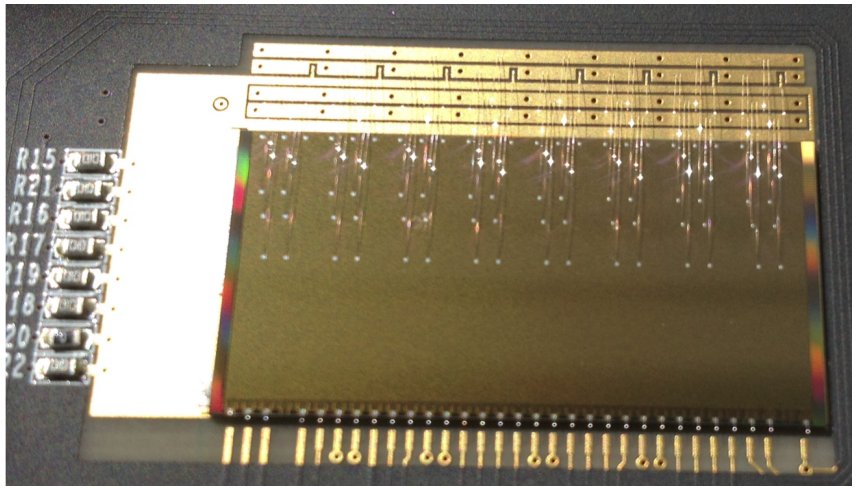
→ Digital-on-top design approach



Advanced monolithics

ALPIDE chip - ALICE ITS

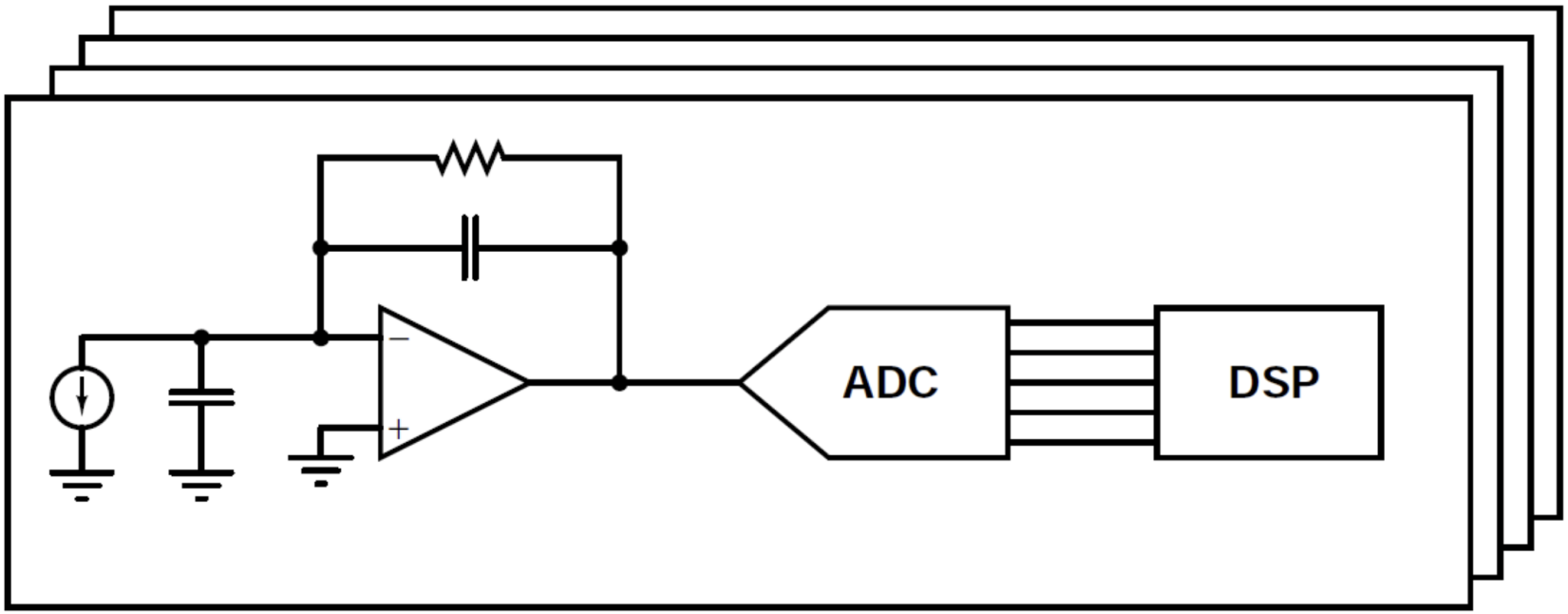




- Hybrid-like readout
- Pixel size: 30 μm$\times$30μm
- Peaking time: 2 μs
- Power: 40 mW/cm^2
- Technology: CMOS 180 nm

$\rightarrow$ Integration of sensing and signal processing electronics

Full digitizing architectures

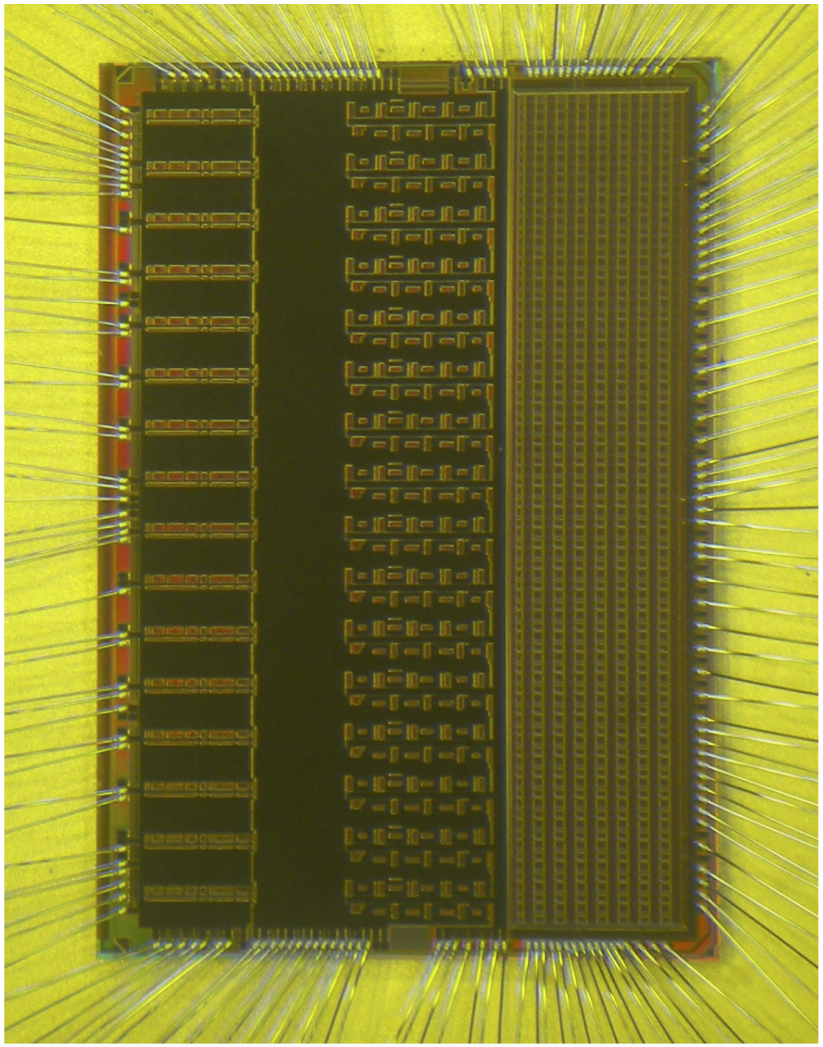


DSP-like chips

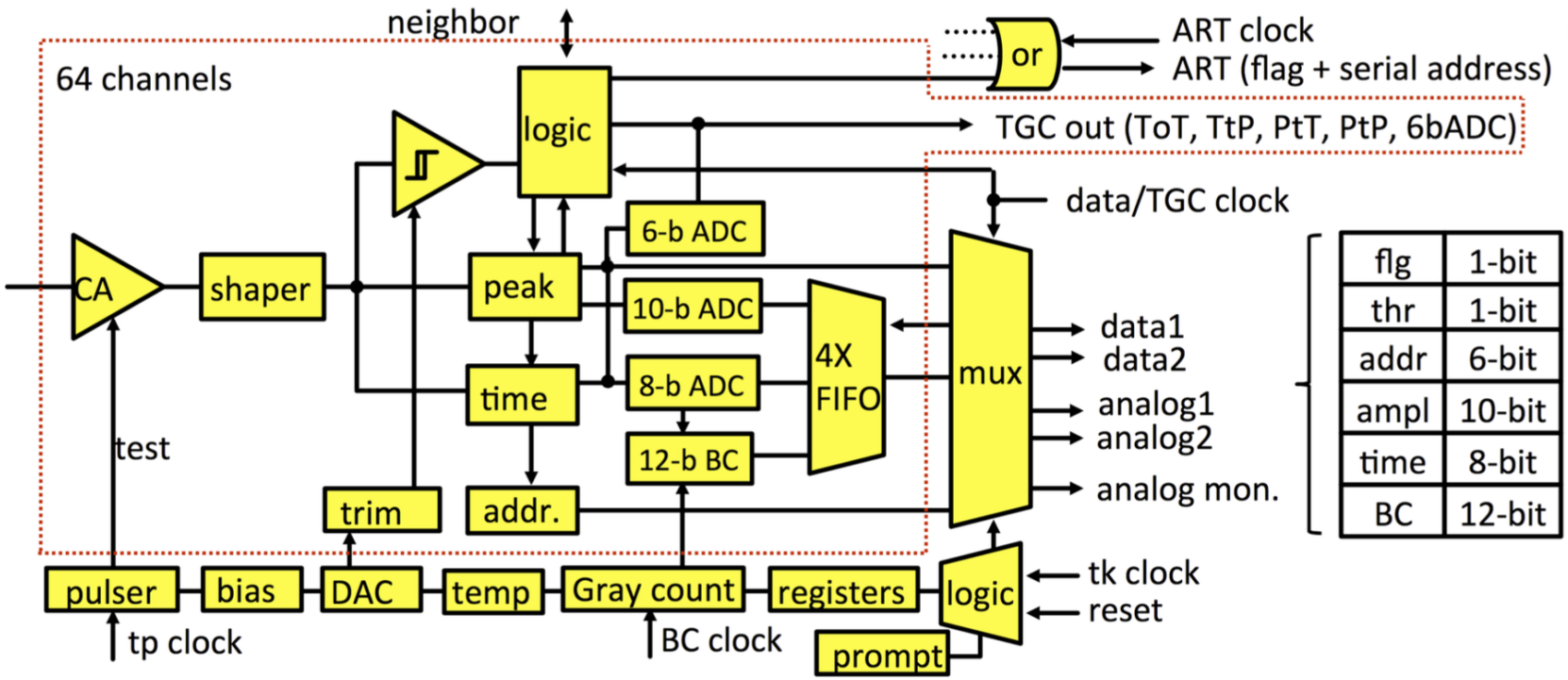
Super-ALTRO chip, CERN

S-ALTRO key performance	
Gain	12, 15,19, 27 mV/fC
Peaking time	30, 60, 90, 120 ns
Signal polarity	both
Detector capacitance	4-20 pF
Number of bits	10
Sampling Frequency	10-40 MHz
Power (active)	47 mW/ch
Power (sleep)	0.6 mW/ch

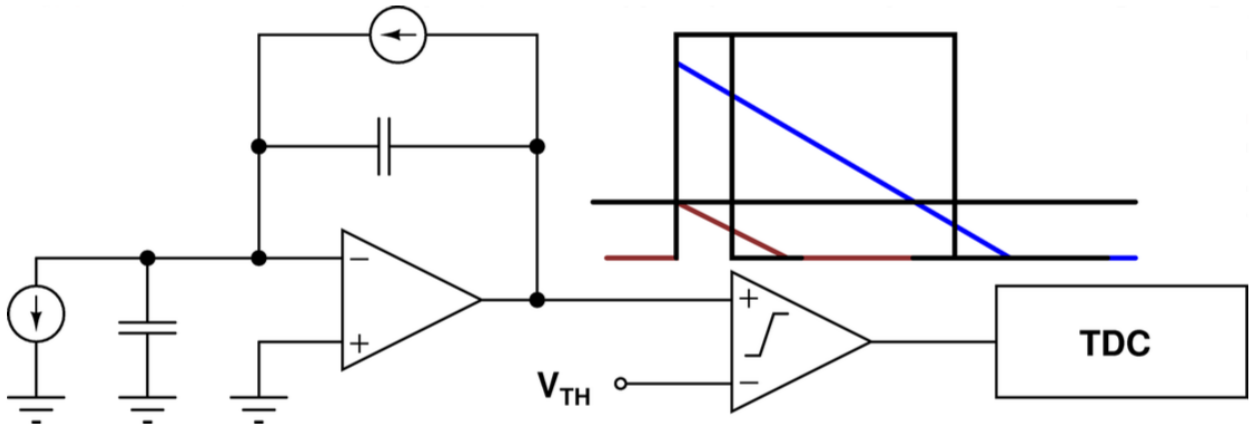
S-ALTRO power break down	
PASA	10 mW/ch
ADC (analog)	31.28 mW/ch
ADC (digital)	1.7 mW/ch
DSP	4 mW/ch



VMM ASIC, BNL


neighbor
64 channels
logic
or
ART clock
ART (flag + serial address)
TGC out (ToT, TtP, PtT, PtP, 6bADC)
data/TGC clock
6-b ADC
CA
shaper
peak
10-b ADC
4X
FIFO
mux
data1
data2
time
8-b ADC
analog1
analog2
test
12-b BC
analog mon.
trim
addr.
pulser
bias
DAC
temp
Gray count
registers
logic
tk clock
reset
tp clock
BC clock
prompt
flg 1-bit
thr 1-bit
addr 6-bit
ampl 10-bit
time 8-bit
BC 12-bit

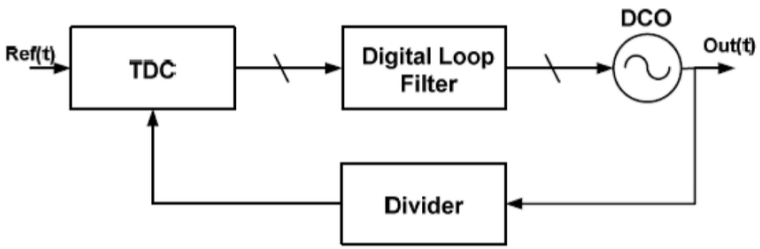
Time-domain signal processing

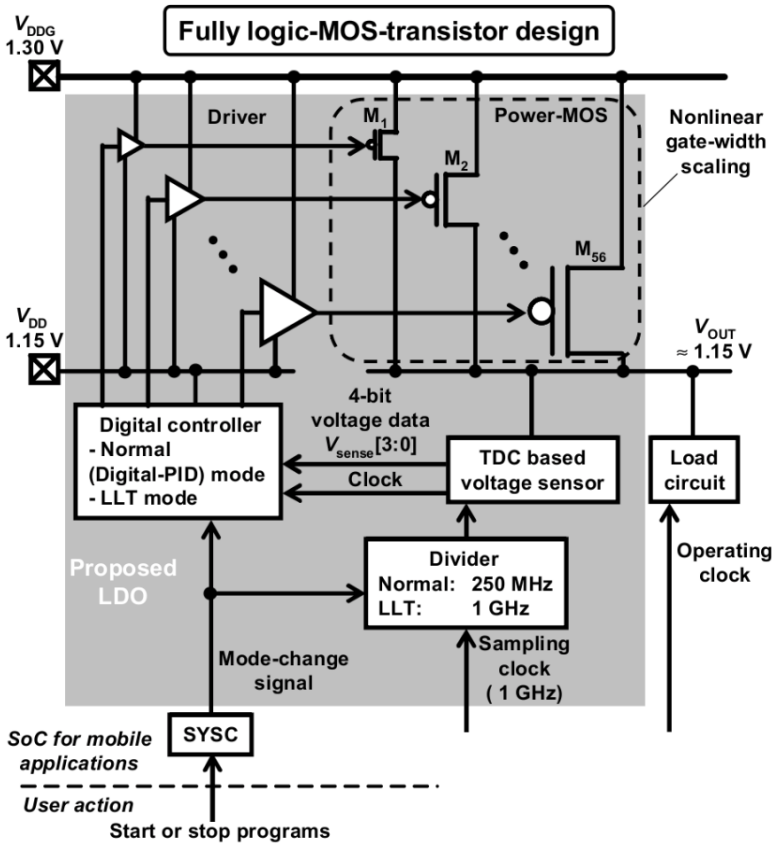


- TDCs are built with digital gates or analog circuits with low dynamic range
- Digitization can occur in the time domain measuring directly the ToT
- Very fast and simple Wilkinson ADC can be built

Time-domain processing

- TDC used to measure phase difference in ADPLL
- With scaling technologies speed of gates increases
- Work in the time domain also to measure voltages



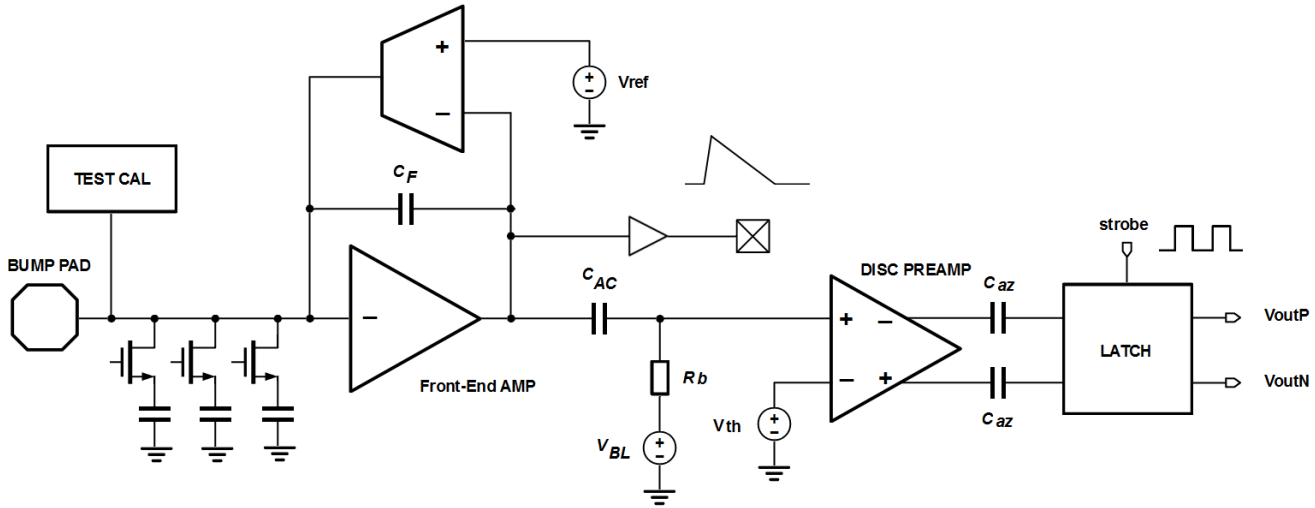


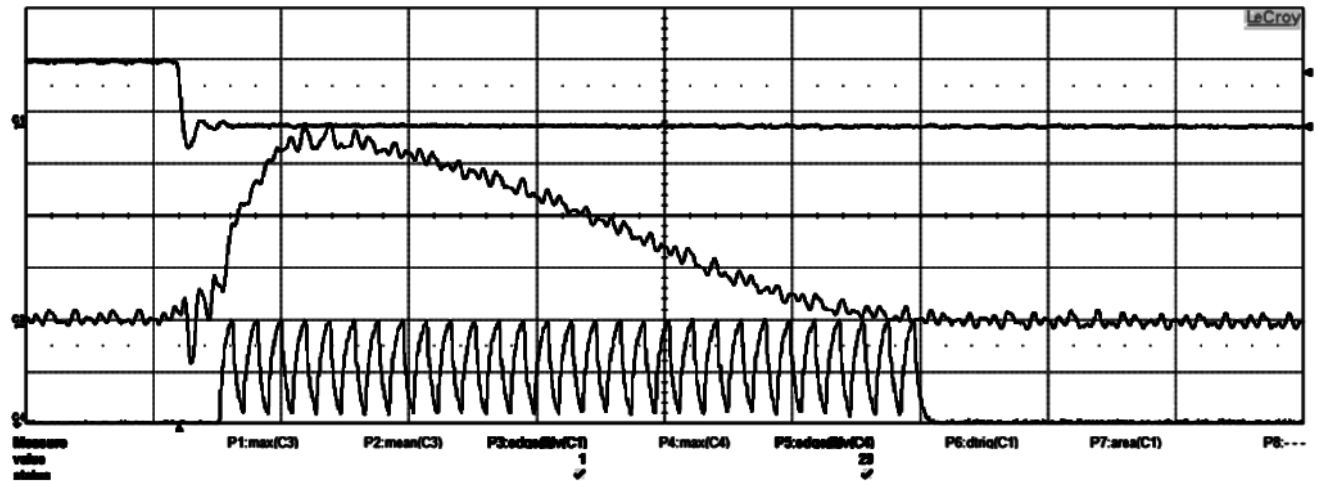
K. Otsuga et al,

IEEE International SoC Conference, 2012

Time-domain processing for detectors

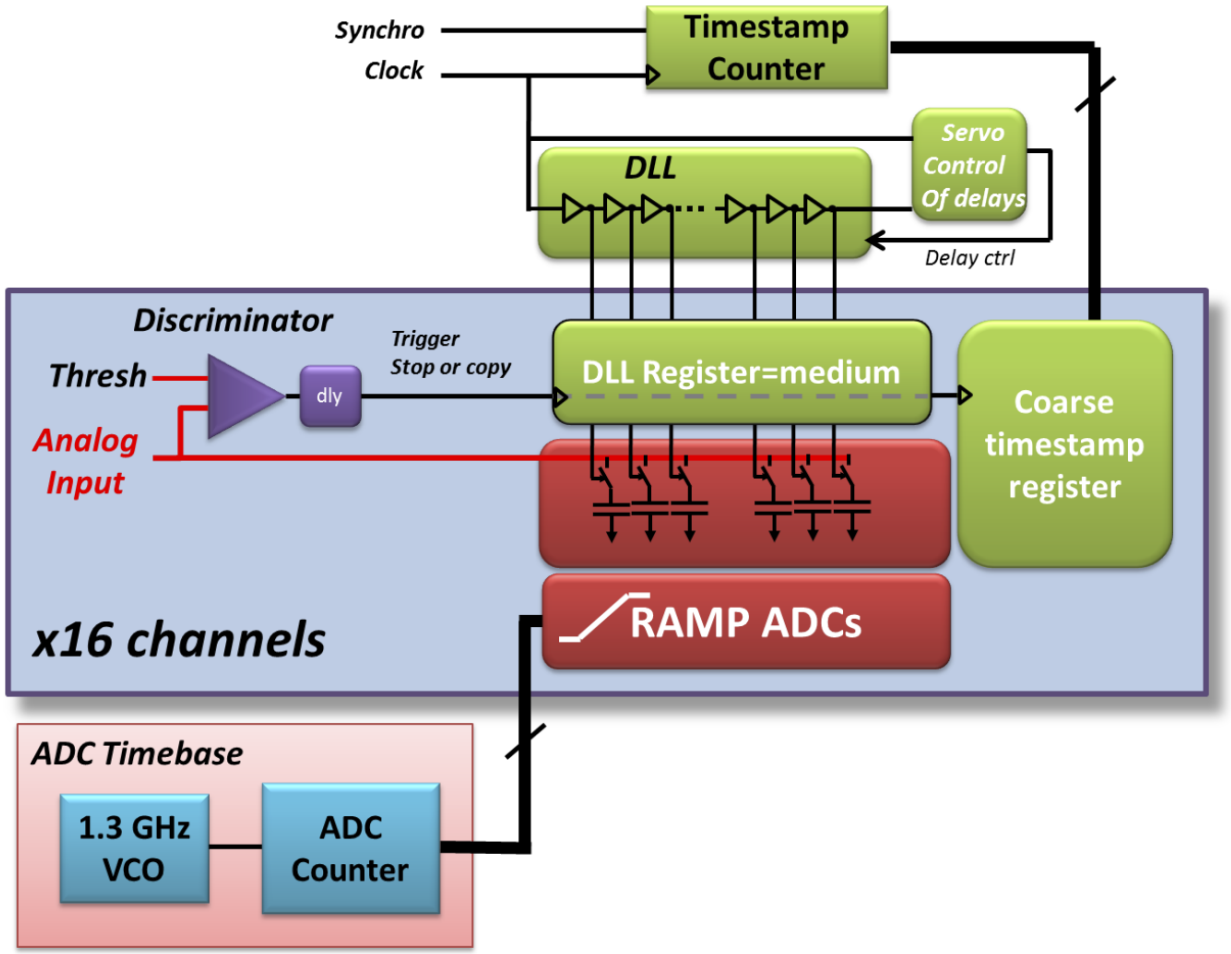
CHIPIX65, INFN





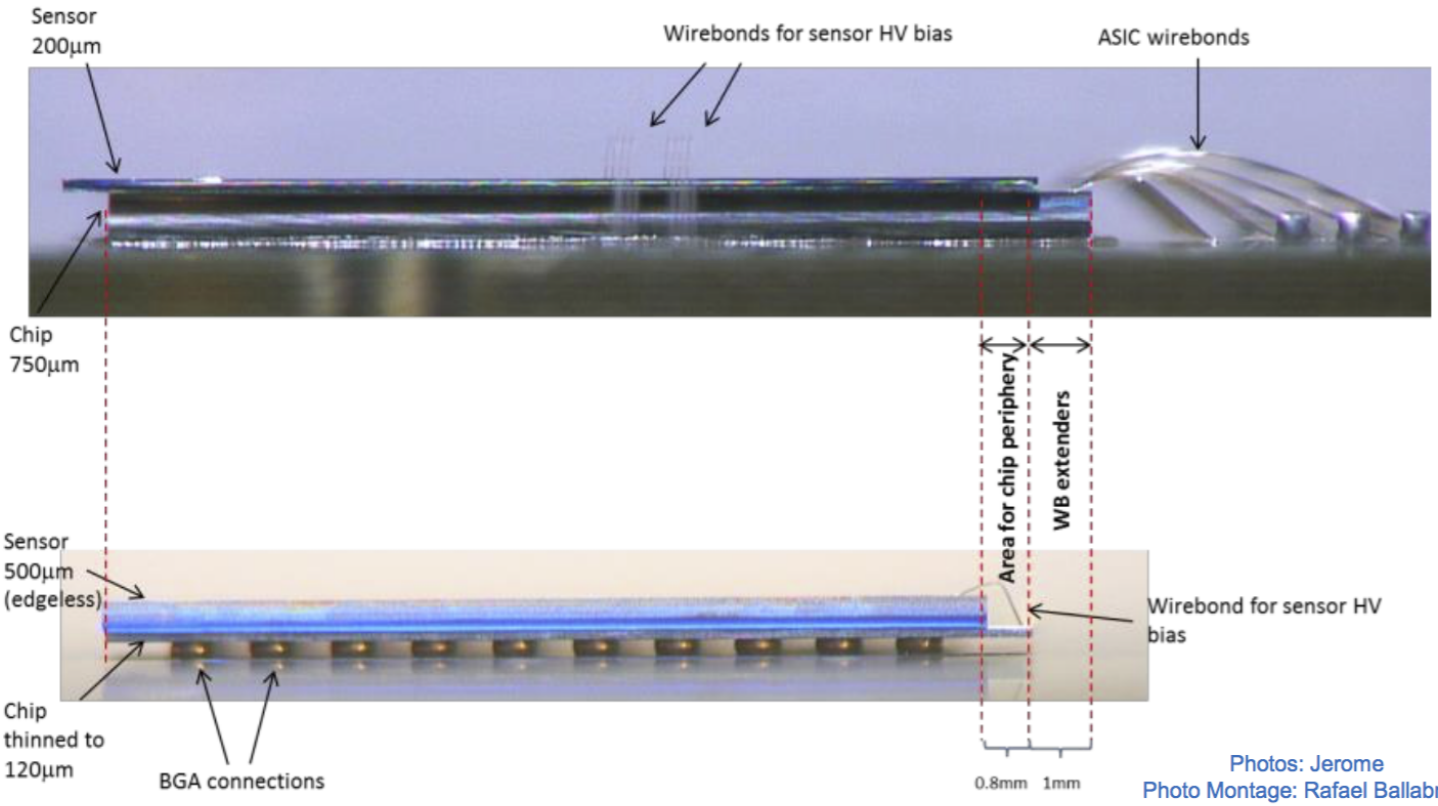
Fast Waveform Digitizer

E. Delagnes et al., Reaching a few picosecond timing precision with the 16-channel digitizer and timestamper SAMPIC ASIC NIM A 787 (2015) 245-249



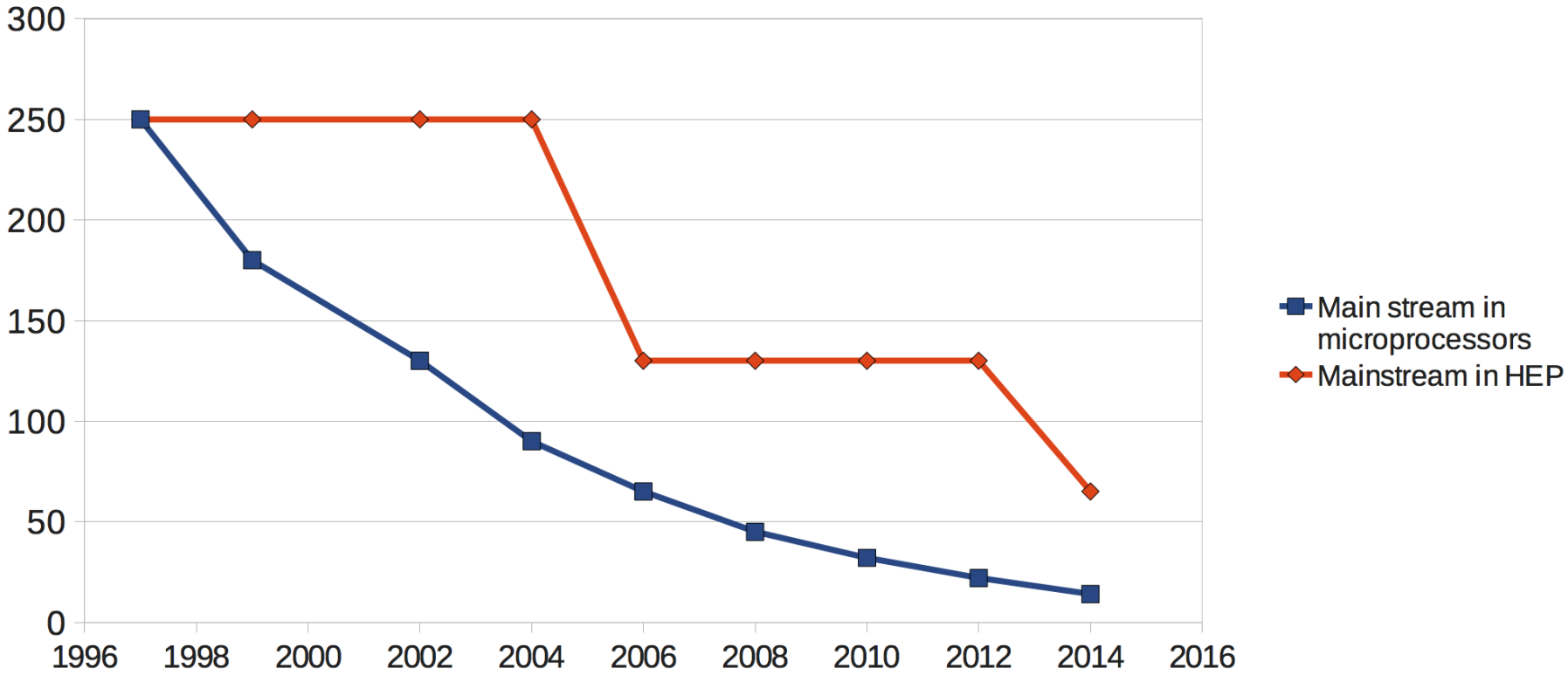
CERN Medipix TSV PROJECT – Second run – Integration

- Comparison between WB and TSV on board integration



Photos: Jerome
Photo Montage: Rafael Ballabriga

The digital divide (again...)



Agenda

1. Introduction
2. The industry: where it is, where it is going
3. Detector electronics: where it is, where it is going
4. Conclusions

Conclusions

- Next ten years in front-end electronics for radiation detectors will still be dominated by CMOS technologies
- Ultra-scaled CMOS processes may provide opportunities for extraordinary performance improvements
- Ultra-scaled processes are affordable for R&D
- Ultra-scaled processes can be affordable for very low or very high volumes
- Scaled and less scaled technologies will coexist for several years

Conclusions

- Need to take advantage non only from the progress on technology, but also from those on key building blocks
- 3D integration coming of age
- Highly complex, monolithic CMOS sensors becoming a reality
- Design tools are vey powerful but also very complex

This is complexity

Snapdragon 820, O(100) man years of work...