Status of DO and TF firmware

IAPP-FTK General Assembly / Executive Board meeting

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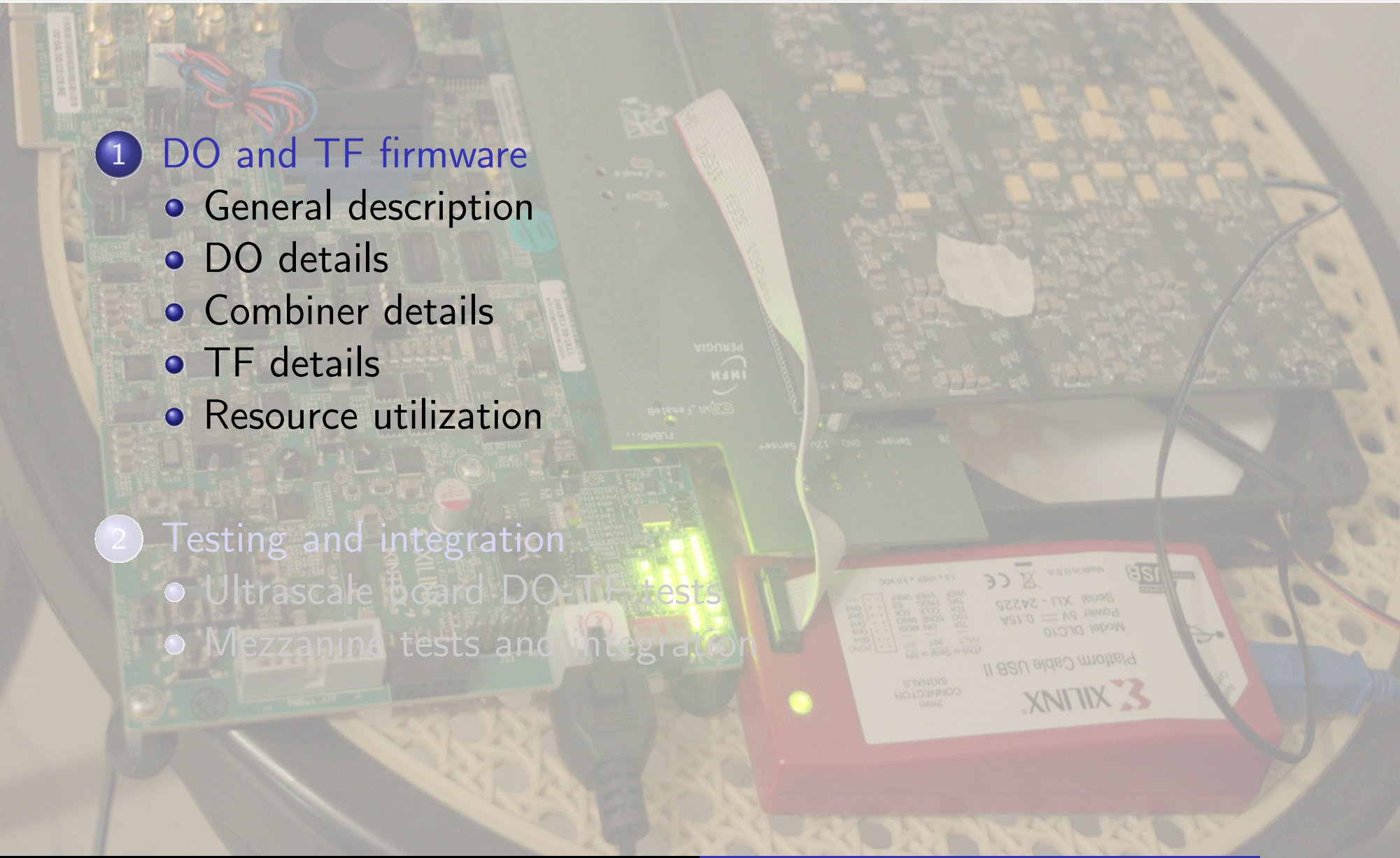
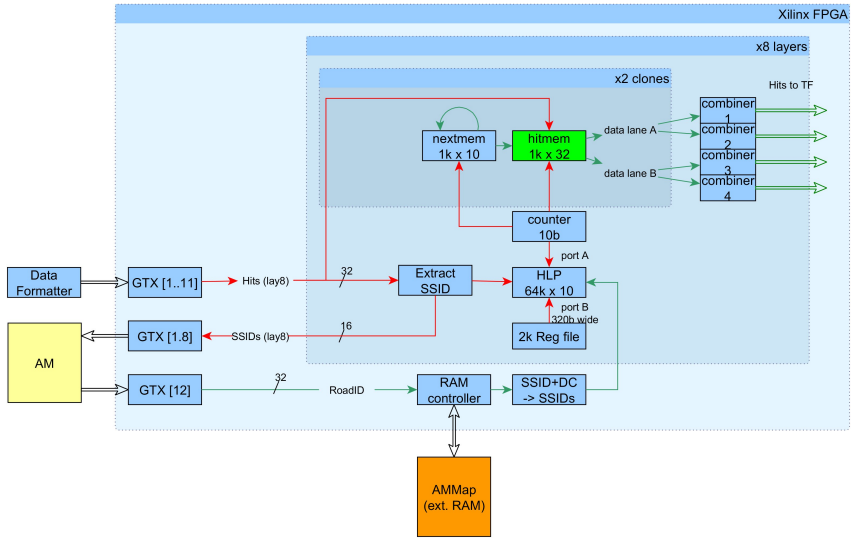
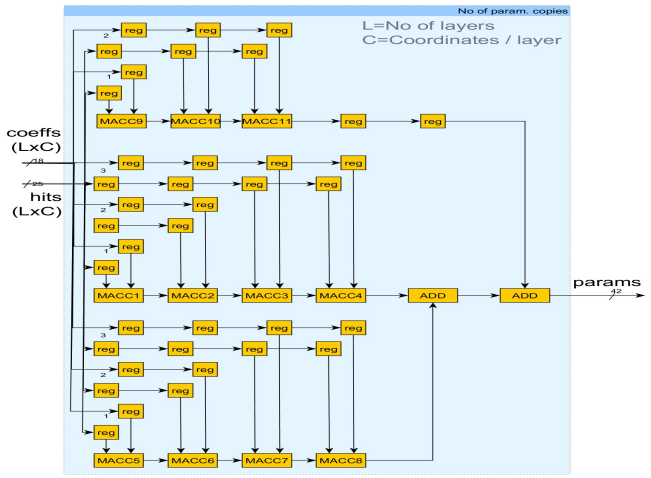


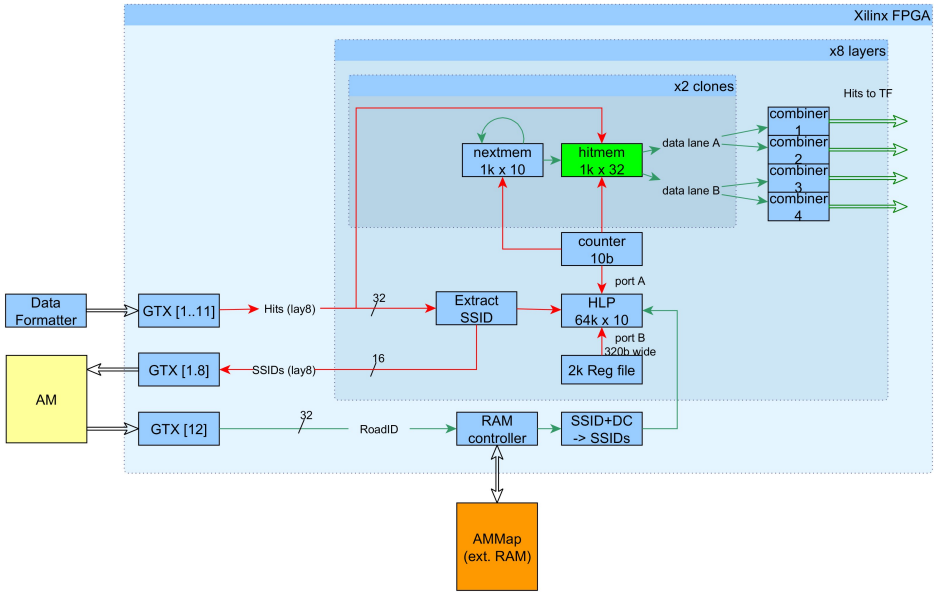
General Description

- High performance implementation
- 200MHits/layer/sec DO input rate
- up to 2GFits/sec TF performance
- 300ns fixed total DO+TF latency (inside the FPGA device)





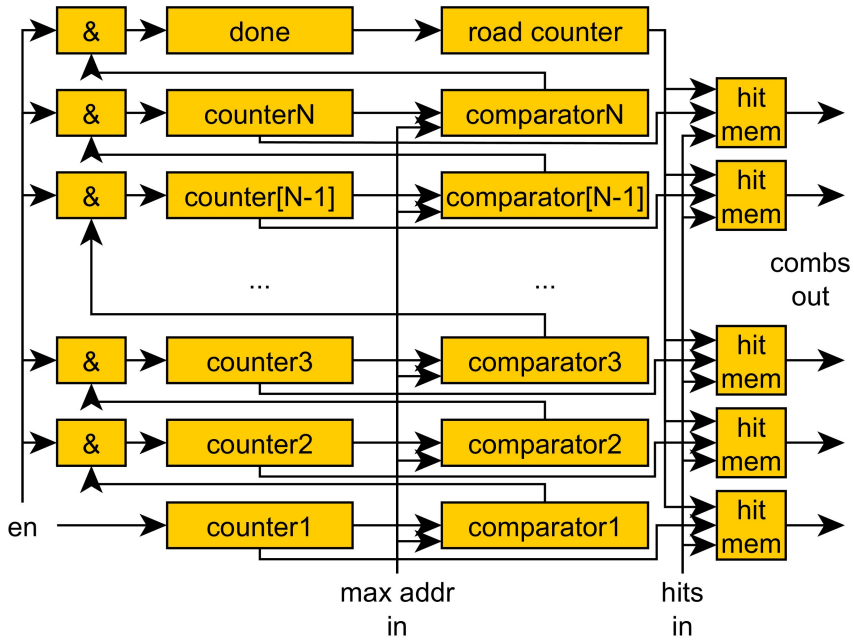
DO details



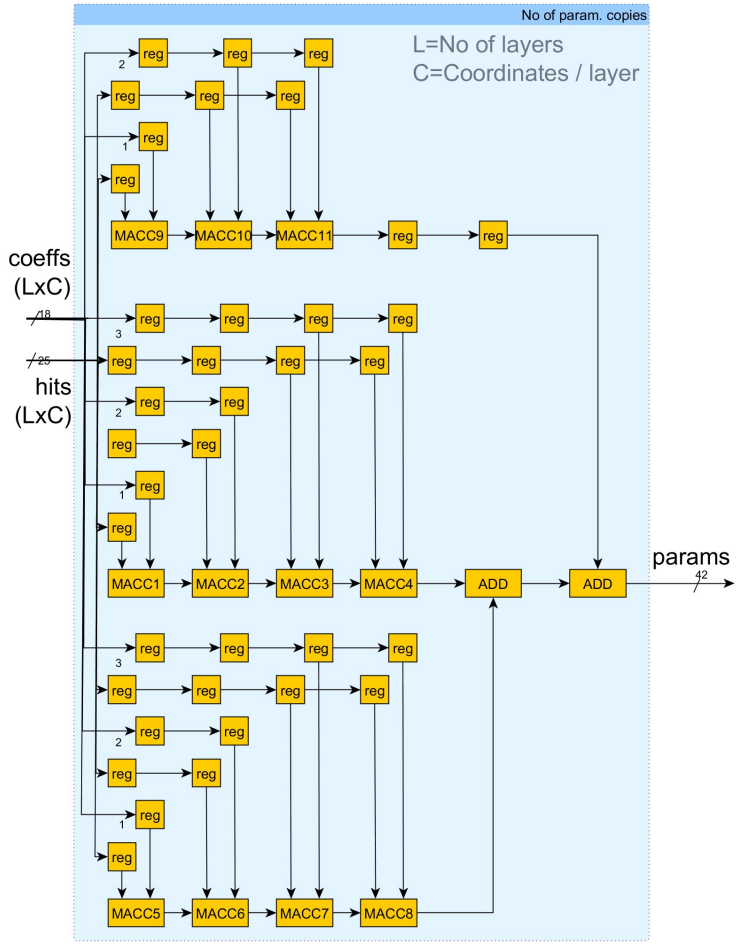
- Fast architecture, 400MHz fmax
- Two modes of operation (write, read)
- Write mode stores stubs in the database and sends the coarse representation to the AMChips
- Read mode gets the results from the AMChips, decodes it using external RAM, and gets the stubs from the database to send to the combiners
- Read mode especially optimized for quick stub retrieval, due to use of very wide memories and parallelism
- Two DO units can fit for ping-pong operation (one writes, other reads)
- TC builder (see next talk) can be integrated on each output to reduce tracks

Combiner details

- Calculates all valid track combinations of a pattern
- Long critical path leads to low op. frequency wrt TF
- We use two combiner modules for each TF module
- Each detected pattern gets assigned to a combiner, a couple of patterns with many combinations may take a long time (while the rest are done)
- Future optimization: modify it to count up/down so two combiners can share one road



TF details

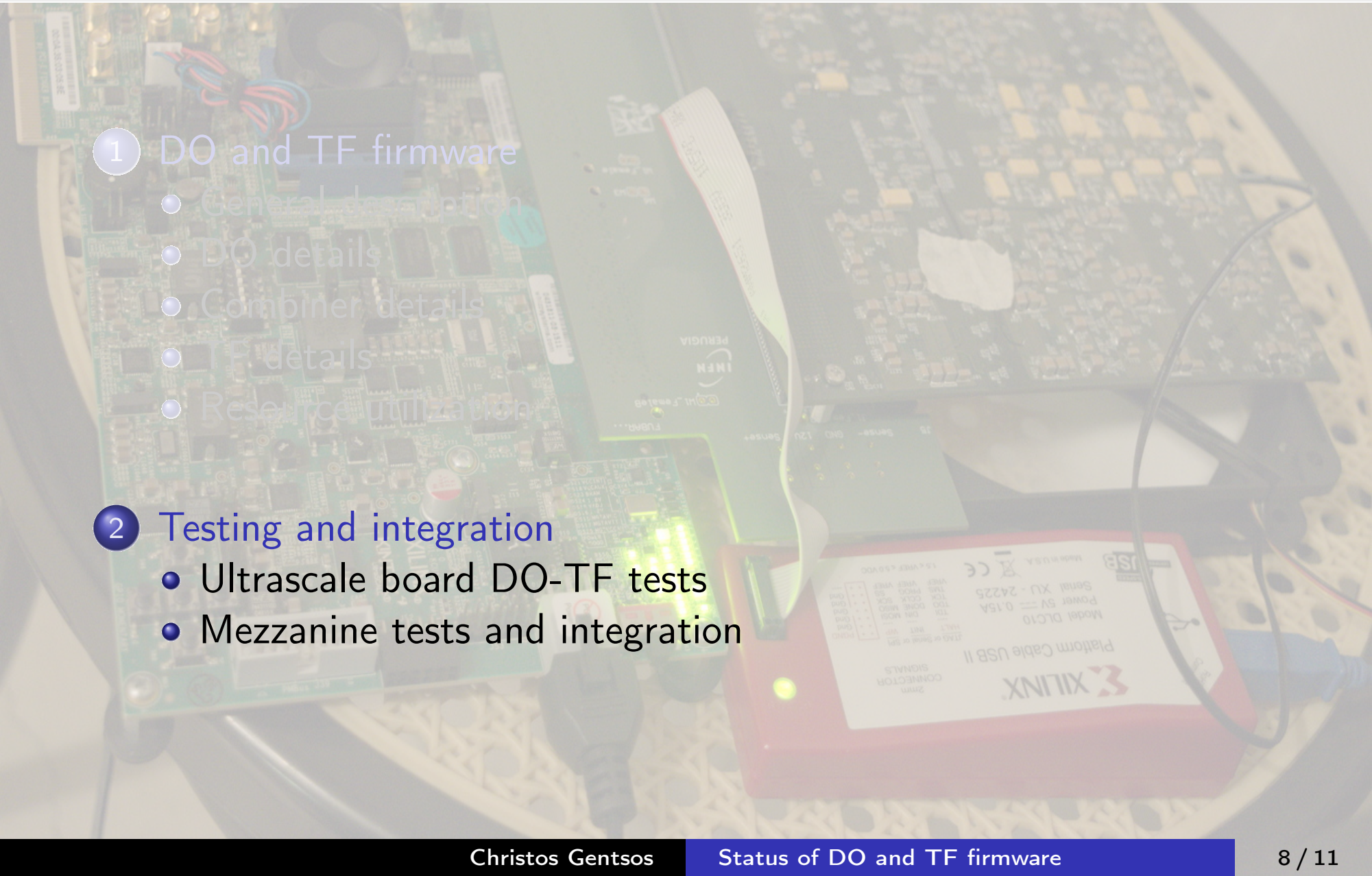


- Extensive use of DSP units
- Frequency of 500MHz+
- One fit/clock cycle
- $<$ 100ns latency
- Multiple units can run in parallel
- 4 units can fit in a mid-grade device giving 2GFits/sec
- Fit coefficients stored in BRAM memory resources
- If we can do with a small number of coefficient sets, possible to fit more TF units in high grade devices

Resource utilization

Type (total)	CLB LUTs (240k)	CLB Regs (480k)	BRAMs (600)	DSPs (1920)
DO	56k	93k	164	0
Comb	0.67k	1.5k	4	0
TF	0.2k	40k	36	190

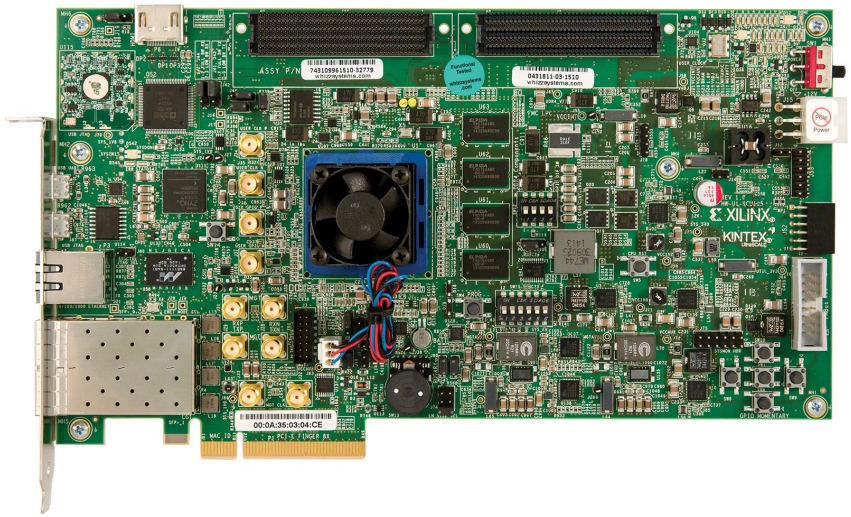
Table: Resource utilization of each component (totals for XCKU040)



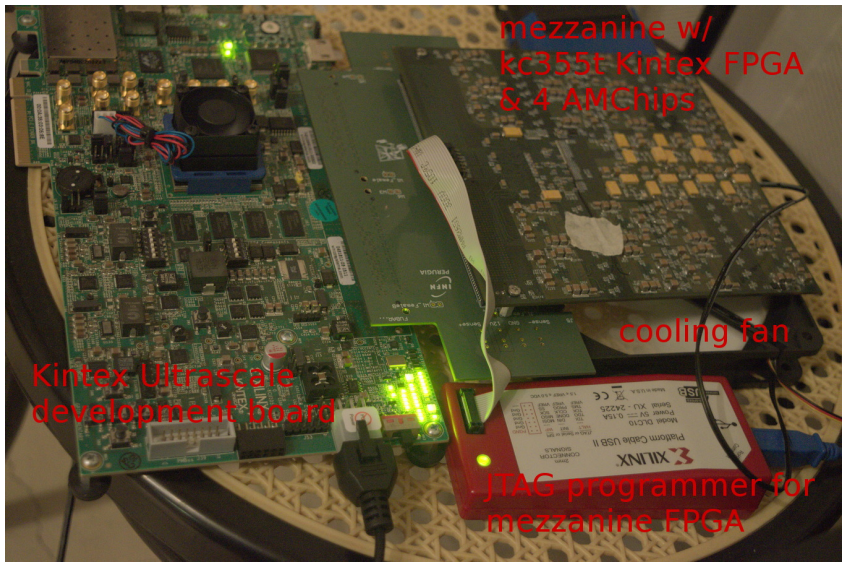
Ultrascale board DO-TF tests

- To test the DO and TF an Ultrascale development board was used
- Verification was done utilizing an IPBus connection over Ethernet
- SystemVerilog testbench running on Modelsim generates random events, emulates the AMChip functionality, and verifies the results

- Tested for 1200 randomly generated events, with 5-15k track candidates each, no major bugs
- A minor bug has to be fixed, but it just affects $< 0.001\%$ of track candidates so we can proceed



Mezzanine tests and integration



- Integration has to proceed towards a more realistic system
- The Ultrascale board will play the role of the Pulsar, sending stubs and receiving the track parameters to forward to the testbench for validation
- The mezzanine currently hosts 4 AMChips and the Kintex-7 FPGA where the firmware will be integrated
- The whole processing chain will initially be verified for single muon events
- This work is currently in progress


Thank you!