Francesco Crescioli secondment to CAEN

3/7/2015 - 21/9/2015

1 Introduction

The secondment lasted from 3/7/2015 to 21/9/2015.
The main topic of this secondment period has been to setup the hardware used for the AMchip05 and AMchip06 test bench in order to be exploited for SLP1 developments.
The period was chosen in order to partially overlap with Christos Gentsos secondment, who is the main developer of the SLP1.

2 AMchip05/AMchip06 test bench

To qualify the associative memory chips of FTK it has been necessary to develop a custom test bench.

The test bench is made of the following hardware components:

- FPGA evaluation board
  - HTG V6 Xilinx Virtex-6 is the board used by the AMchip05/AMchip06 test bench
- FMC mezzanine
  - BGA socket to host AMchip05 or AMchip06
  - Power connectors
  - (AMchip06) DC-DC converters
  - (AMchip06) Shunt resistors for current measurements
  - (AMchip06) SPI ADC for current measurement readout

Figure 1: AMchip05/AMchip06 test bench structure

Two different FMC mezzanine have been developed for AMchip05 and AMchip06 since the BGA pinout is different between the two chips.

The firmware running on the FPGA is able to:

- Deliver JTAG commands to the AMchip
- Send data from internal RAMs to the AMchip
  - Fully programmable
  - Possibility to insert IDLEs and OPcodes in the data stream
  - Loop mode
- Collect data from the AMchip in an internal RAM
  - Possibility to compare internally the data with a reference data stream

The FPGA RAMs (data, program) are accessible from a PC via the IPBus protocol over ethernet connection.

A set of python scripts is available to generate test data, load it on the FPGA and program the test. It is also possible to download a snapshot of the data from the AMchip collected by the FPGA for offline analysis.

All these features were developed in order to have a complete and flexible test environment, but they can be exploited to use the system as a generic FPGA+AM application hardware.

3 SLP1-like environment

The original AMchip05/AMchip06 test bench firmware is written to target the Virtex-6 FPGA available on the HTG V6 evaluation board.

The SLP1 architecture is targeting a series-7 FPGA from Xilinx. The evaluation board available to setup the SLP1-like environment are:

- Xilinx KC705 board equipped with a Kintex-7 325T FPGA
- Xilinx KU705 board equipped with an Ultrascale Kintex-7 FPGA

During the secondment the preliminary work for the setup of the SLP1 algorithm development environment has been done:

- Porting of the IPBus firmware to the series-7
- Porting of the GTX (high speed serial transceivers) IP cores setup to the series-7
- Hardware setup in the laboratory

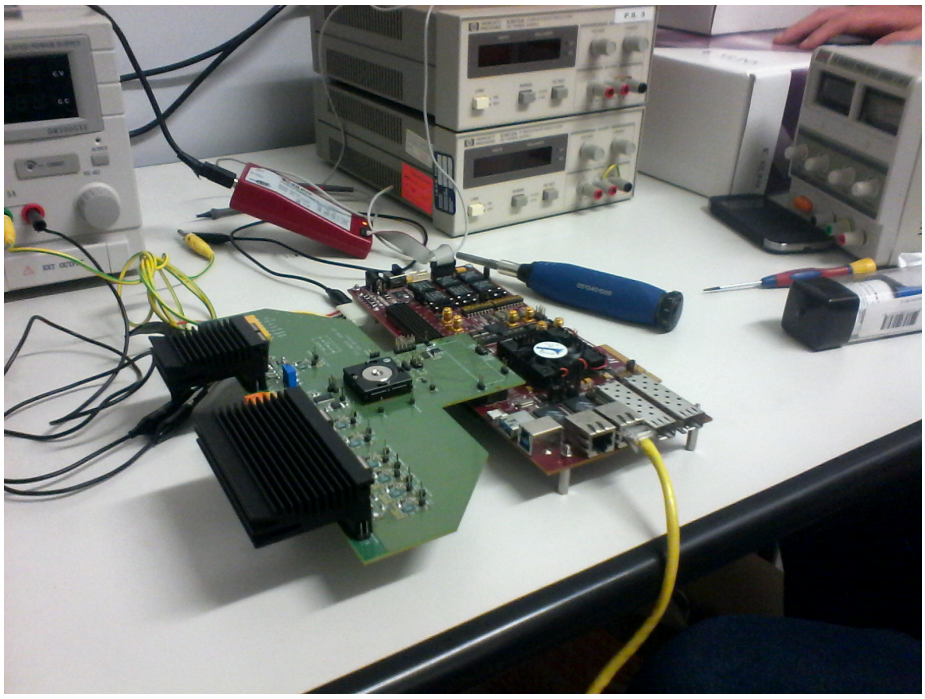

Figure 2: AM06 test bench setup in Pisa

- Software setup on a server PC

With this setup it is possible to build a simple SLP1-like prototype.

4 Conclusions

Exploiting the existing AMchip05/AMchip06 test bench environment for SLP1 development is a fundamental step since the final target hardware of the SLP1 (System on Chip FPGA+AM chip) is not yet available.

It was a natural transfer of knowledge since I am one of the main developers of the AMchip and architects of the AMchip test bench.