Content-Addressable Memory
With pipelined hierarchical search scheme

Outline:

- CAM Operations
  - Nor CAM Cells
  - Pipelined Match-Line
  - Hierarchical Search-Line
- Schematics
- Conclusions
  - Present status
  - How we proceed

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NOR CAM Cells

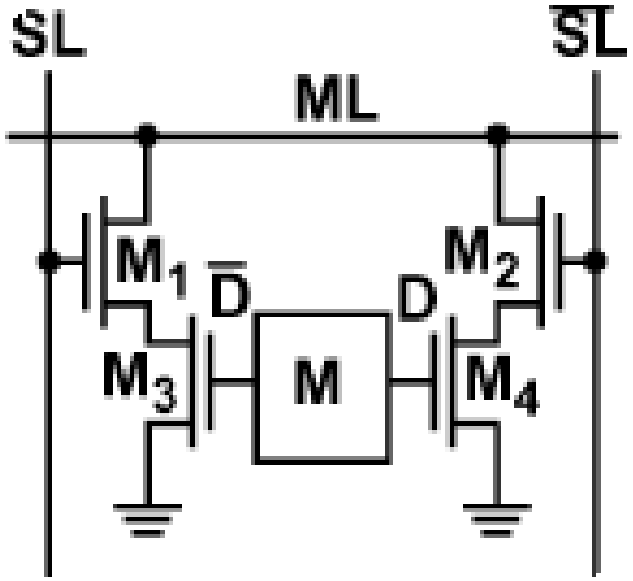

Fig.1: NOR CAM cell schematic

- CAM Compares search data in SL (Search-Line) with stored data D in M
- The Match-Line (ML) is precharged to VDD (ML=VDD match state)
- A mismatch between SL and D results in a series path from ML to ground (ML=0 Miss State)
- M is a 6 transistor SRAM

High power consumption for every Match-Line and Search-Line

Solutions:

- **Pipelined ML**
- **Hierarchical SL**

Pipelined Match-Lines

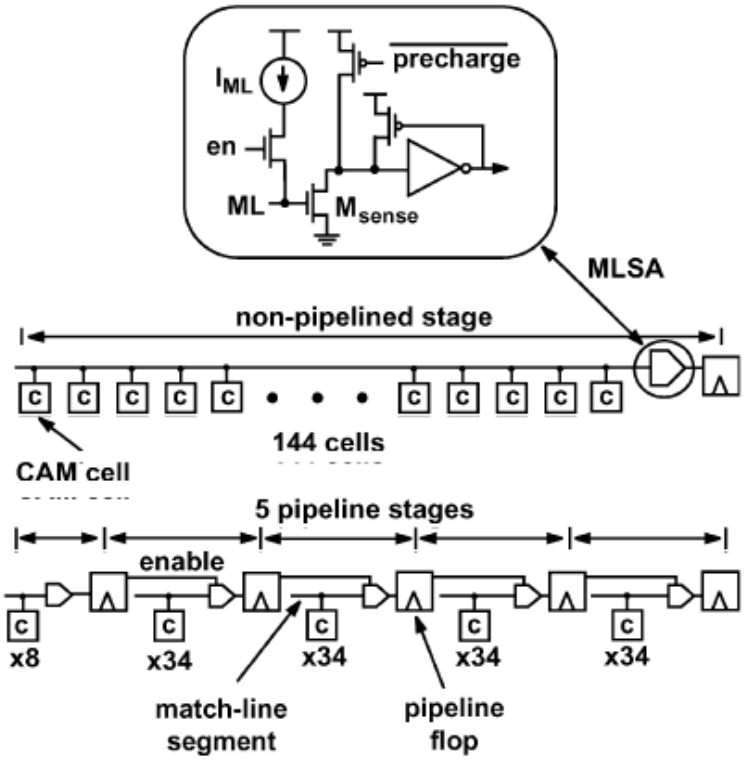

Fig.2: Non-pipelined ML vs Pipelined SL and MLSA schematic

- MLSA: Current-Based Match-Line Sense Amplifier
- MLSA is responsible for the ML precharge
- Dividing ML into segments prevent from charging the full Match-Line: an enable signal for charging a ML segment is given only if every stored data match with the SL data in the previous segment
- There is much power consumption due to flip-flop but it is compensated by power saving

Hierarchical Serch-Lines

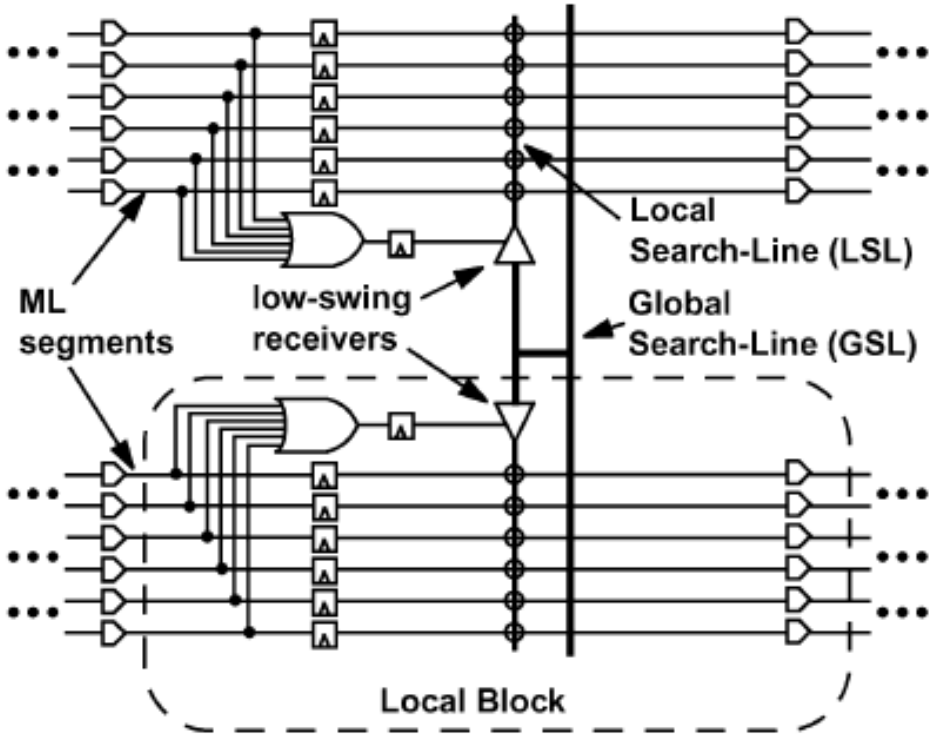

Fig. 3: Hierarchical SL simplified Schematic

- In order to reduce power consumption , data are broadcast on the Global SL using low-swing signaling
- Low-Swing receivers translate GSL signal to a VDD signal on the Local SL that will be compared to stored data
- An enable signal is sent to low-Swing Receivers only if at least one ML is in the Match State

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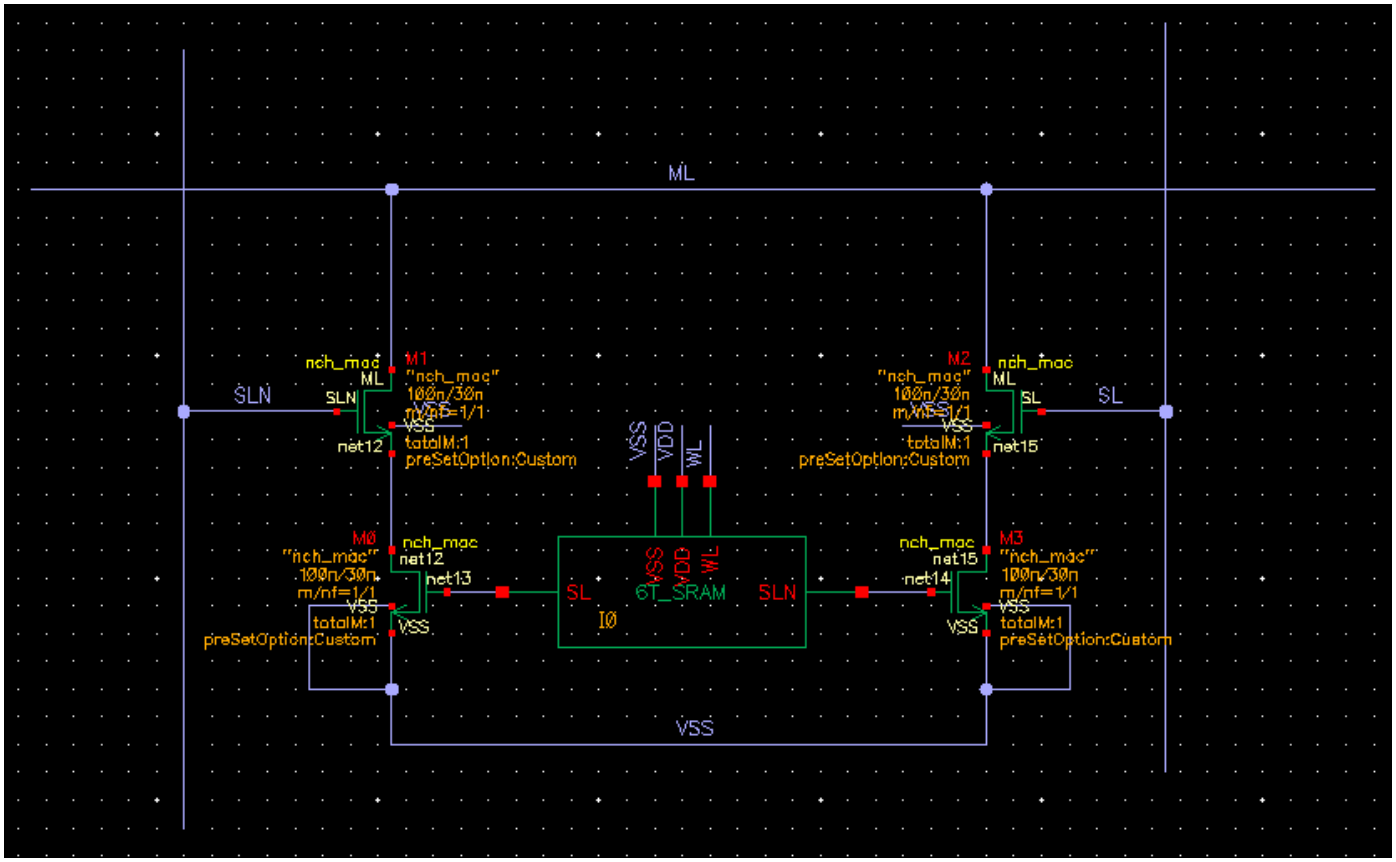
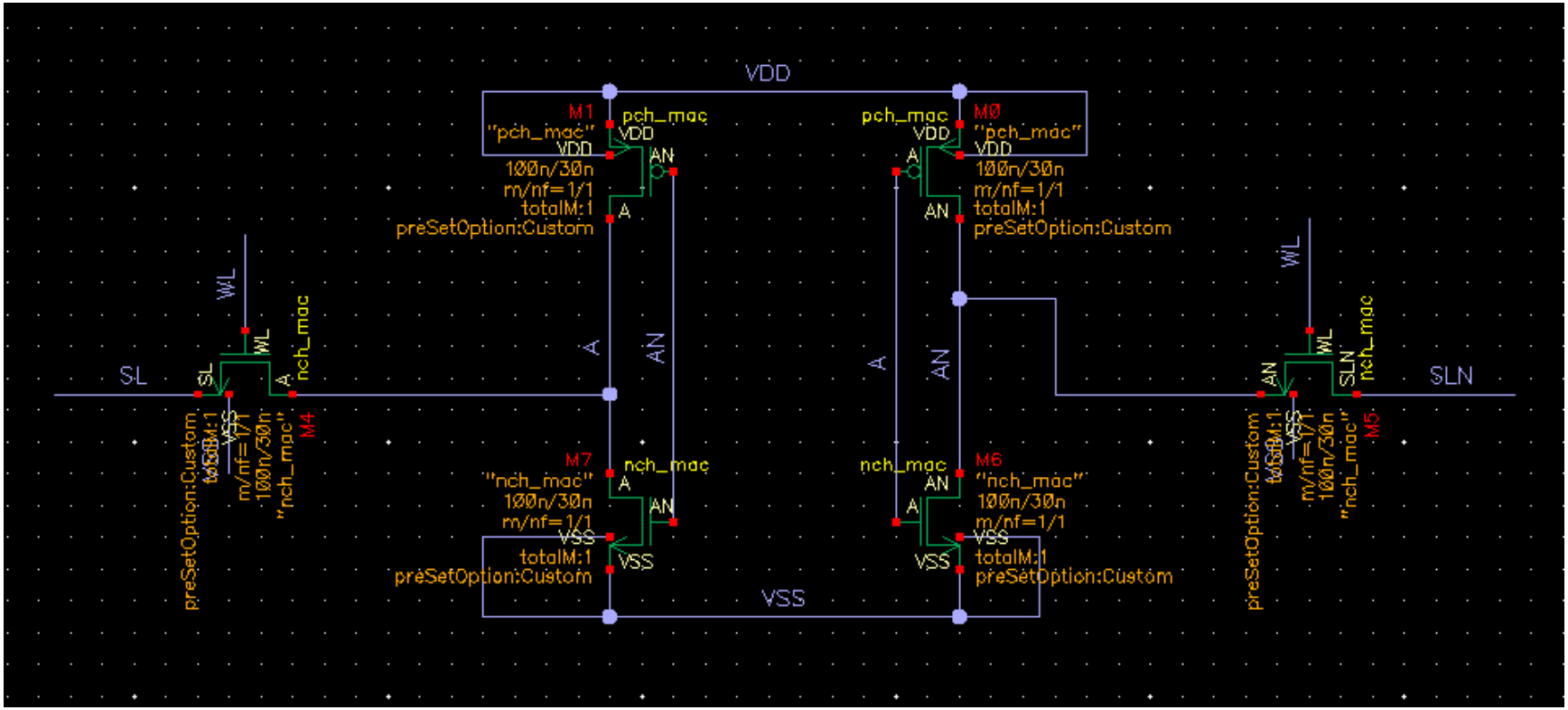
NOR CAM Cell Schematic



- 6T_SRAM is the previous called M
- NMOS: 4x nch_mac, W/L 100n/30n

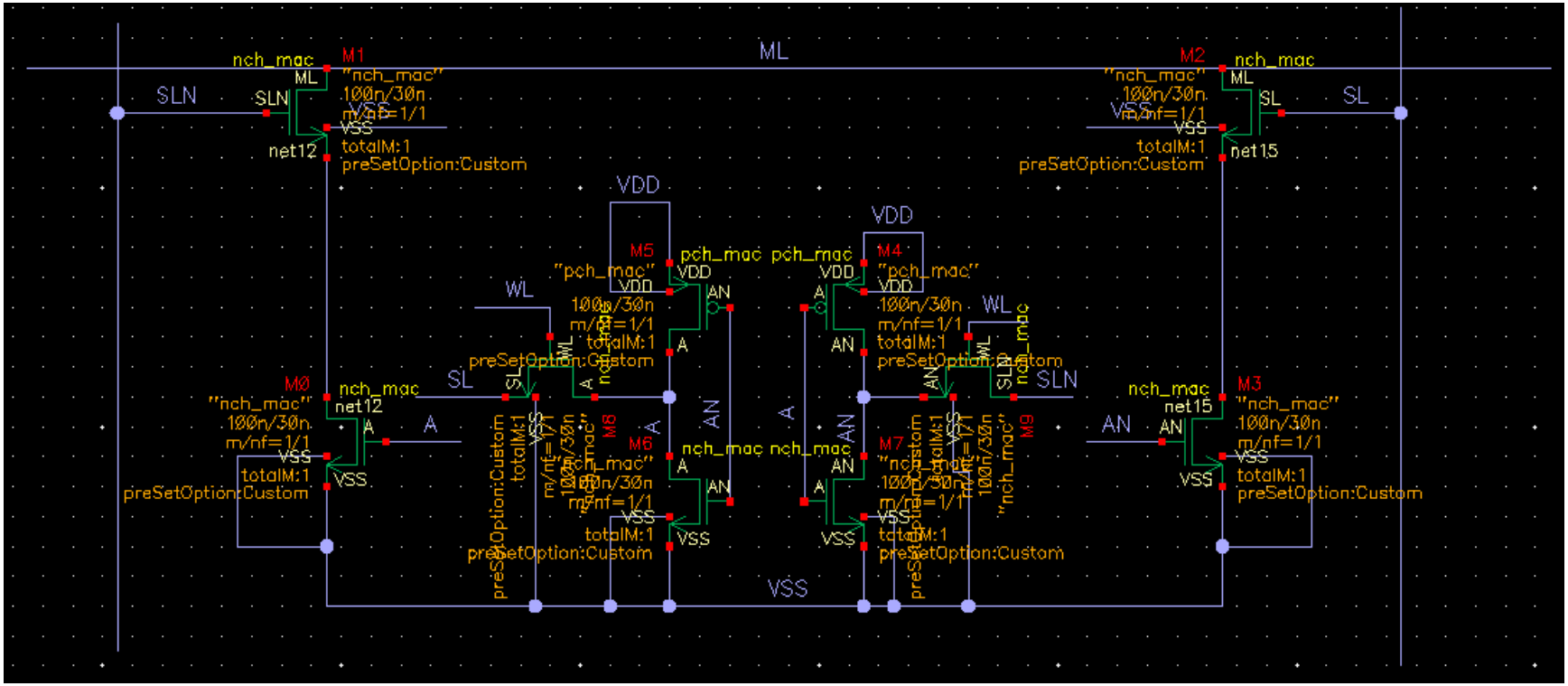
6 transistor SRAM Schematic



- PMOS: 2x pch_mac, W/L 100n/30n
- NMOS:4x nch_mac, W/L 100n/30n

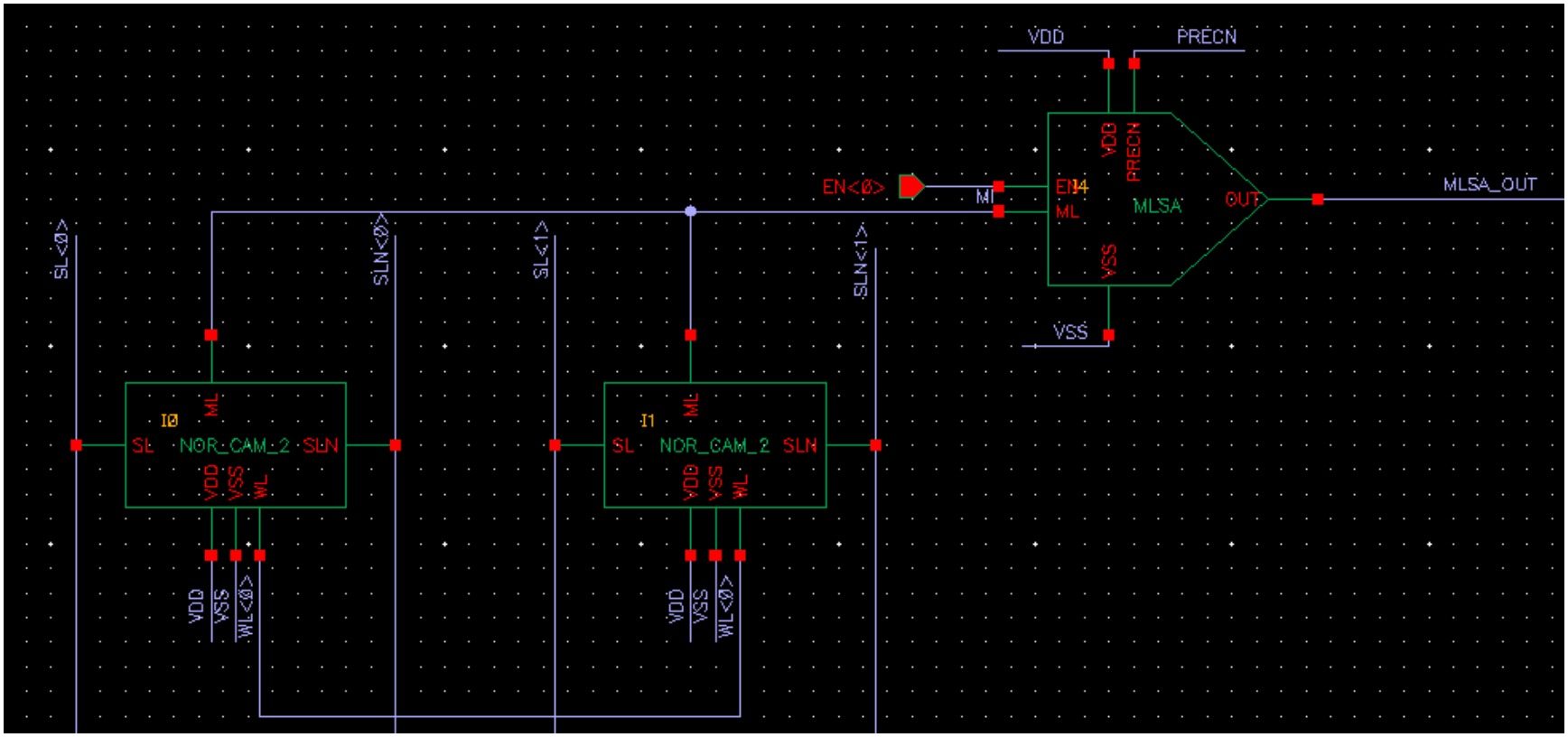
- READ-ONLY: Also if a Write line is shown it is not possible to change the stored data

NOR CAM Cell Schematic Modified



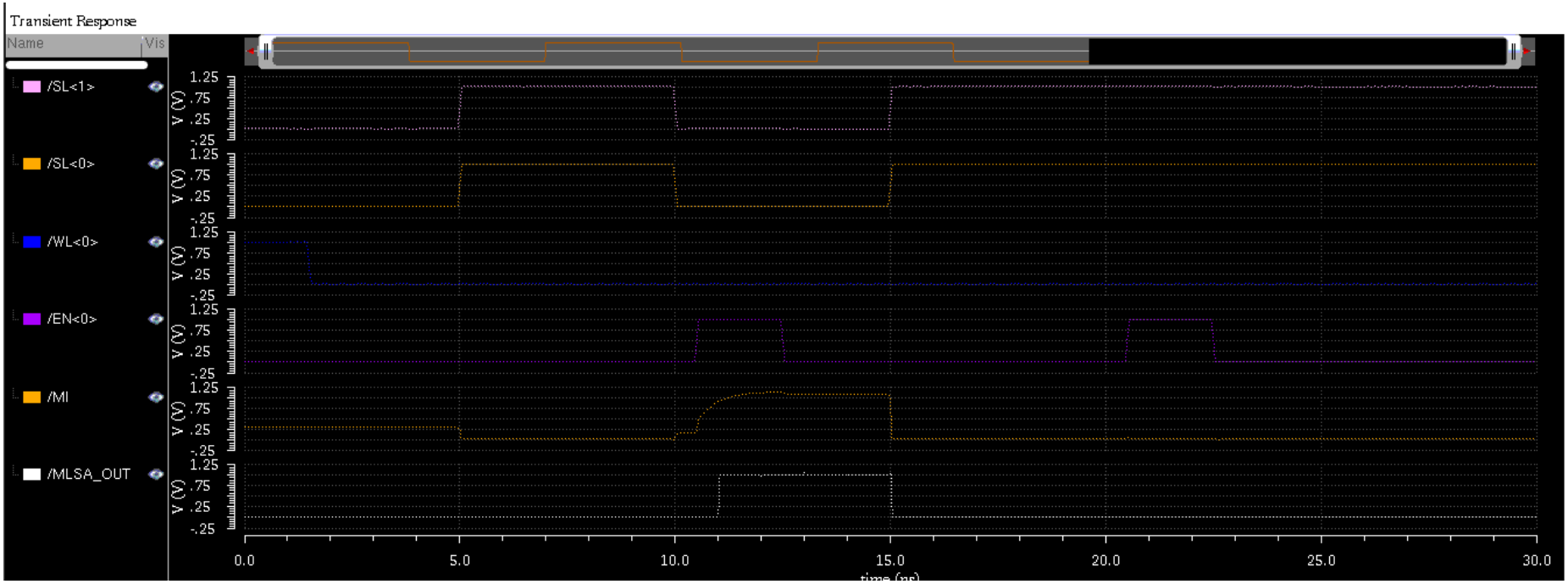
- WL transistor are directly connected with SL and SLN
- The second transistor in the NOR cell is connected to A and AN and it is not connected , as before, to the WL transistor
- READ and WRITE Memory cell

NOR CAM Simulation



- Simulation for 2 NOR CAM Cells modified and a MLSA
- Controlling WL it is possible to save SL's data in the CAM cells, then with an enable signal the ML is charged and stays charged if there is a match

NOR CAM Simulations



- Test for 2 NOR CAM and a MLSA in series.
- When WL is high SRAM cells memorise SLs data (00 in that case)
- EN is a signal that allows MLSA to charge ML
- ML stays high only if the data, that was stored when WL was high, matches with SLs data
- MLSA_OUT will become the ENable signal for the subsequent MLSA in a pipeline scheme

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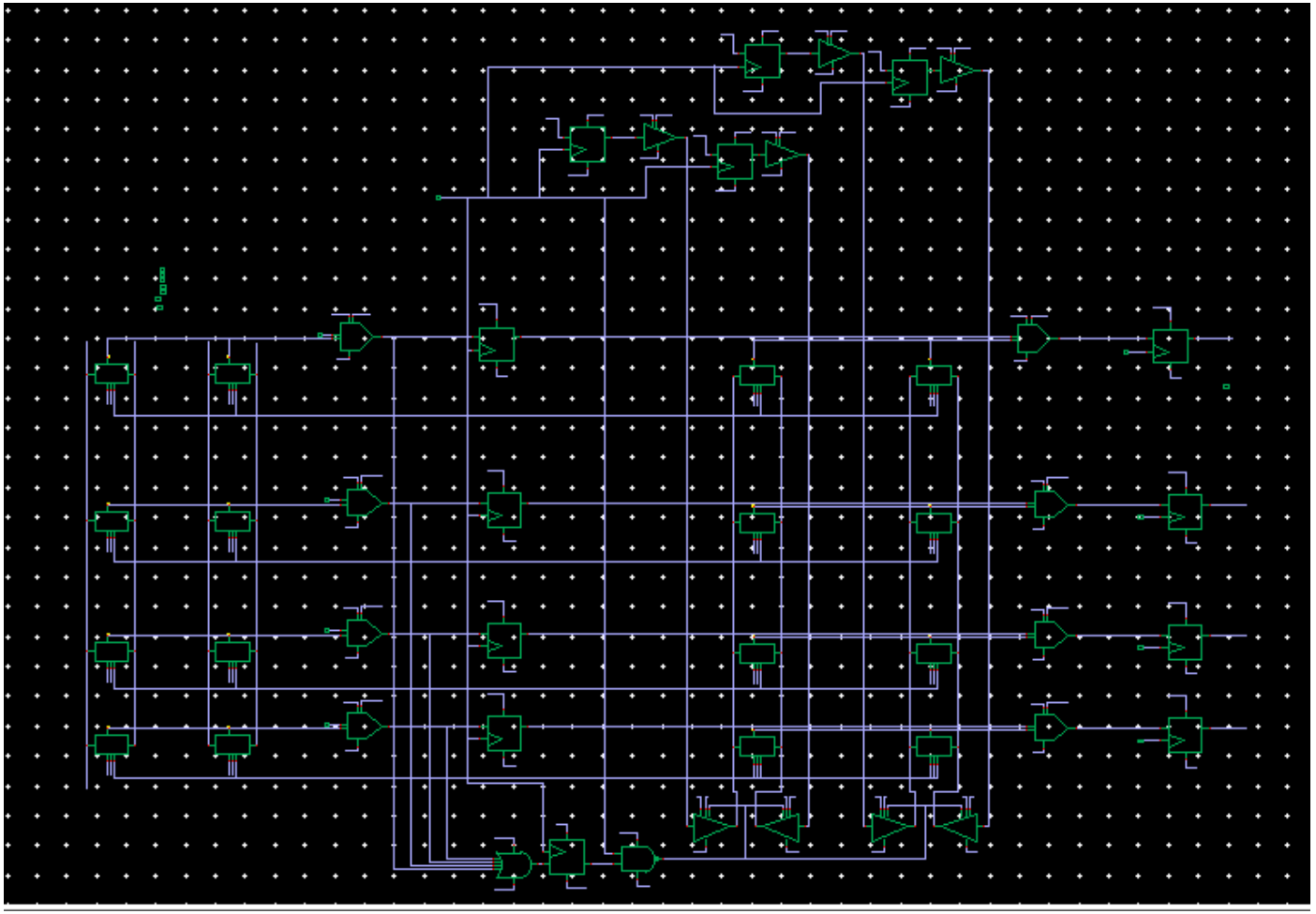
Present Status



Tests and simulations for a 4x4 bit CAM, divided into 2 pipeline and with 2 hierarchical SL

How we proceed:

- Simulations and tests conclusion for the 4x4 Cam
- Realisation of a bigger CAM: 1024x144???
- Tests, simulations and measurements for that CAM
- Layout
- Parasitic capacitors extraction and measurements

What we did:

- Schematics:
  - NOR CAM cells (with 6T-SRAM and Modified)
  - MLSA (Match-Line Sense Amplifier)
  - Low-Swing drivers and receivers for hierarchical SL
- Simulations:
  - Single and multiple CAM cells in series with MLSA
  - 3 pipelined ML of 2 CAM in series with MLSA and Flip-Flop
  - 4x4 CAM Matrix with 2 pipelined ML and 1 hierarchical SL

What we have to do:

- Simulations and tests for the 4x4 CAM with multiple hierarchical SL
- Realisation of a bigger CAM: 1024x144 bit???
- Tests, simulations and measurements for that CAM (rise and fall time vs clock frequency, dinamic and static power consumption vs frequency)
- Layout
- Parasitic capacitors extraction and measurements (area, rise and fall time, power consumption,...)