Content-Addressable Memory With pipelined hierarchical search scheme

- CAM Operations
 - Nor CAM Cells
 - Pipelined Match-Line
 - Hierarchical Search-Line
- Schematics
- Conclusions
 - Present status
 - How we proceed

- CAM Operations
 - Nor CAM Cells
 - Pipelined Match-Line
 - Hierarchical Search-Line
- Schematics
- Conclusions
 - Present status
 - How we proceed

NOR CAM Cells

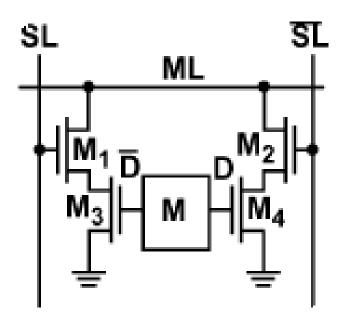


Fig.1: NOR CAM cell schematic

- CAM Compares search data in SL (Search-Line) with stored data D in M
- The Match-Line (ML) is precharged to VDD (ML=VDD match state)
- A mismatch between SL and D results in a series path from ML to ground (ML=0 Miss State)
- M is a 6 transistor SRAM

High power consumption for every Match-Line and Search-Line

Solutions:

- Pipelined ML
- Hierarchical SL

Pipelined Match-Lines

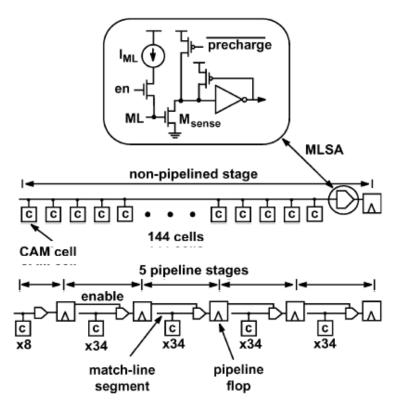


Fig.2: Non-pipelined ML vs Pipelined SL and MLSA schematic

- MLSA: Current-Based Match-Line Sense Amplifier
- MLSA is responsible for the ML precharge
- Dividing ML into segments prevent from charging the full Match-Line: an enable signal for charging a ML segment is given only if every stored data match with the SL data in the previous segment
- There is much power consumption due to flip-flop but it is compensated by power saving

Hierarchical Serch-Lines

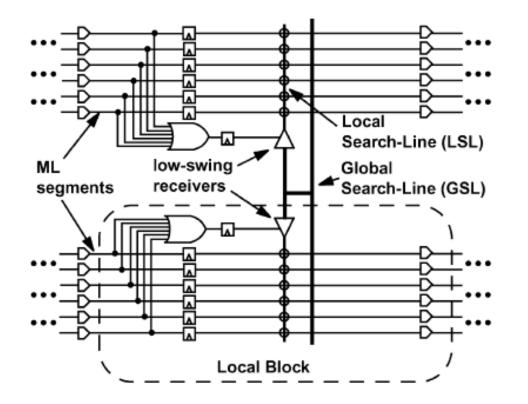
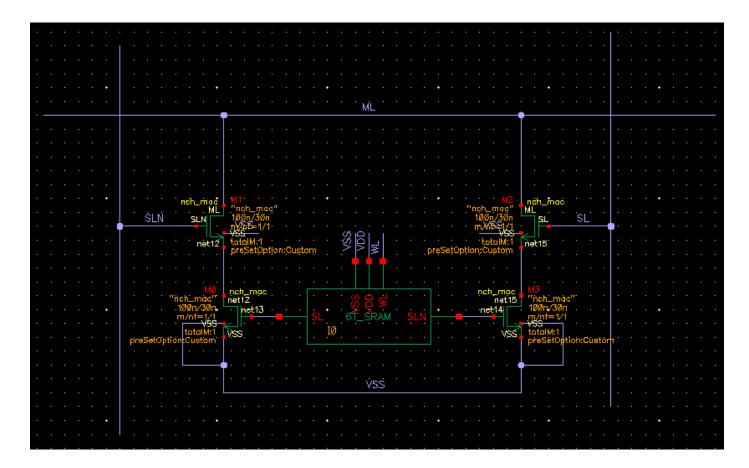


Fig. 3: Hierarchical SL simplified Schematic

- In order to reduce power consumption , data are broadcast on the Global SL using low-swing signaling
- Low-Swing receivers translate GSL signal to a VDD signal on the Local SL that will be compared to stored data
- An enable signal is sent to low-Swing Receivers only if at least one ML is in the Match State

- CAM Operations
 - Nor CAM Cells
 - Pipelined Match-Line
 - Hierarchical Search-Line
- Schematics
- Conclusions
 - Present status
 - How we proceed

NOR CAM Cell Schematic



- 6T_SRAM is the previous called M
- NMOS: 4x nch_mac, W/L 100n/30n

6 transistor SRAM Schematic

															·													•			,																										·			
																							•					٠v	DI	D.																														
• •																	Γ						₽														÷P		_				1																	
																		pċ	h_	m	M ac	1	k	pel /DE		m¢	IÇ						P	ich	<u>п</u> _1	nac VDI		M	0 pch	<u>i</u> n	na	c"																		
· ·																	L	1/	X(7)	-) - /	71) 3Ø1	<u></u>	7	٦	٨N	ł									٠A	1	4		DD ØØr	./3	ИЛ -		J																	
												•						m	√n	f=	17	1			٢	I									ľ	1L		m	e/m	Ē1	17-	1																		
																	ι.		ţo	ta	M:	1	ļ	Δ.												A١	1	to	otal reS	M:	Ĭ.																			
							1						P	reS	set	:Op	otn) D	CI	JSt	ton	n																Р	reS	etl	Jb	tio	ונח	JUS	tor	n														
							·																																											Ŵ	5									
· ·						1715 -	1		•																													_	•	•																				
· ·							·		. (ĕ .																											T																	ngo						
							·	WL		2												∢			AN											·	-															WL	_	2						
			SL			പ്പ			a Ì	2															4									Æ		ΔN	ζ												٨N				2	No!		SL	N			
				_		<u> </u>	- -	L	-													_	÷.																		L						 		-	Y		L	-				<u> </u>		-	
					Ę	14	\$ <u>8</u> _	ĝņ.	÷. :	4																																							8	- 8	X	Øп	20	Ş.						
· ·					sto :	闣	₹	2	βщ			•												•											ł			ы										1	89	1	Ĩ	2	Ë							
· ·					- ng	3	14	102	Ē								.0	nċ	Ь	m	ac'	ŭ.	• ,	nci A	n_	m	1¢						n	ch	-n	nac AN		1	net	i r	пà	ic"						ġ	33	ř,	/nt	<u>80</u> r	2							
					5		<u>.</u> Е	÷	'nc'									19	30		3Ør	П	Ľ	È	٨N										A	۱Ë	•	-15	ØØr	1/3	iØ,	1							Ë.		В	16	2							
					oti.				.								_	m	/n	f -	JL.	1																ņ	V/n	f=	1/	1						1												
					ę														to	tal	M:	1	Ń	/S\$,	vss	ই	ťc	otal	M:	1							- 5	3											
• •					Š								pr	eS	Set	Op	stic	n:	Cι	,et	M: tom	n	ľ	10,												γ ₂ .	1	р	reS	ieti	Ďр	tio	n;(Cus	to	m i		ų	ğ											
• •					5															•			I	•		•	•	•	A.	55	ì	•	•		•	·				•	•							1	ā											
· ·	•	•	+			•	•	•	•		•	•					•	•					•	+		•	•	•	•	•		•	•		+	•	•		•	•	•		•	•	+		•	•			÷			-	+			-		

- PMOS: 2x pch_mac, W/L 100n/30n
- NMOS:4x nch_mac, W/L 100n/30n
- READ-ONLY: Also if a Write line is shown it is not possible to change the stored data

NOR CAM Cell Schematic Modified

 •		•	•	•	·	•	·	•		S					÷	<u>s</u>									i.					•	•	•	·	·	•	•			•	•		•	Ľ	J							Ċ	
·			· n	ch	ma	c _	Mit																	ML	Ľ																	_ nc	:h	ma	c							
	. s	LN		S	M	L ·	‴п 1Ø лъ	ch. Øn, ⊈	_m /30 ≍1/	ac' in /1	•				•					•	·																, ,	nch 10 /£	ևո Øn Դnf:	100 (3Ø =1/	n. 1	ML	SL	ma		S	L				·	
·					net1	2	tot pr	S talN eSe	vi:1 etO	ptic	on:(Cus	iton	n																				рп	eSe	etO	ptic	t Sm:C	oto Jus	VS alM: stor	1	ne	t 1,5									
•																	ſ		DD	1								1	701	እ											j	•										
																			45		pch		na	ср	ch	n	nac	Γ	м4	, .]											i.											
													W	iL.	.")	pch	L h	nac VE	с" 20	¥	DD/	AN			·	N A	/00	Y.	"po VDI	h	ma 74	c''																				
• •]	10) m/	如宜	/ 59 (= 1,	9n /1			2				-0			-196 m/1 tot	hn∕. hf≕	50n :1/1 .4		WL.	mbo								•										
					MØ					ŀ	รเ	pn	eSe	tOp	y i i	εις 5π:Ο		sto	ie I Im		\				•	•	AN		pre	Set		tio		ģ	om SI	N.						M										
•			"ncl 19	h_n ∭n	nac' /30r		net		mai	: 			.е т	<u>у</u> .ф					~	•	A N I	AN		i i	A	Ì	N	•		.E '	_γ ∵են		یّا 5.5	Ð		_ ·	Д	, nk N		nno 1et1 NILL	с 15	" .1(nch ØØr	Lm 73(iac' ðn	1						
			T	/nf:	=1/1 VSS	÷,	_	·	·)ustoi htalM			5 ŏ Ech	i -≥ i⊢n	i M mar	16 c"		nch A	1_ri	na	ç n	ch.	-m	t⊃ 100 AN		M7 "n(<u>f</u> isto	N R R	「二氏に									4		/nf SS	=1	/1 ר ר							
•	preSe	rtOpt	ión	Cus	stom	•	VSS	3.					ion:0 4		201	äefi my	ðn, nf	/32 =1,	ðп /1			AN				A			1Ø0 m/	紀/: [型=	50r = 1/1		"nch							.V5	5\$	тс рі	reS	м: I et0	pti	on:	Cus	iton	'n			
				•	·	_•						DI	e topt	fOr	stin	t m-f	ote	alM stor	55 1:1 m	K	/sˌs					Ň	vss		tot pre		:1 106	tio	n:Ci	uet	am																	
													preS	·										V	ŚŚ	5				preS																						
						. L								•						•								•	•			•																				
•																																																				

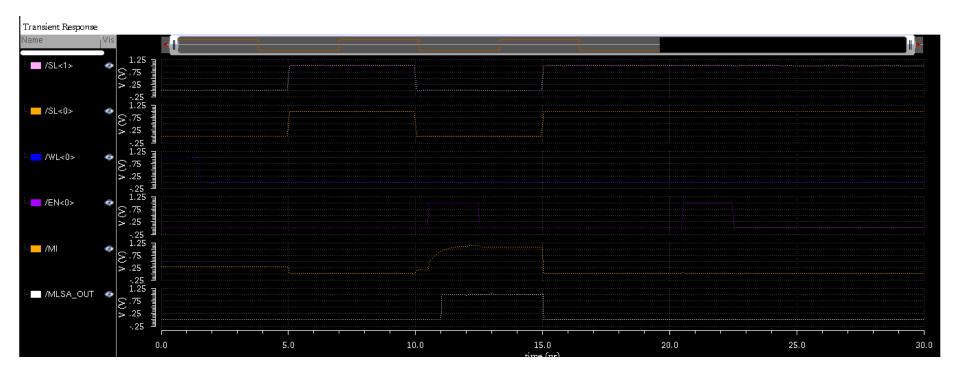
- WL transistor are directly connected with SL and SLN
- The second transistor in the NOR cell is connected to A and AN and it is not connected , as before, to the WL transistor
- READ and WRITE Memory cell

NOR CAM Simulation

• •			Ý TRÉCNÍ TRÉCH PRÉCNÍ TRÉCH PRÉCNÍ TRÉCH
• •			
	· · · · · · · · · · · · · · · ·		······································
• •		<u> </u>	MLSA_OUT
< Ø>	;	\$;	· · · · <mark>,</mark> · · · · · · · · · · · · · · · · · · ·
× 2	⊻	(· · · · · \ · · · · · · · ·	· · · · · 🖓 · · · · · · · · · · 🖗 · · · · 🖌 · · · · · · · · · · · · · ·
· ਯ	<u>.</u>	י י י י י י שוֹן י י י י י ו	· · · · Z · · · · · · · · · 🎽 · · 🖌 · · · · · · · · · · · · · · · ·
			
	<mark>.</mark>		i i i i i i i i i i i i i i i i i i i
• •	· · 10 · · · · · · ·		
• •	SL · NOR_CAM_2 · SLN	📫 · · · · · · · 📫 — SL· NOR_CAM_	2 SLN
• •	· · · · · · · · · · · · · · ·	······································	<mark> </mark>
	· · · · ·	· · · · · · · · · · · × ≯≫≱	<mark> </mark>
	· · · · · · · · · · · · · · · · · · ·		
	· · · · · · · · · · · · · · ·	<mark></mark>	
	· · · · <u></u>		
• •	· · · · · · · · · · · · · · · ·		
• •		· · · · · · · · · · · · · · ·	
	· · · · · · · · · · ·		

- Simulation for 2 NOR CAM Cells modified and a MLSA
- Controlling WL it is possible to save SL's data in the CAM cells, then with an enable signal the ML is charged and stays charged if there is a match

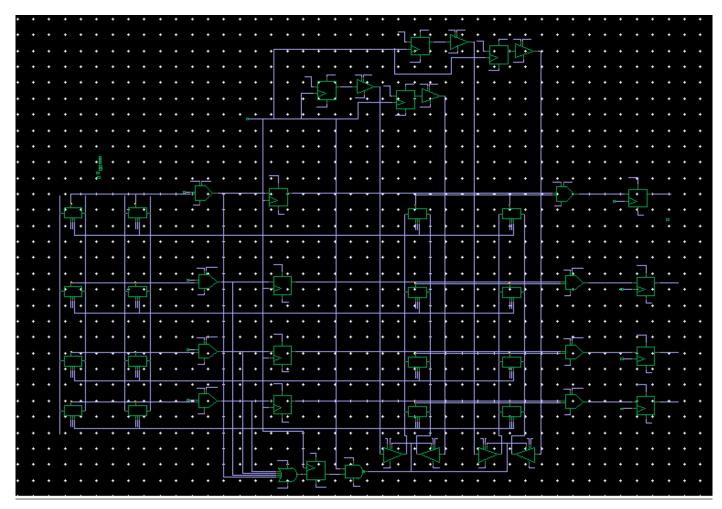
NOR CAM Simulations



- Test for 2 NOR CAM and a MLSA in series.
- When WL is high SRAM cells memorise SLs data (00 in that case)
- EN is a signal that allows MLSA to charge ML
- ML stays high only if the data, that was stored when WL was high, matches with SLs data
- MLSA_OUT will become the ENable signal for the subsequent MLSA in a pipeline scheme

- CAM Operations
 - Nor CAM Cells
 - Pipelined Match-Line
 - Hierarchical Search-Line
- Schematics
- Conclusions
 - Present status
 - How we proceed

Present Status



Tests and simulations for a 4x4 bit CAM, divided into 2 pipeline and with 2 hierarchical SL

How we proceed:

- Simulations and tests conclusion for the 4x4 Cam
- Realisation of a bigger CAM: 1024x144???
- Tests, simulations and measurements for that CAM
- Layout
- Parasitic capacitors extraction and measurements

What we did:

- Schematics:
 - NOR CAM cells (with 6T-SRAM and Modified)
 - MLSA (Match-Line Sense Amplifier)
 - Low-Swing drivers and receivers for hierarchical SL
- Simulations:
 - Single and multiple CAM cells in series with MLSA
 - 3 pipelined ML of 2 CAM in series with MLSA and Flip-Flop
 - 4x4 CAM Matrix with 2 pipelined ML and 1 hierarchical SL

What we have to do:

- Simulations and tests for the 4x4 CAM with multiple hierarchical SL
- Realisation of a bigger CAM: 1024x144 bit???
- Tests, simulations and measurements for that CAM (rise and fall time vs clock frequency, dinamic and static power consumption vs frequency)
- Layout
- Parasitic capacitors extraction and measurements (area, rise and fall time, power consumption,...)