AM07a & AM07b Test Board

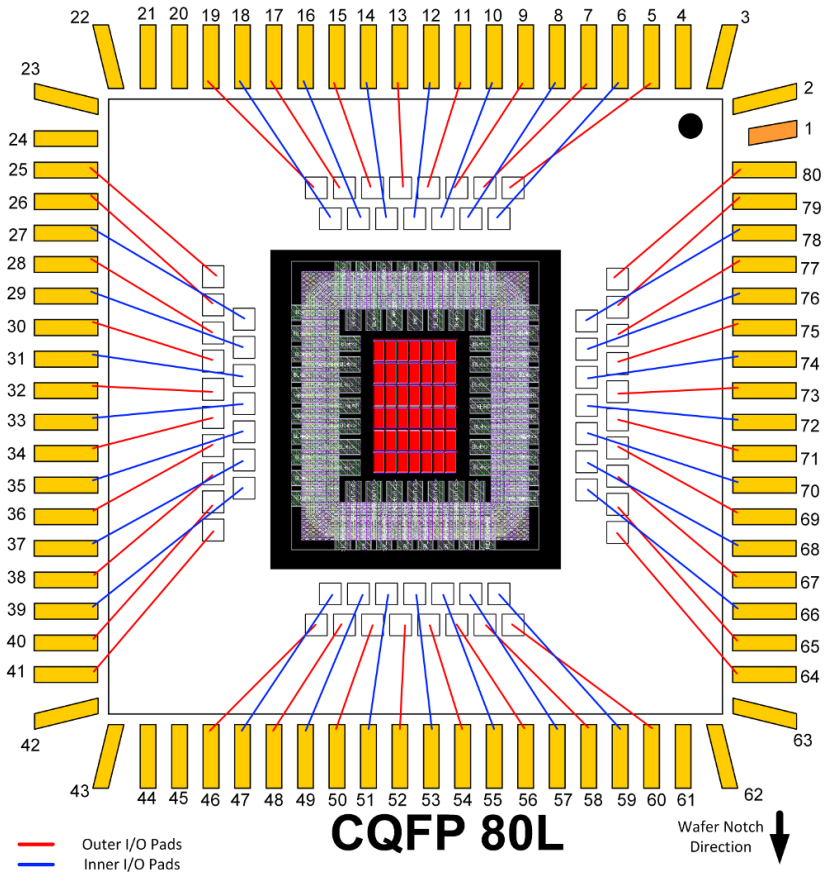
F. Crescioli, O. Le Dortz, P. Bailly, A. Vallereau

(LPNHE - IN2P3 - CNRS)

2/10/2015

AM07a tests objectives

- Verify the functionality of the CAM layer in 28 nm technology
- Characterize power consumption vs speed
  - The target is 200 MHz
  - Optional: measurements up to 500 MHz



$18 * 2 = 36$ high speed input lines + clock + slow control lines

AM07a Test Board

Conceptually a very simple board:

- HPC FMC mezzanine (160 signals available)
- a clam shell test socket for the AM07a CQFP80L package
- a power connector for external power supplies to track power consumption

The FMC test board will plug into an FPGA kit with an ethernet connector that will act as interface / buffer for the tests.
Conceptually it is the same setup that we used for the AM04/AMmini@sic/AM05 (and AM06 soon).

AM07a Test Board Issues

- **Issue:** CQFP80L test socket has been ordered (25/9) but it isn't in stock, we have to wait 8 weeks
- **Solution:** we'll produce a test board without the test socket and solder the chip. It is reasonable to be able to test few chips with this board. We'll produce a second test board later with the test socket to accumulate statistics on the remaining chips.

AM07a Test Board Issues

- **Issue:** AM07a has 1.8 V LVCMOS IOs not tolerant to 2.5 V, on our dear HTG V6 FPGA board it isn't possible to configure the all needed signals on the FMC connector to 1.8 V LVCMOS
- **Solution:** We'll use another FPGA kit. We verified that the KC705 board and a Zynq board that we have here in Paris are compatible. The KC705 board is available also in Milan. There's more work to do on the firmware side since we can't exploit directly the old AM test firmware for the HTG V6

AM07a Test Board Issues

- **Issue:** to go at 200-500 MHz with LVCMOS18 signals it is necessary to have well adapted lines. A standard 50 ohm termination to gnd requires 36 mA while the IO pads on our FPGA kits can drive up to 24 mA.
  - A termination in series should be near the input, but we can place it just at the FMC connector, about 4 cm away from the FPGA. SPICE simulations shows that this is not a good solution.
  - Some IO pads of the FPGA have an internal termination in series, but not the type that is connected to the FMC
- **Solution:** place a termination at VTT=0.9 V using a stable source (LP2995)
- **Remaining issues:**
  - This way we'll need 18 mA per signal. Our FPGA kit will it be capable to drive 36*18 mA links at >200 MHz on the same bank?
  - Preliminary SPICE simulation shows that at 8 cm (FPGA to AM07a) it will be hard to reach 500 MHz

AM07a Test Board Issues

- **Issue:** to go at 200-500 MHz with LVCMOS18 signals it is necessary to have well adapted lines. A standard 50 ohm termination to gnd requires 36 mA while the IO pads on our FPGA kits can drive up to 24 mA.
- **Alternative solution:** use LVDS from FPGA to near the AM07a and then LVDS $\rightarrow$ LVCMOS
- **Remaining issues:**
  - Very limited set of choices for LVDS $\rightarrow$ LVCMOS transceiver to go over 250 MHz
  - The few rated transceivers for 600 Mbps are LVCMOS33, we need a divider
  - The transceiver add a significant skew ($\sim$400 ps), at 500 MHz we might be in trouble

AM07a Test Board Issues

The design of the schematics is going on well, but our layout expert has taken a much needed 3 weeks vacation.
He will be available starting from the last week of October.
We currently don't have an alternative in our lab, we'll have to wait for him to complete the board and then send to production.

AM07a Test Issues

- The firmware/software to execute the tests is much less complex with respect to previous AM tests
- Nevertheless there is a certain amount of code to be written (expecially if we go to the Zynq)
- Our “tradition” is to write a significant share of code during tests, but if help is available we could prepare it in advance!

Let's talk about AM07b ...

Take all the issues of AM07a and multiply by an order of magnitude.

- ∼300 signals: it is not possible to use a single HPC FMC connector, but the KC705 has the other FMC connector as LPC and the Zynq board has only one connector. Maybe the Ultrascale board in Pisa? But that board is dedicated to other developments
- it would be much better to have the possibility to optimize the signal distributions over the FPGA banks to avoid driving limits. With an FPGA kit we are limited to what the kit designers did with the FMC connector connections

Solution:

build a test board with one (or more) FPGA on board.

- FMC mezzanine (using MGT to transfer data from host to mezzanine) ?
- stand alone board?
- “expensive” but more similar to the future multi-package (i.e. with the Zynq or Kintex)
- “cheap” but safe (i.e. with more than one little FPGA to drive the busses, 2x or 4x Spartan6 or Lattice ECP5)