# introduction

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# Main work packages

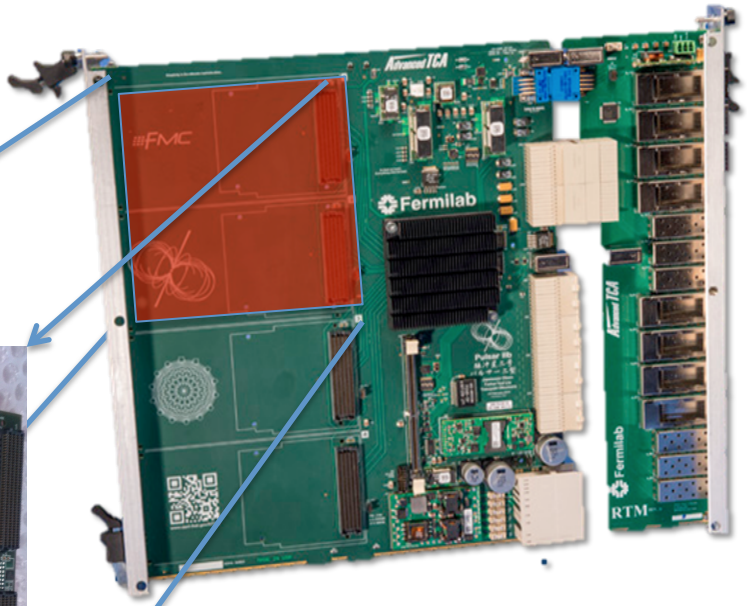
- Build 28nm prototype AM chips
- Multipackage AM chips with FPGA
- Build a ATCA demonstrator
  - Finding real tracks

# Common HW Model for Phase-II Track Triggers

ATCA


32 AM chips/slot

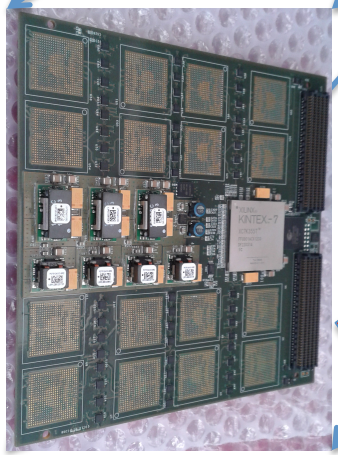
FTK Data Formatter




http://www-ppd.fnal.gov/ATCA/

future AM chip


x16



**16 AM chips**
**1 FPGA**
**RAM**
**Power modules**

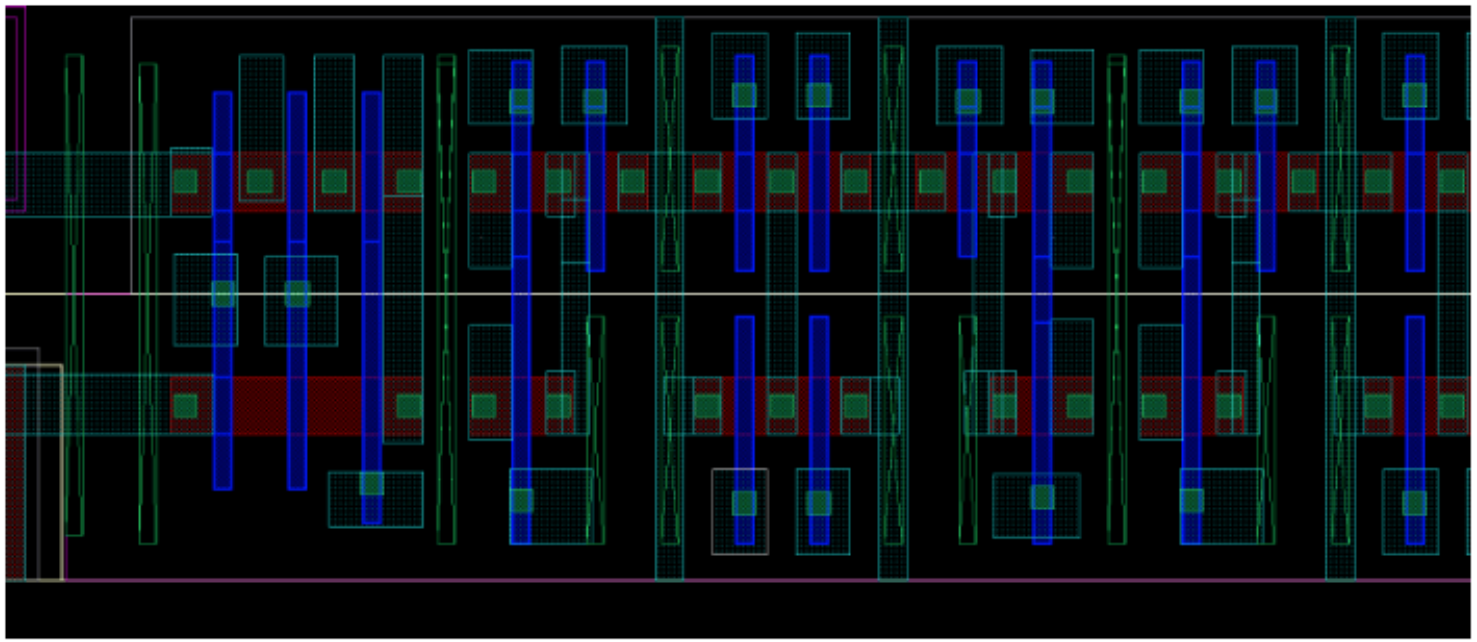
Pattern recognition mezzanine
D. Magalotti et al (RDfase2)

https://indico.cern.ch/event/299180/session/11/contribution/38/material/poster/0.pdf

# Power estimate

- "Standard" upper limit 400W / ATCA slot
  - 500 W/slot also mentioned. I'd rather not assume this for now
  - Note that 400-500 is per slot, not just the front mezzanine part
- Reserve 100W for the mother board
  - Max 150W per mezzanine (2 FMC per mezzanine)
    - Too much for cooling?
- AM06 power 2.4-3W/chip (128k patterns) 100MHz
- AM2020 assume 512k patterns 200MHz
  - Power 8*AM06 * 28nm reduction (70%) = 13-17W !!!
- Mezzanine power
  - 16 AM2020 → 200-250W
  - Ext RAM and 1 FPGA @ XX Watts
- Goal save another factor of 2 in power!

# Primi confronti AM06-AM07a (sim)



| | | AM04 | AM05 miniasic | AM06 | AM07 | AM06 vs AM07 |
|---|---|---|---|---|---|---|
| main block size | size (um^2) | 27798 | 26388.72 | 21833.28 | 6925.8896 | 31.72% |
| | length (um) | 226 | 257.2 | 100.8 | 110.32 | 109.44% |
| | height (um) | 123 | 102.6 | 216.6 | 62.78 | 28.98% |
| SIM power | uW/layer | 1.07 | | 1.91E-06 | 1.30E-06 | 68.12% |
| BL capacitance | pF/line | 0.07 | 0.06 | 0.027 | 0.018 | 66.67% |

Size. Real size 0.9*0.9~=25%

Power/MHz/bit

# 28nm chips

- Test AM07a
  - Required before starting/completing AM07b design
- Order AM07b now
  - LPNHE + LNF
- Define the AM07b interface
  - Logic
  - Physical

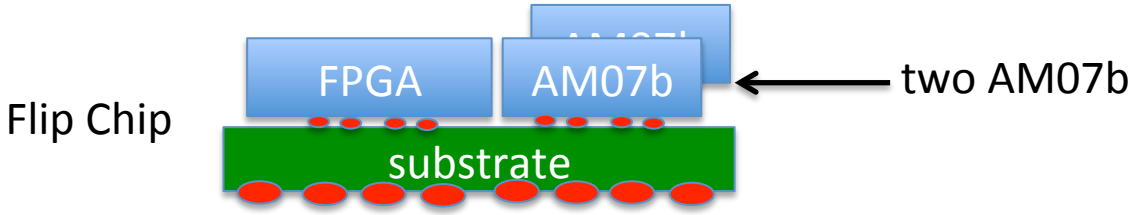
# 28nm chips

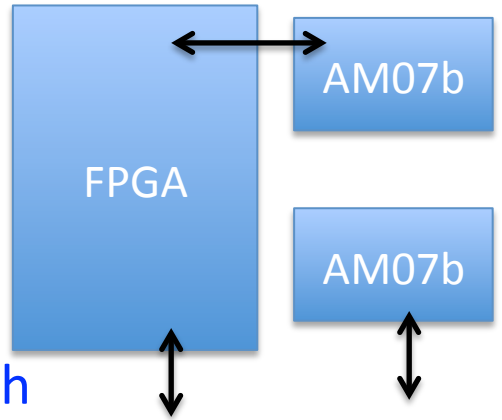
- AM07b goals:
  - Improve power consumption (pattern density secondary goal)
    - Show that 28nm is the right technology for phase-II
  - A fully working chip usable for finding patterns
  - Packable with the FPGA
  - >=200MHz do not limit ourselves to 200MHz
  - Submission March 2016?
- Follow up with AM08 as final device for this R&D
  - Goal: all features tested with AM07b
  - Bug fixes in AM08 if any.
  - Add potential improvements in AM08 using only a fraction of the area

# FPGA + AMchip system in package

Explore multipackaging

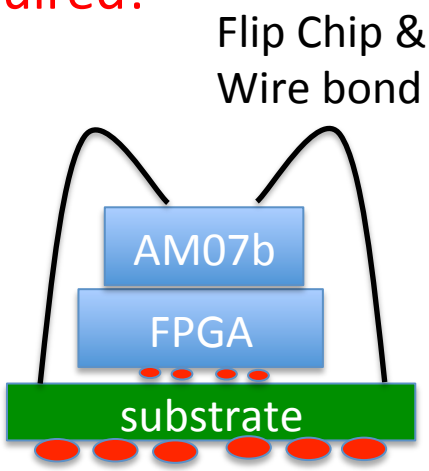
– 1 or 2 AM chip + 1 FPGA in the same package

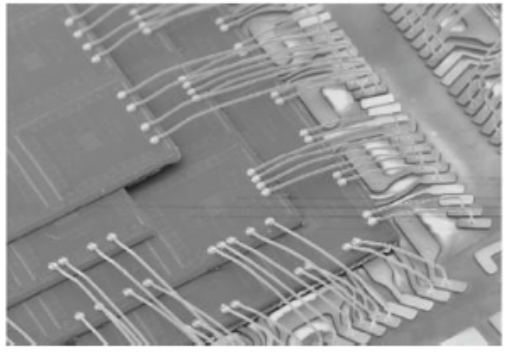



- Dramatically increases AM to Track Fitter bandwidth
  – "Through Silicon Vias not required!"

- No need to buy new SerDes IP
- Reduce FPGA-AM latency
- Simplify the AM development
- Increase fitting power/AMchip



# Multi package questions

- Fully flip chip?
  - In this case, AM07b tested only with multipackage!
- Mixed flip chip (FPGA) and wire bond?
- Thermal dissipation?
- Power consumption for FPGA?

- Multipackage pinout?
  - Pin compatibility with another FPGA?
    - E.g. Kintex7 355 (same as pattern reco mezzanine)
    - Need to chose one FPGA sharing same voltages…
    - Need same ball grid “foot print”
    - We can drop this requirement if problematic

# Multipackage

- Study multipackage options
  - Place dies on a naked PCB (no package)?
    - Interesting for prototype
- Place multipackage order in 2016 (?)

- Purchase of FPGAs
  - Choice?
  - When do we need them?
  - Ordering now. We need safe “storage”