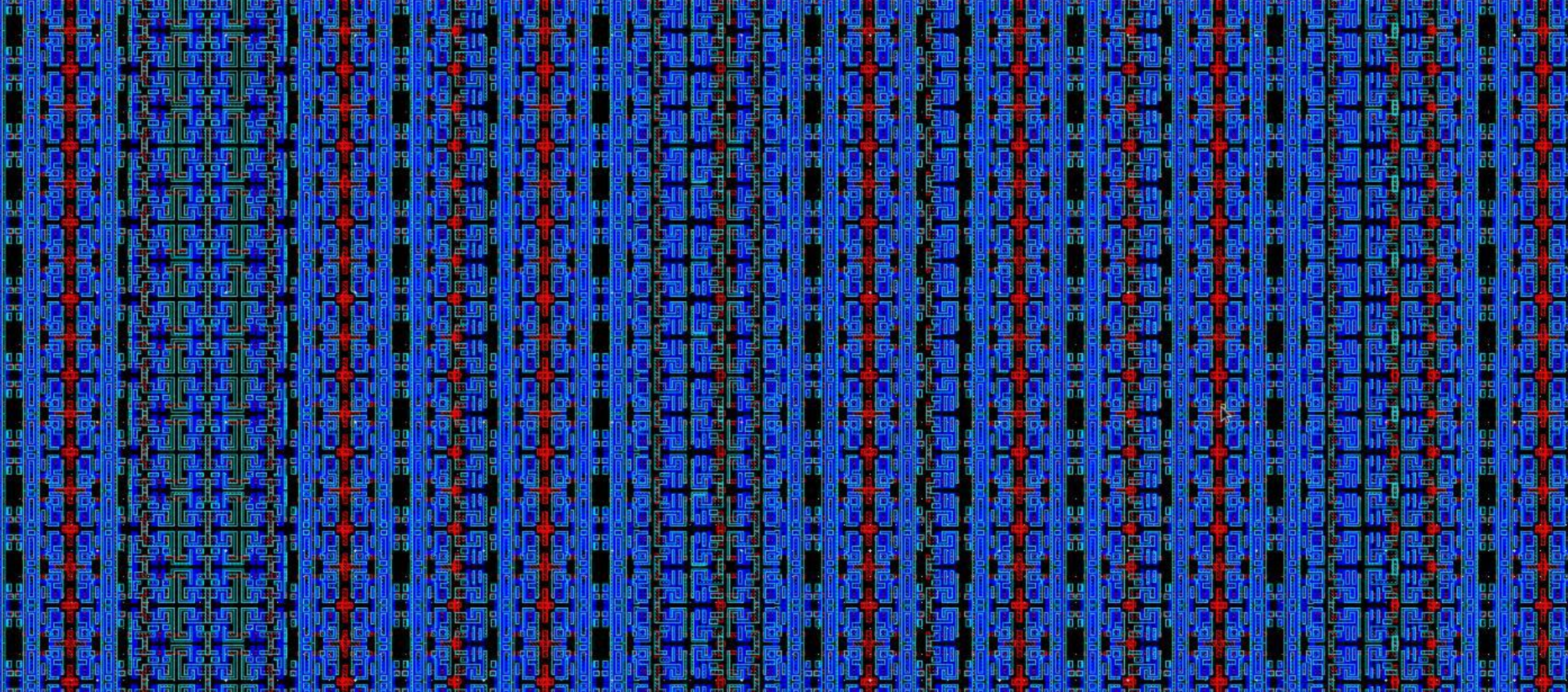
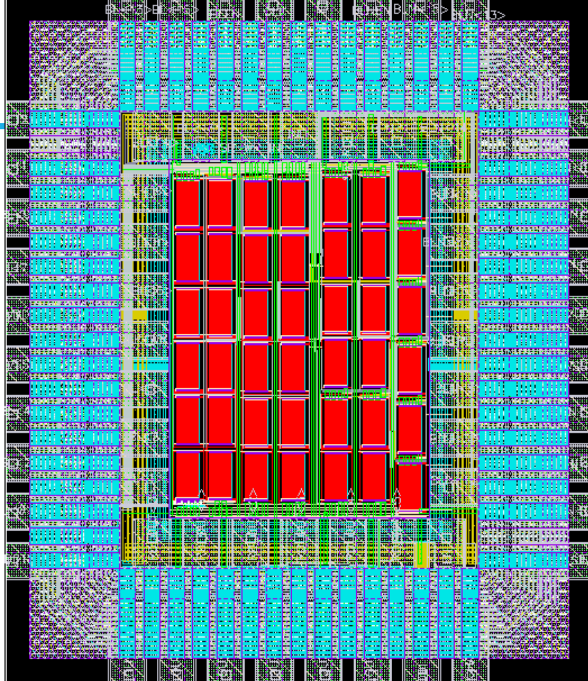


INNOVATIVE MULTI-CHIP SYSTEM FOR MULTI-PURPOSE PATTERN RECOGNITION TASKS (IMPART)

Alberto Stabile

Oct. review

AM CHIP DEMONSTRATOR



A new little **AM07a already** designed in June 2015

- **Silicon area:** 0.6 mm^2
- **Memory depth:** ~50 kbit (336 patterns)
- **Main aim:** characterize performance technology at 28 nm
- **Characterization** in Milano in Nov 2015

Next chip: AM07b will be submitted in Feb 2016

- **Memory depth:** ~5.5 Mbit (38 kpatterns)
- **Mixed approach:** full-custom + standard cells
- **Improve power save:** New cell tech

After 2017-2018: new larger chip AMCHIP2020

(i.e., 0.5 Mpatterns of 8×16 bits)

AM07B WIRE BOND

Area: 10 mm^2

Memory depth: 5.48 Mbit (38 kpatterns)

Architecture: two independent AMCORE

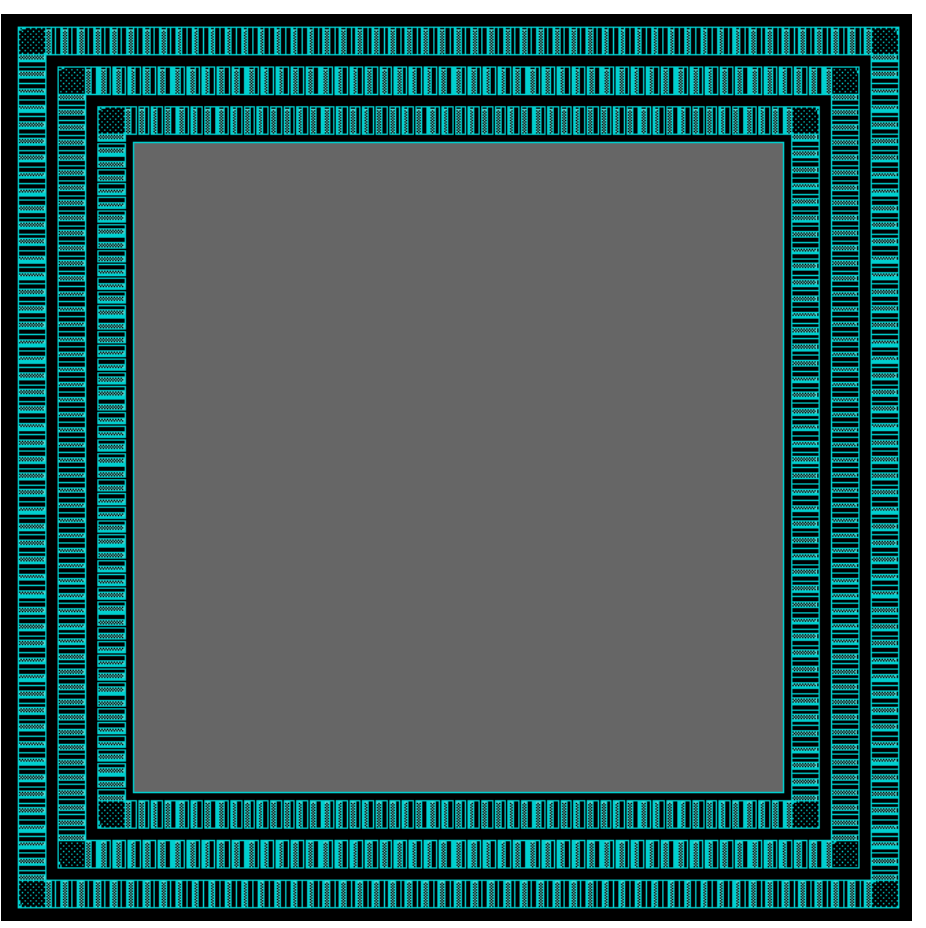
- First core for XORAM
- Second core for new low power cells

598 pads (PAD50GU)

- 347 signals – 251 power

Ext. cost 97 k€

Core area 2600 um x 2600 um



AM07B FLIP CHIP

Area: 10 mm^2

Memory depth: 5.48 Mbit (38 kpatterns)

Architecture: two independent AMCORE

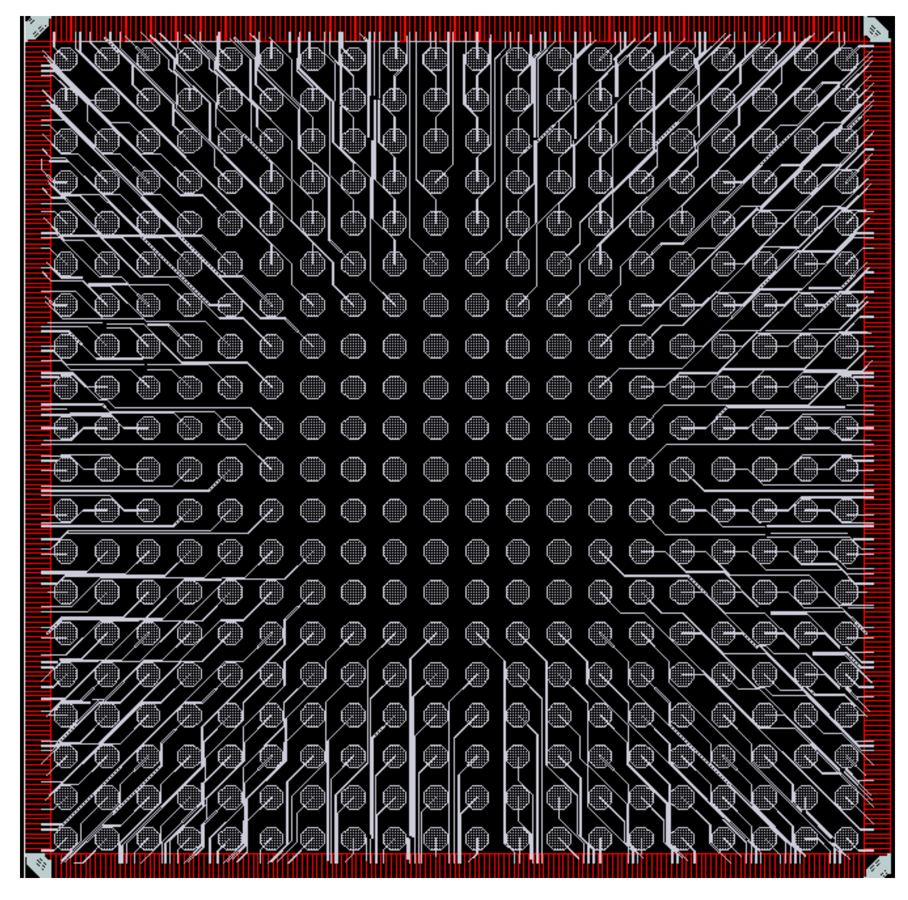
- First core for XORAM
- Second core for new low power cells

400 bumps

- 347 signals bumps – 53 power bumps

Ext. cost 97 k€ + 10 k€ for the bumps

Max current density at 125 degrees: 4.19 A



AM07B OPEN QUESTIONS

More signals IO cells? Not compatible with Zynq 100

How many cells?

- AM07a XORAM design by Alberto & Federico
- XORAM optimized by Alberto & Luca
- NOR cells studied by Marcello & Federico

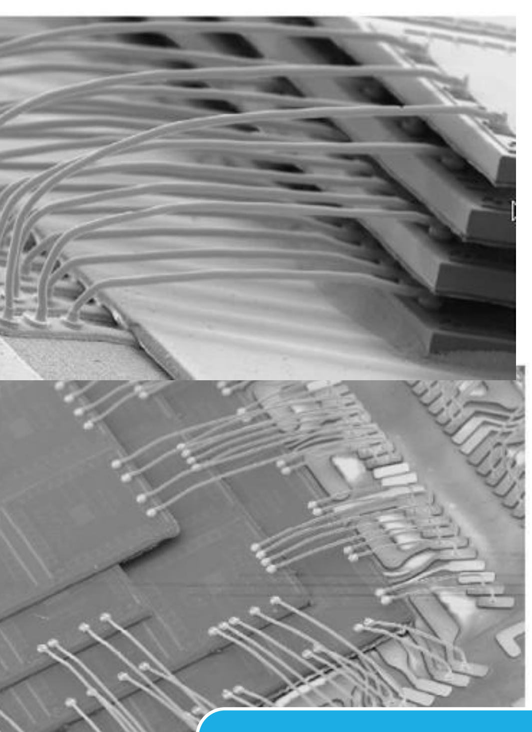
Package & bonding method:

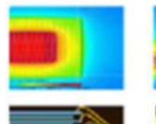
- Flip chip?
- Wire bonding?

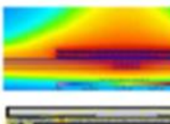
FPGA choice:

- Kintex 325T
- Zynq 100
- Ultrascale?

MULTI PACKAGE AND POWER CONSIDERATIONS







3D assembly technology **studies:**

- **Choose technology** which optimize power consumption
- Electrical and thermal **3D simulations** needed
- **Design and test** of the package
- Milestone & deliverable in Work Package 2 (WP2)

Support by **IMEC** (a micro- and nanoelectronics research center with headquarters in Leuven, Belgium)

- **broad expertise** in multi-chip package technologies

Demonstrate potentiality: AM chip v.7 consuming **less than 0.3 W**

In the future, larger area AM chip will have a still manageable consumption of a few watts **(less than FPGA power consumption)**

MULTI PACKAGE STUDIES

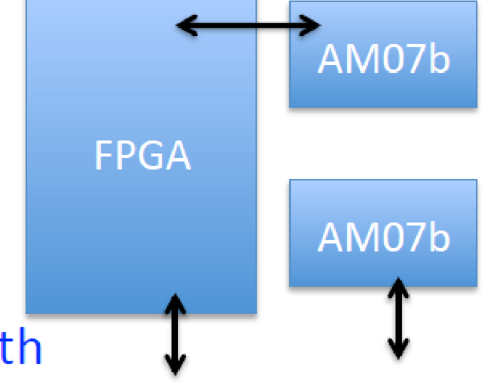
Explore multipackaging

- 1 or 2 AM chip + 1 FPGA in the same package

Flip Chip

FPGA AM07b ← two AM07b

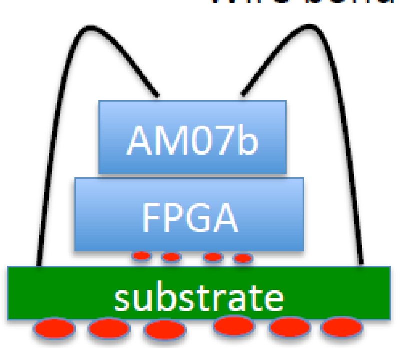
substrate

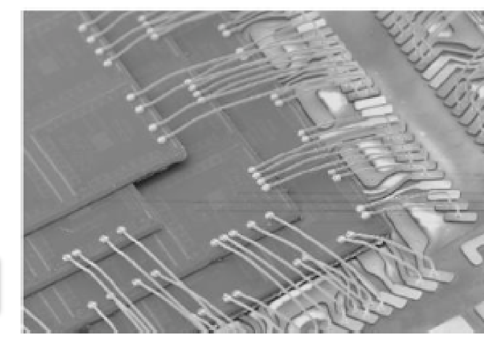


- Dramatically increases AM to Track Fitter bandwidth
  - "Through Silicon Vias not required!"

Flip Chip &
Wire bond

- No need to buy new SerDes IP
- Reduce FPGA-AM latency
- Simplify the AM development
- Increase fitting power/AMchip





FPGA COSTS

	Maximum Price	Minimum Price	Difference	Die Price	Ext die price (with the avg of package prices: 28% of minimum price)	Ext die price (with the avg of package prices; 22% of max price)
XC7A100T-DIE0628	$242.00	$183.00	76%		$51.24	$53.24
XC7K160T-DIE4058	$409.00	$198.00	48%		$55.44	$89.98
XC7K325T-DIE4058	**$1,843.78**	**$854.00**	**46%**	**$211.20**		
XC7K70T-DIE4058	$225.00	$113.00	50%		$31.64	$49.50
XC7V585T-DIE4058	6,038.60	4,830.41	80%		$1,352.51	$1,328.49
XC7VX690T-DIE4058	$11,151.00	$7,757.00	70%		$2,171.96	$2,453.22
XC7Z010-DIE0628	$72.00	$53.00	74%		$14.84	$15.84
XC7Z020-DIE0628	$154.00	$98.00	64%		$27.44	$33.88
XC7Z030-DIE4058	$456.00	$219.00	48%		$61.32	$100.32
XC7Z030-DIE4378	$456.00	$219.00	48%		$61.32	$100.32
XC7Z045-DIE4058	**$2,512.00**	**$1,060.00**	**42%**		**$296.80**	**$552.64**
XC7Z100-DIE4058	$4,727.00	$3,635.00	77%	$326.00	$1,017.80	$1,039.94

DEVICES RESOURCES

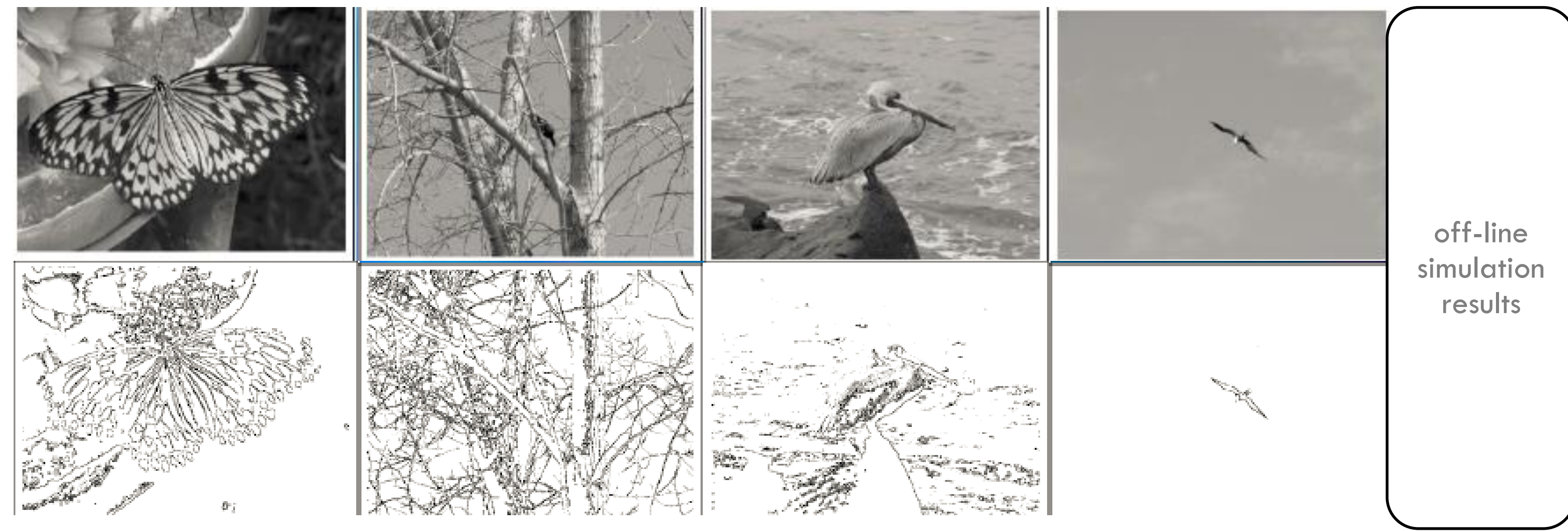
	XC7K70T	XC7K160T	XC7K325T	Z-7010	Z-7020	Z-7030	Z-7045	Z-7100
Logic Cells	65,600	126,240	326,080	28K	85k	125k	350k	444k
BlockRAM (Kb)	4,860	11,700	16,020	240	560	1060	2180	3020
DSP Slices	240	600	840	80	220	400	900	2020
PCIe® Gen2 Blocks	1	1	1					
GTX Transceivers	8	8	16	0	0	4	16	16
I/O Pins	300	400	500					
Max Power Consumption			12 W	1.5 W		3 W		

COMPUTER VISION FOR SMART CAMERAS AND MEDICAL IMAGING APPLICATIONS

Smart cameras capture high-level description of a scene and perform **real-time extraction of meaningful information**

- Current compression algorithms: **few seconds** are required
- **For safety-critical applications (e.g., transports, or personnel tracking in a dangerous environment), latency could lead to serious problems.**

Del Viva et al algorithm[1] studied how to reproduce initial stage of the brain visual processing: find contours



off-line simulation results

[1] *M. Del Viva, G. Punzi, and D. Benedetti. Information and Perception of Meaningful Patterns. PloS one 8.7 (2013): e69154.*

COMPUTER VISION FOR SMART CAMERAS AND MEDICAL IMAGING APPLICATIONS

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- Current compres[...]**nds** are required
- **For safety-cri[...] or personnel tracking in a dangerous e[...] problems.**

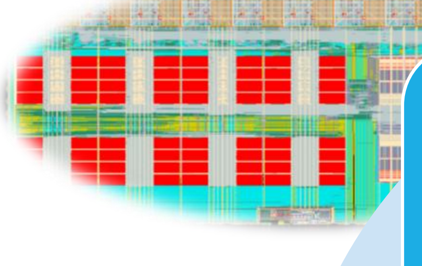
Del Viva et al algori[...]d contourns

Strong improvement by INFN of Pisa. Many presentation at hiPEAC conference

off-line simulation results

[1]M. Del Viva, G. Punzi, and D. Benedetti. Information and Perception of Meaningful Patterns. PloS one 8.7 (2013): e69154.

RESEARCH UNITS DESCRIPTION AND DUTIES



INFN (Sezione di Milano)

Principal Investigator:
Alberto Stabile (100%)
Age 31

- WP1: AM chip design and simulation

External collaborations

- IAPP EU project
- LPNHE (Paris)
- EMC S.r.l.

The 3 laboratories are funded by the FTK project and will provide their facilities for these new developments. The costs for the IMPART project will be used to fabricate the new IMPART system.

INFN (LNF)

Group team leader:
Matteo Beretta (30%)
Age 45

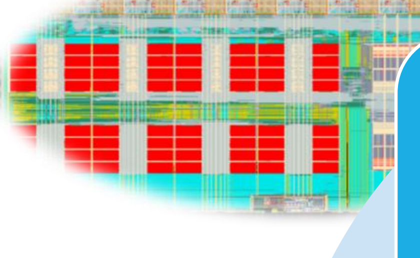
- WP2: System in Package (SiP) design, simulation, and tests

INFN (Sezione di Pisa)

Group team leader:
Calliope L. Sotiropoulou (50%)
Age 33

- WP3: Smart Cameras and DNA sequencing

RESEARCH UNITS DESCRIPTION AND DUTIES



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~~**Age 45**~~

- ~~WP2: System in Package (SiP) design, simulation, and tests~~

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Group team leader:
P. Luciano (80%) **Age 27**

- WP3: Smart Cameras and DNA sequencing

RESEARCH UNITS DESCRIPTION AND DUTIES

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Principal Investigator:

Alberto Stabile (100%)

Age 31

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- WP2: System in Package (SiP) design,

- IAPP EU project
- LPNHE (Paris)
- EMC S.r.l.
- **Bicocca**

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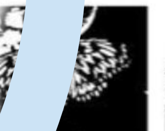

WP1. AM CHIP DESIGN AND SIMULATION

Alberto Stabile (INFN – Milano)

This work package consists in the **design of the Associative Memory ASIC** in a standard **28 nm CMOS** process.

Starting time: Jan. 2015

	Work package	deadline
Deliverable	**WP1.1:** AM cell design (M. Beretta) • Minimize the silicon area and the power consumption	May 2015
Deliverable	**WP1.2:** Front-end design (A. Stabile) • Writing a behavioral netlist	May 2015
Deliverable	**WP1.3:** Floorplan and back-end design (A. Stabile) • Automatic place & route	Sept. 2015
Deliverable	**WP1.4:** Functional simulation (N. Biesuz) • Validate through digital simulations to confirm the functionality of the layout	Nov. 2015
Milestone	**WP1.5:** Chip integration and submission (A. Stabile) • Final checks: Design Rule Check (DRC) and Layout Versus Schematic (LVS)	Dec. 2015
Fabrication	**WP1.Fab:** AM chip will be fabricated by TSMC	Feb. 2016
Milestone	**WP1.6:** Characterization of the AM chip (M. Beretta) • AM chip will be characterized in a single-chip package.	Apr. 2016

WP1A. AM CHIP DESIGN AND SIMULATION

Alberto Stabile (INFN – Milano)

This work package consists in the **design of the Associative Memory 07a** in a standard **28 nm CMOS** process.

Starting time: Mar. 2015

deadline

Deliverable — **WP1a.1:** AM cell design (Bicocca) — DONE — May 2015
- Minimize the silicon area and the power consumption

Deliverable — **WP1a.2:** Front-end design (A. Stabile) — DONE — May 2015
- Writing a behavioral netlist

Deliverable — **WP1a.3:** Floorplan and back-end design (A. S... — DONE — Jun. 2015
- Automatic place & route

Deliverable — **WP1a.4:** Functional simulation (Bicocca) — DONE — Jun. 2015
- Validate through digital simulations to confirm the functionality of the la...

Milestone — **WP1.5:** Chip integration and submission (A. St... — DONE — Jun. 2015
- Final checks: Design Rule Check (DRC) and Layout Versus Schem...

Fabrication — **WP1.Fab:** AM chip will be fabricated by TSM... — In work — Feb. 2016

Milestone — **WP1.6:** Characterization of the AM chip (A. Stabile) — Nov. 2015
- AM chip will be characterized in a single-chip package.

WP1B. AM CHIP DESIGN AND SIMULATION

Alberto Stabile (INFN – Milano)

This work package consists in the **design of the Associative Memory 07b** in a standard **28 nm CMOS** process.

Starting time: Jun. 2015

	Work package	deadline
Deliverable	**WP1.1:** AM cell design (Bicocca) • Minimize the silicon area and the power consumption	Nov. 2015
Deliverable	**WP1.2:** Front-end design (A. Stabile) • Writing a behavioral netlist	Dec. 2015
Deliverable	**WP1.3:** Floorplan and back-end design (A. Stabile) • Automatic place & route	Feb. 2016
Deliverable	**WP1.4:** Functional simulation (N. Biesuz) • Validate through digital simulations to confirm the functionality of the layout	Feb. 2016
Milestone	**WP1.5:** Chip integration and submission (A. Stabile) • Final checks: Design Rule Check (DRC) and Layout Versus Schematic (LVS)	Feb. 2015
Fabrication	**WP1.Fab:** AM chip will be fabricated by TSMC	Apr. 2016
Milestone	**WP1.6:** Characterization of the AM chip (M. Beretta) • AM chip will be characterized in a single-chip package.	Sept. 2016

OLD TIMETABLE OVERVIEW

2015	Jan	Mar	May	Jul	Sep	Nov	Jan 2016	Mar	May	Jul	Sep	Nov	2016

- **WP1.1: AM cell design**
- **WP1.2: Front-end design**
- **WP1.3: Floorplan and back-end design**
- **WP1.4: Functional simulation**
- **WP1.5: Chip integration and submission**
- **FAB: AM chip fabrication**
- **WP1.6: Characterization of the AM chip**
- **WP2.1: Studies on 3D technologies**
- **WP2.1: Design and simulation of multi-chip package**
- **FAB: Package fabrication and chip assembly**
- **WP2.2: Characterization of the System in Package**
- **WP3.1: Study of the processing techniques**
- **WP3.2: Firmware and software implementation**
- **WP3.3: Characterization of the IMPART device**
- **WP3.4: Field tests (smart cameras)**

OLD TIMETABLE OVERVIEW

2015 | Jan | Mar | May | Jul | Sep | Nov | Jan 2016 | Mar | May | Jul | Sep | Nov | 2016

WP1a.1: AM cell design

WP1b.1: AM cell design

WP1a.2: Front-end design

WP1b.2: Front-end design

WP1a.3: Floorplan and back-end design

WP1b.3: Floorplan and back-end design

WP1a.4: Functional simulation

WP1b.4: Functional simulation

WP1a.5: Chip integration and submission

WP1b.5: Chip integration and submission

FABa: AM chip fabrication

FABb: AM chip fabrication

WP1a.6: Characterization of the AM chip

WP1b.6: Characterization c

WP2.1: Studies on 3D technologies

WP2.1: Design and simulation of multi-chip package

FAB: Package fabrication ar

WP2.2: Characte

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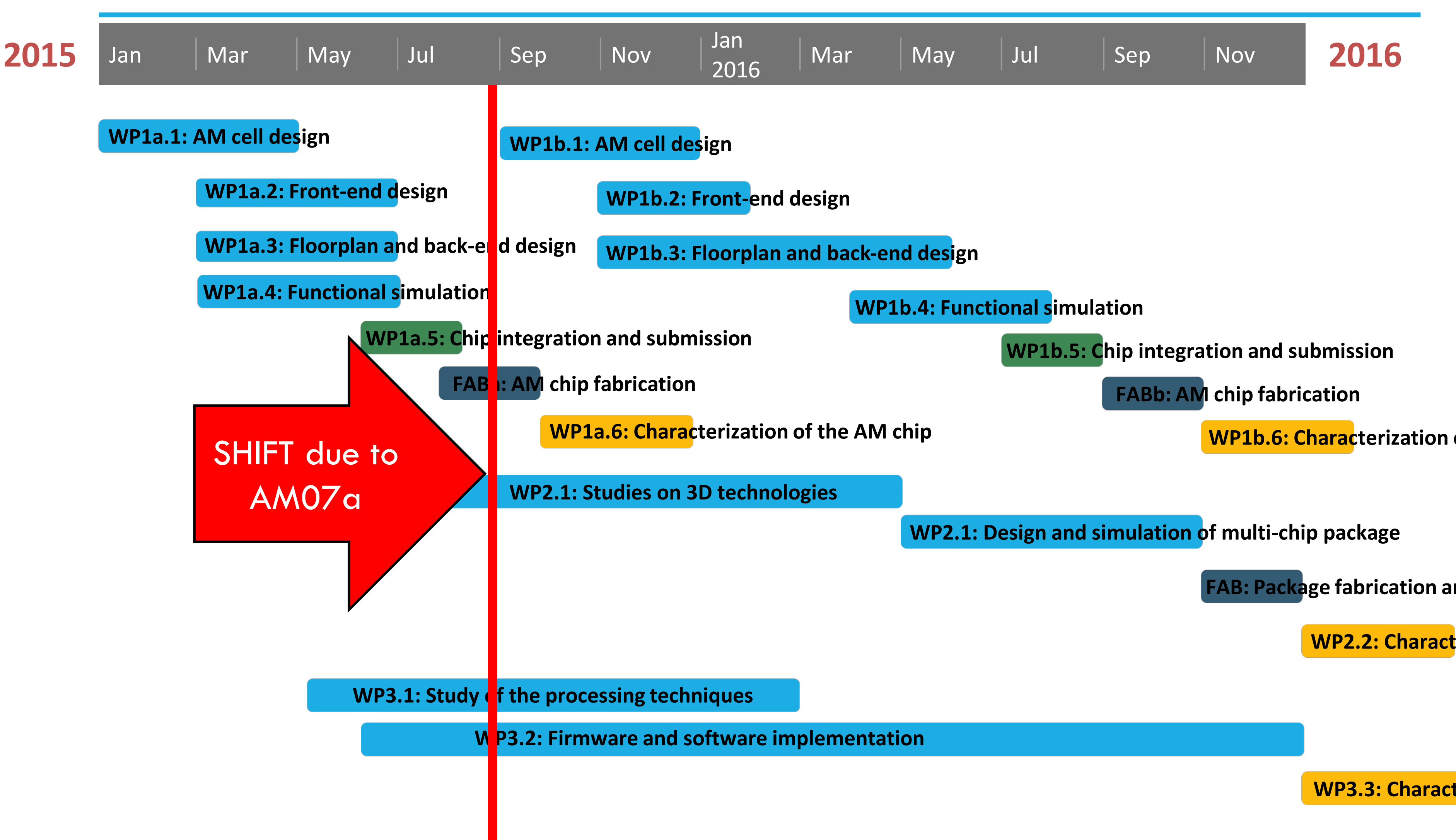
WP3.3: Charact

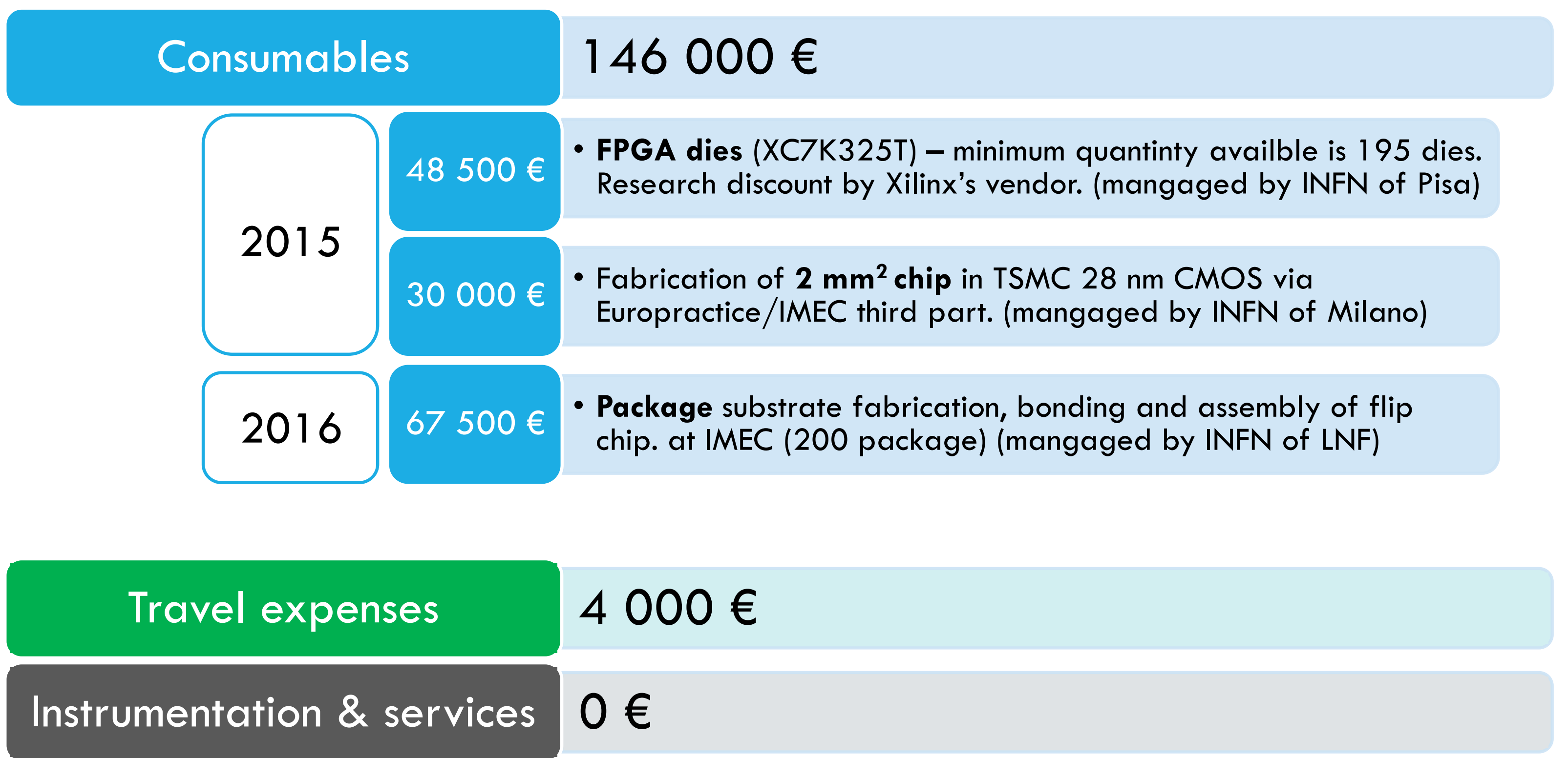
OLD TIMETABLE OVERVIEW



COSTS

Project budget

- **150 000 € in 2 years (75 000 € per year)**



The 3 laboratories provide their facilities for these new developments.

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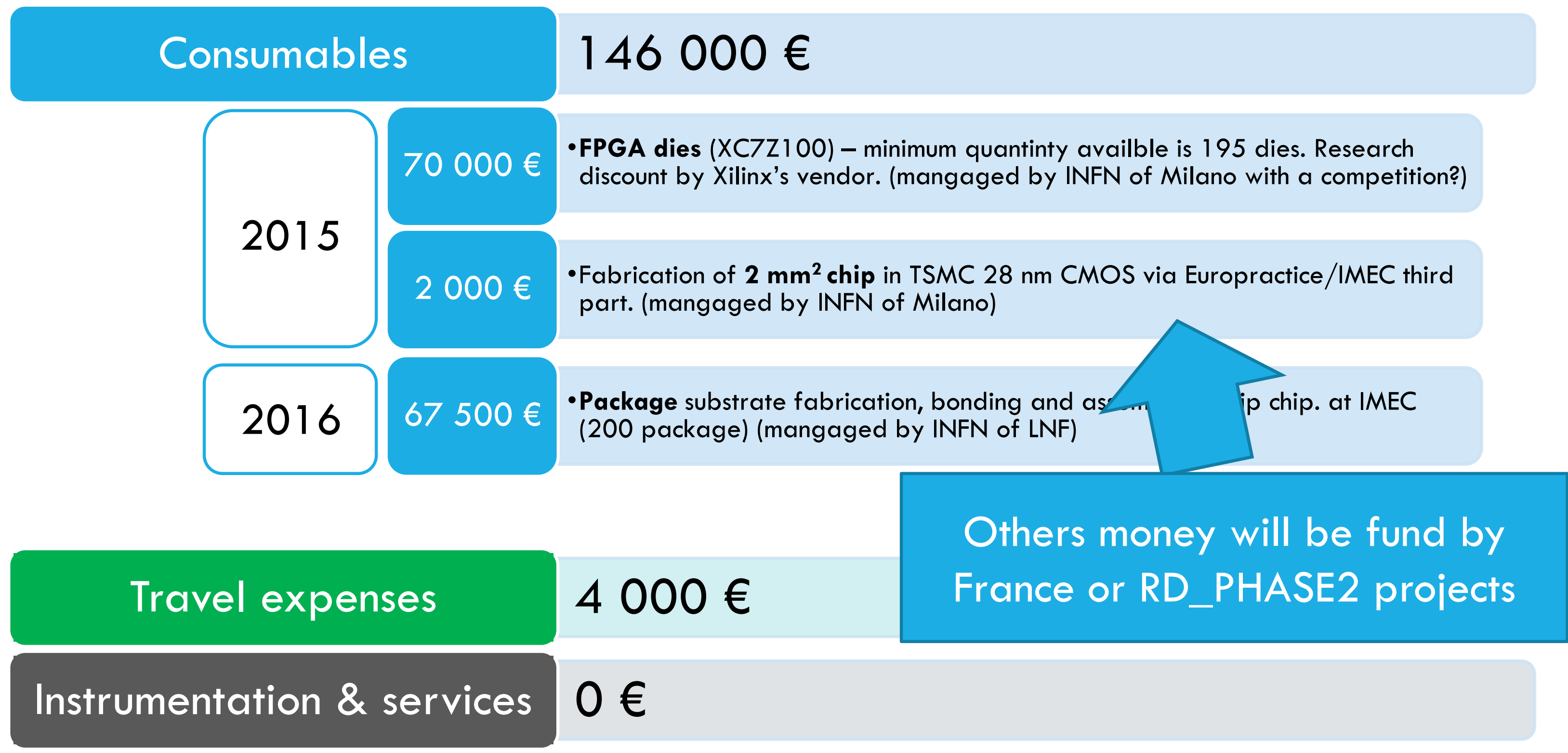

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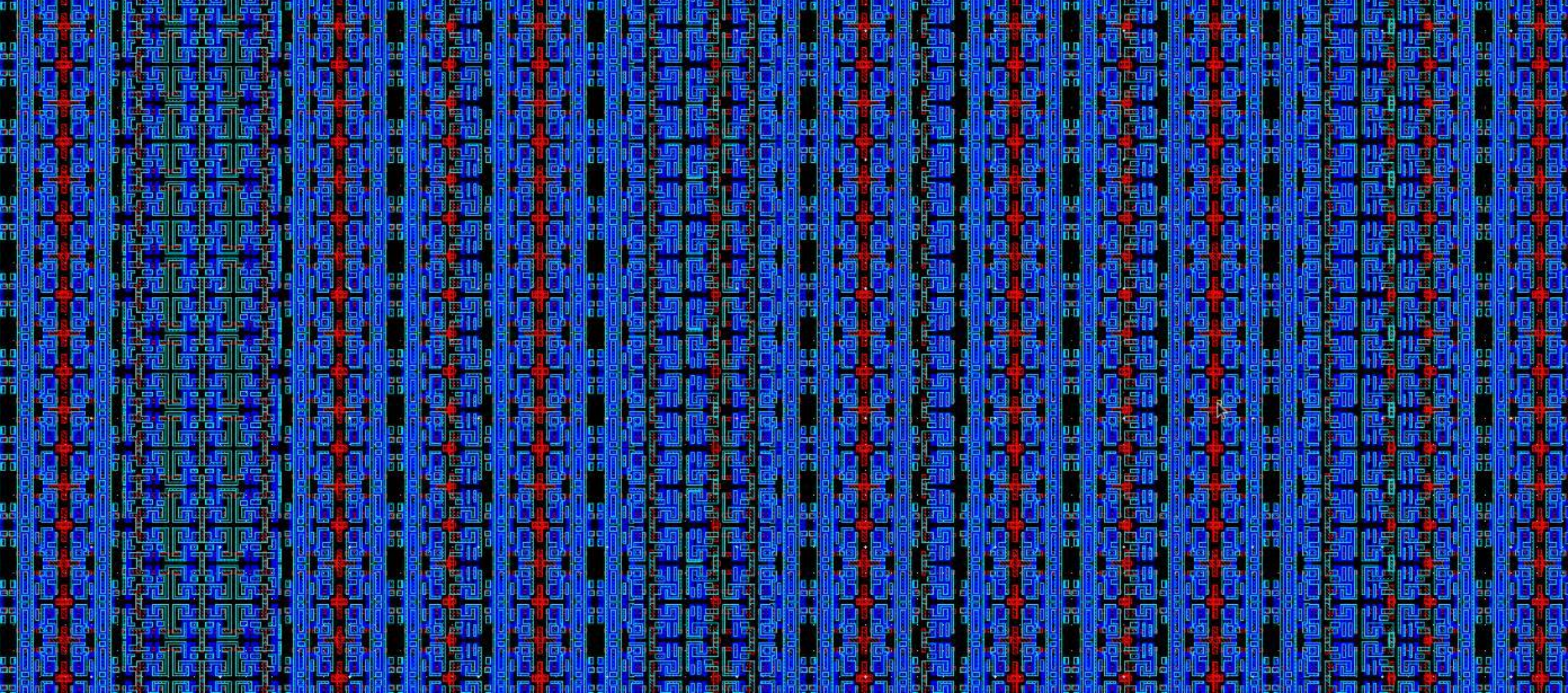

BACKUP SLIDES

Alberto Stabile