



ID contributo: 47

Tipo: poster

IDSAC - IUCAA Digital Sampler Array Controller

IUCAA Digital Sampling Array Controller (IDSAC) is a generic CCD Controller which is flexible and powerful enough to control a wide variety of CCDs and CMOS detectors used for ground based astronomy. It has a fully scalable architecture, which can control multiple CCDs and can be easily expanded. The controller has a modular backplane architecture consists of Single Board Controller Cards (SBCs) and can control a mosaic or independent of 5 CCDs. Each Single Board Controller (SBC) has all the resources to run Single large format CCD having up to four outputs. All SBCs are identical and are easily interchangeable without any reconfiguration. A four channel video processor can process up to four output CCDs with or without dummy output at 1Mpixels/Sec/Channel with 16 bit resolution. Each SBC will have USB 2.0 interface which will be connected to a separate computer via USB to Fiber converters. The SBC uses a reconfigurable hardware (FPGA) as a Master Controller. The best feature of IDSAC is it uses the technique of Digital Correlated Double Sampling(DCDS). It is known that CCD video output is dominated by thermal KTC noise contributed from the summing well capacitor of the CCD output circuitry. To eliminate thermal KTC noise Correlated Double Sampling (CDS) is a very standard technique. CDS performed in Digital domain (DCDS) has several advantages over its analog counterpart, such as - less electronics, faster readout and easier post processing. It is also flexible with sampling rate and pixel throughput while maintaining the core circuit topology intact. The noise characterization of the IDSAC CDS signal chain has been performed by analytical modelling, software simulation and practical measurements. Various types of noise such as white, pink, power supply, bias etc. has been considered while creating a analytical noise model tool to predict noise of a controller system like IDSAC. Standard test bench softwares like Pspice and Multisim are used to simulate the noise performance while several tests are performed to measure the actual noise of IDSAC. The theoretical calculation matches very well with component level simulation as well as practical measurements within 10% accuracy.

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