8th International Workshop on Semiconductor Pixel Detectors for Particles and Imaging.

PIXEL 2016

Contribution ID: **79** Type: **contributed paper**

Thin hybrid pixel assembly with backside compensation layer on ROIC

ATLAS will replace the entire tracking system for operation at the HL-LHC. This will include a significantly larger pixel detector of approximately 10 m2. It is critical to reduce the mass of the pixel modules and this requires thinning both the sensor and readout to about 150 micrometers each. The bump yield in thin module assembly using solder based bump bonding can be problematic due to wafer bowing during processing at high temperatures. A new bump-bonding process using backside compensation on the readout chip to address the issue of low yield will be presented. Results from characterization of assemblies produced from readout wafers thinned to 100 micrometers and the effect of applying backside compensation will be presented. Hybrid modules with bond yields close to 100% have been measured using 100 um thick FEI4 readout chip.

Summary

The ATLAS FE-I4 readout IC, ROIC, is almost 20 mm x 20 mm in size with order 10 micrometers of metal and dielectrics above the CMOS implants. When the die is thinned to a few hundred micrometers it bows due to the stress in the dielectric/metal layers no longer being resisted by a thick silicon substrate. This bowing is increased further at elevated temperatures due to the different coefficient of thermal expansions of the dielectric/metal layers and silicon substrate. Solder based bump-bonding typically takes place at 260C and will increase the bow of the die significantly to several hundred micrometers. The size of the solder bumps are only 25 micrometers in diameter. Therefore, bowing of the ROIC will cause issues with the yield of the solder connections as they will not make electrical connection with the sensor and ROIC. The work will show that the bow of the die can be affected with the use of a post-processed dielectric layer and metal layer deposited on the backside of the wafer. The bow of the FE-I4 dies as a function of die temperature for different backside dielectric deposition is shown. The details of the fabrication process and the characterization techniques are described, as well as the final result. The processing technologies have been chosen to be compatible with both the existing CMOS ROIC but also with the through-silicon-via, TSV, technology of the foundry. The near 100% bond yield of assemblies made from 100 micrometer thick ROICs and 150 micrometers sensors are shown. The assemblies have been shown to be robust to thermally cycling from 60C to -40C 100 times and to thermal shock (defined as a sudden change from room temperature to -40C).

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