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Pixel hybridization technologies for the HL-LHC

During the 2024-2025 shutdown, the Large Hadron Collider (LHC) will be upgraded to reach an instantaneous luminosity up to 7×10 cm^{-2} s^{-1}. This upgrade of the accelerator is called High-Luminosity LHC (HL-LHC). The ATLAS and CMS detectors will be upgraded to meet the new challenges of HL-LHC: an average of 200 pile-up events in every bunch crossing and an integrated luminosity of 3000 fb^{-1} over ten years. In particular, the current trackers will be completely replaced to meet the requirements coming with the high instantaneous and integrated luminosities.

The pixel detectors, the innermost part of the trackers, need significantly rethinking in all their basic elements to the performance and/or to reduce the overall cost of the trackers. A new 65 nm front-end electronics is being developed by the RD53 collaboration. The new front-end chip will be compatible with 50 × 50 μm^2 or 25 × 100 μm^2 pixel size sensors. An intensive program of R&D has been promoted to study new sensor technologies. The smaller pixel sizes imply up to five times the number of bumps used in the current ATLAS Insertable B-Layer modules and consequently an order of 120 thousands pixels per chip.

In this talk, a review of the hybridization technologies will be presented. In particular, the on-going qualification program at Selex will be discussed. Selex has been one of the two vendors for the current ATLAS pixel detector and as required by the HL-LHC projects, it is now upgrading its capability to meet larger wafer size at higher bump density. The qualification of some flip-chip sites will be also presented as a possible help in the organization and production workflow. Finally, alternative hybridization techniques, as the capacitive coupling for HVCMOS detectors, will also be discussed.

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