INFN
Istituto Nazionale
di Fisica Nucleare

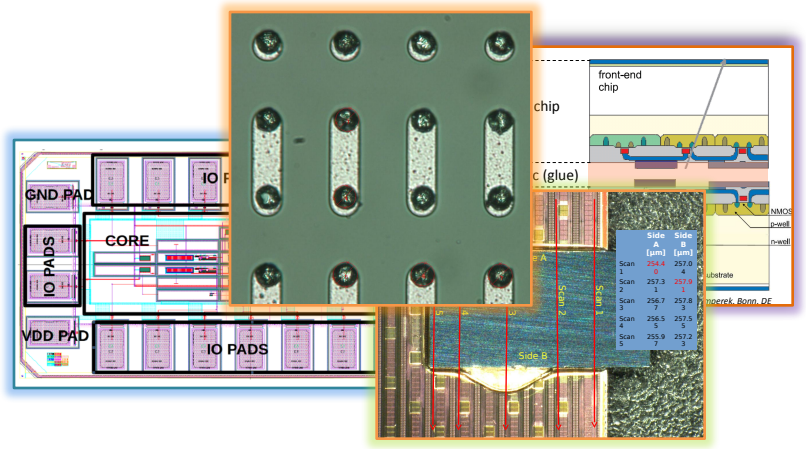
PIXEL
2016

International Workshop on Semiconductor Pixel Detectors for Particles and Imaging
Sestri Levante, 5-9 September

Pixel Hybridization Technologies for HL-LHC

M. Biasotti[1], V. Ceriale[1], G.Darbo[1], G.Gariano[1], **A.Gaudiello[1]**, C. Gemme[1], L. Rossi[1], A. Rovani[1], E. Ruscino[1], G. Alimonti[2]

ATLAS
EXPERIMENT



[1]Istituto Nazionale di Fisica Nucleare Sez. Genova
[2]Istituto Nazionale di Fisica Nucleare Sez. Milano

Introduction

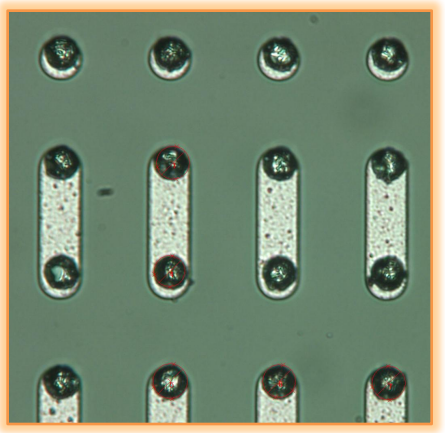
The new 65 nm front-end chip, being developed by RD53 Collaboration, will be compatible with **50 × 50 µm² or 25 × 100 µm² pixel size sensors.**

➘ The smaller pixel sizes imply up to five times the bump density used in the current ATLAS Insertable B-Layer modules and consequently an order of **120 k pixels per FE-I4 size chip.**

Necessary to improve or develop new hybridizations forms, in next slides:

- High-Density Bump Bonding
- Capacitive couplings

Indium BB Studies at High Density



Indium BB Studies at High Density

Old and consolidated technology
Bump-Bonding at high density is a real productive effort:

- It is very competitive for innermost layers as **indium bumps** have an easier process even for thin wafers
  - **It does not need any type of temporary support**
    - e.g. as for SnAg process used for the Insertable B-layer: here a glass substrate was connected to the wafer with a polymeric glue, removed via laser exposure at the end of the process
- At the moment we are optimizing the process using dummies produced by **FBK** (Trento) with bump deposition and the flip-chip of some tiles done at **Selex** (Rome):
  - This R&D allows studies on bump height, size and the process parameters as pressure and temperature.
  - Visual, mechanical and electrical test are also performed, before and after the assemblies.

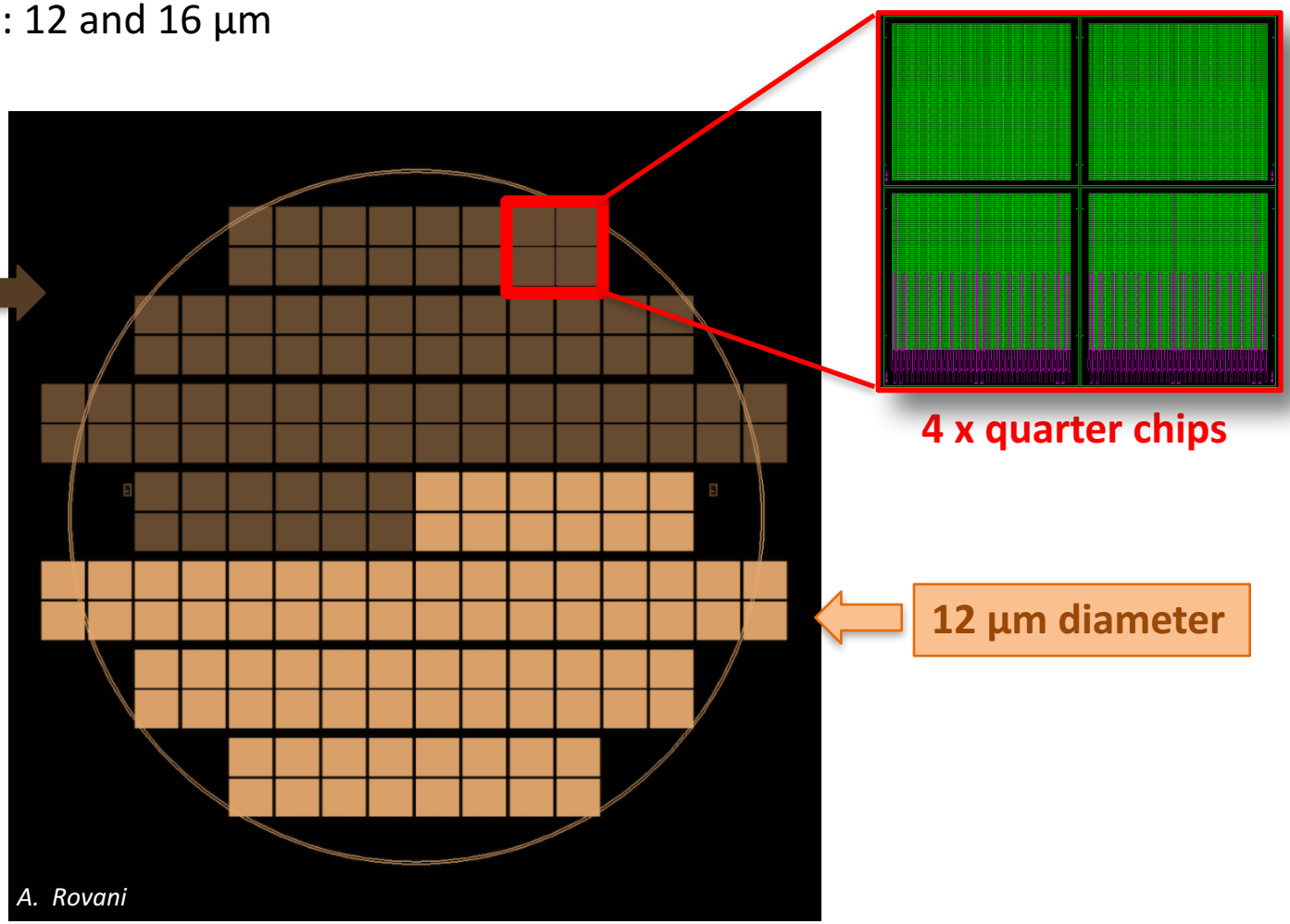
In last months we performed a bump deposition on 6-inch and 12-inch wafers, in the following slides an overview of the activity is reported.

High-density Large-surface bump bonding

Dummy wafers produced by FBK with resistive chains:

- 6-inches, 640 µm thick wafers with 30 FE-I4 size dummy chips (**or 4 x quarter chips**)
- Metal pad: 18 and 20 µm
- Passivation open: 10 and 12 µm
- Indium bump size: 12 and 16 µm

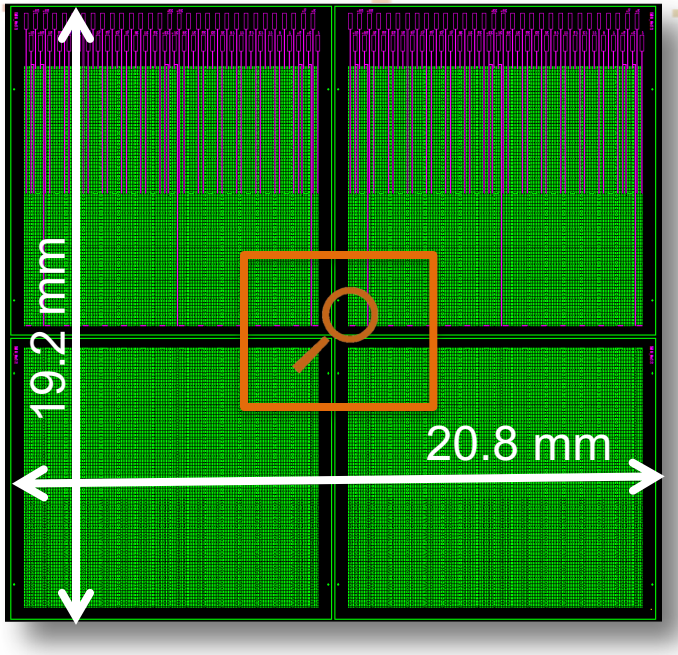
FE-I4 chip

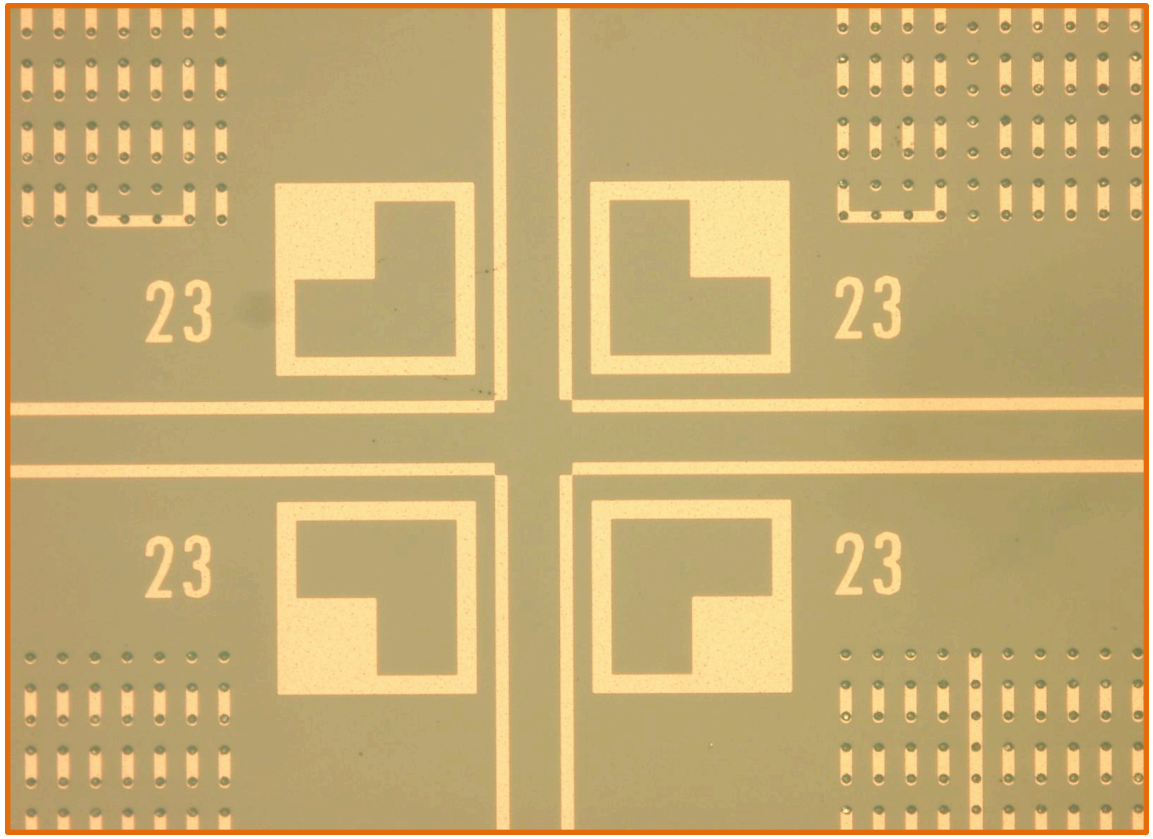


High-density Large-surface bump bonding

Dummy chip with resistive chains

- FE-I4 size
  - With flip-chip possibility for the tiles
- 120k-bumps: **but only 21.3 k-bumps tested (124 chains of 172 bumps per chip, uniformly distributed over the chip)**



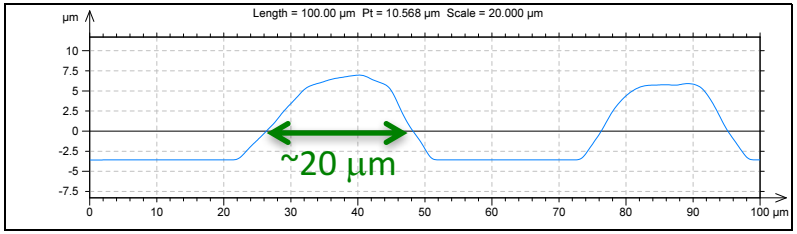


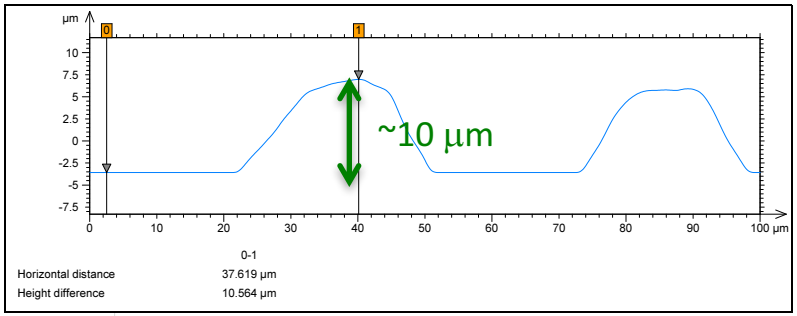
Here a picture of the bump deposition before flip-chip

High-density Large-surface bump bonding

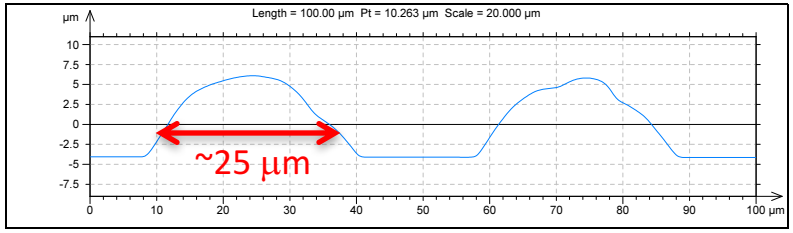
Preliminary measurements of bumps dimension before the flip-chip, done in Genova using a profilometer

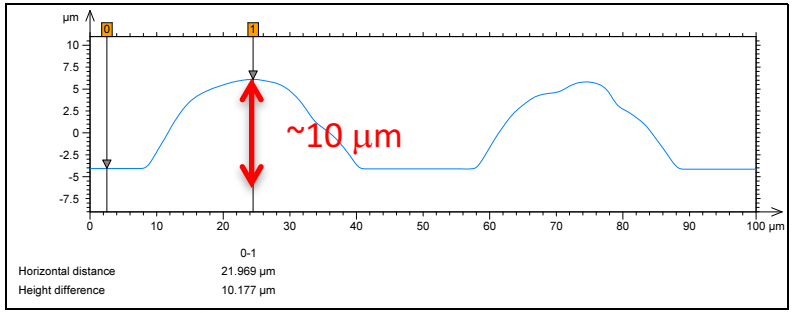
12 µm ⌀ bump

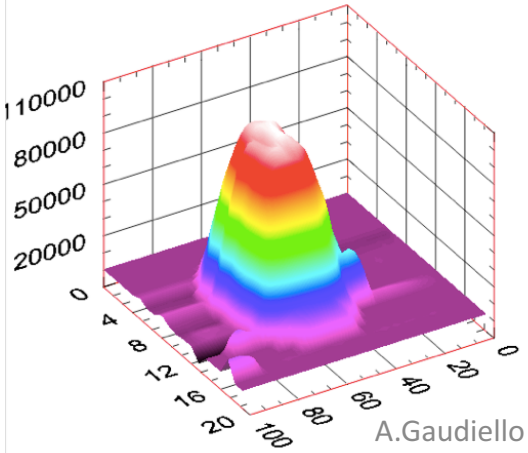




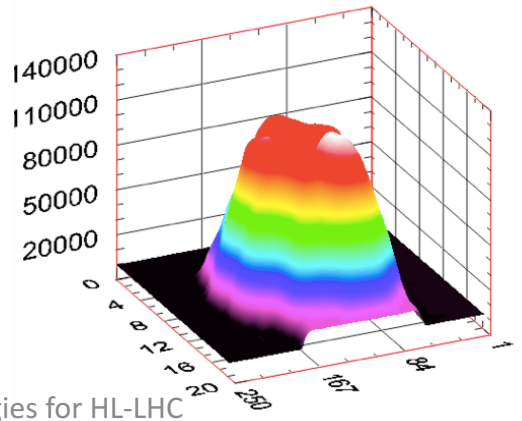
16 µm ⌀ bump





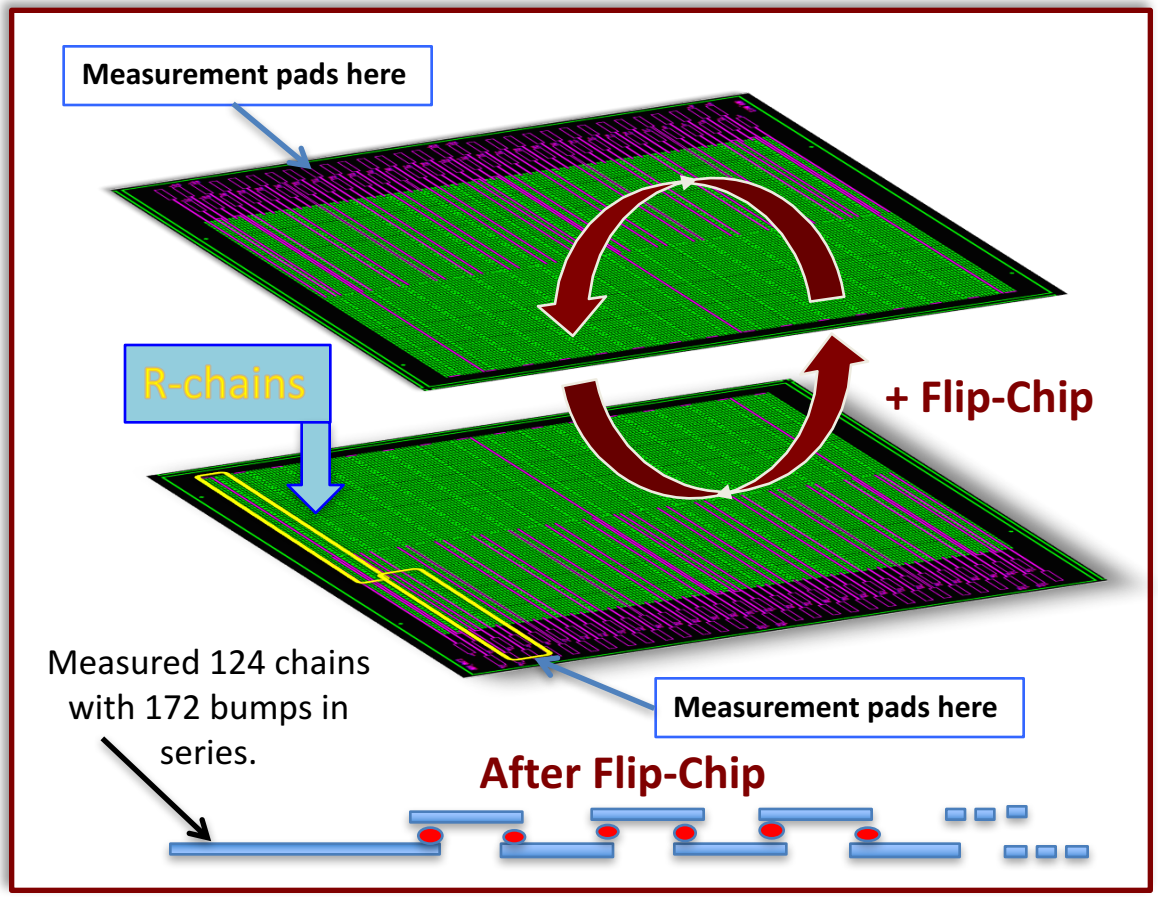


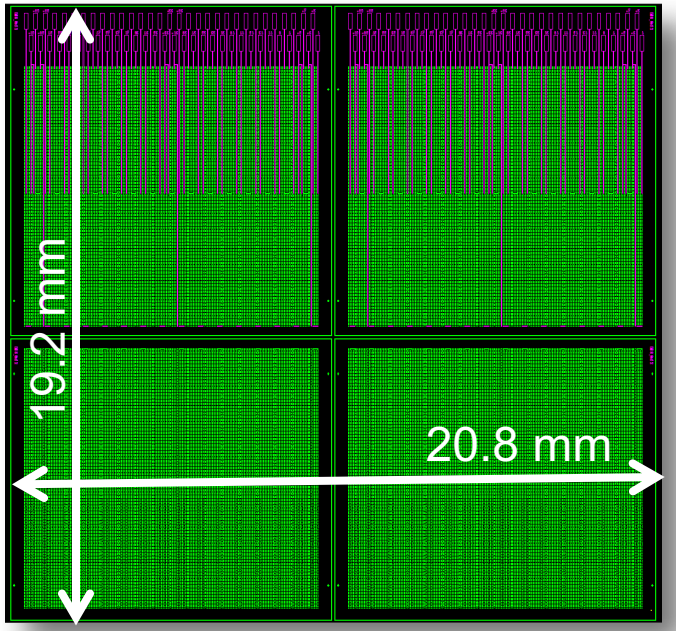
3D bump profile



High-density Large-surface bump bonding

Should flip one quad-chip on top of the other leaving the measuring pads free for measurement under needles (i.e. flip one chip over the other rotated by 180^{o} and superimpose the bump pattern).



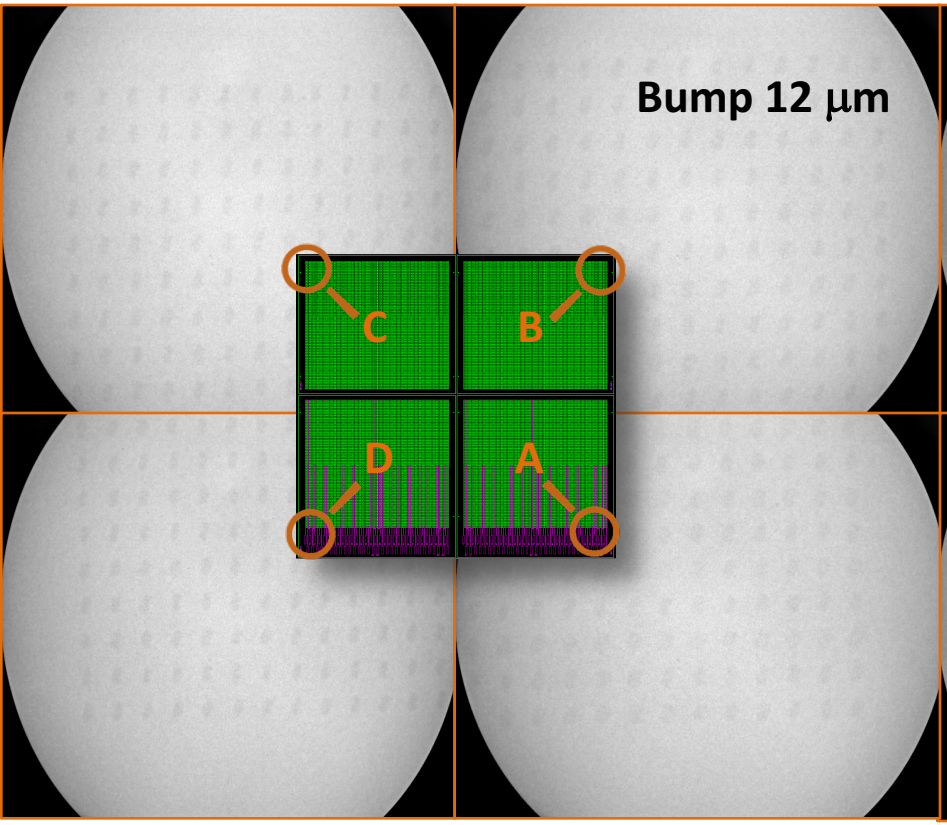


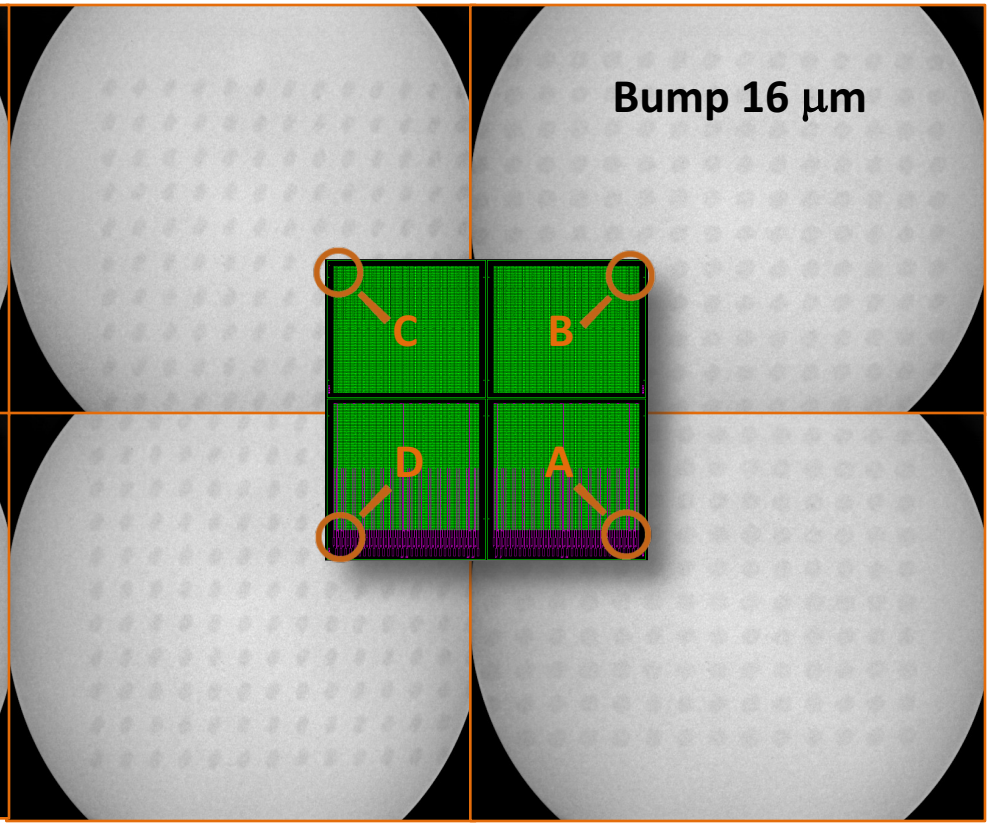
No "open" amongst ~64 k bumps (3 devices tested)

No indications of shorts bumps

High-density Large-surface bump bonding

The flipped chips have been also tested with X-ray to @ 120 keV to check the entire surface and both bumps type at 12 and 16 µm look ok!



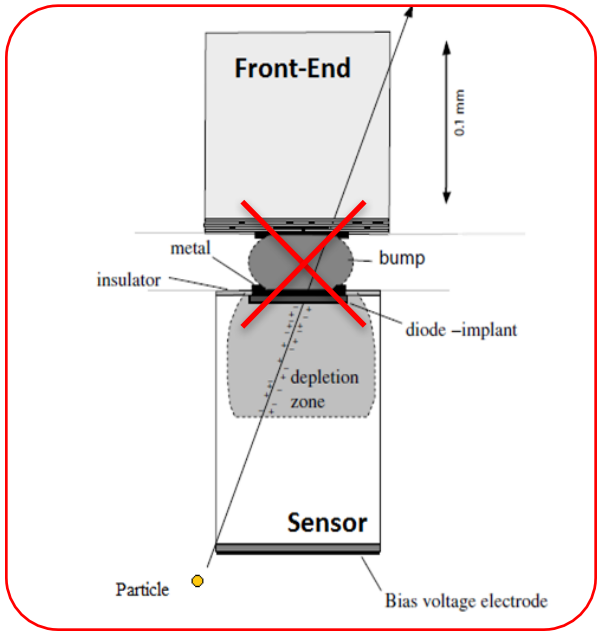


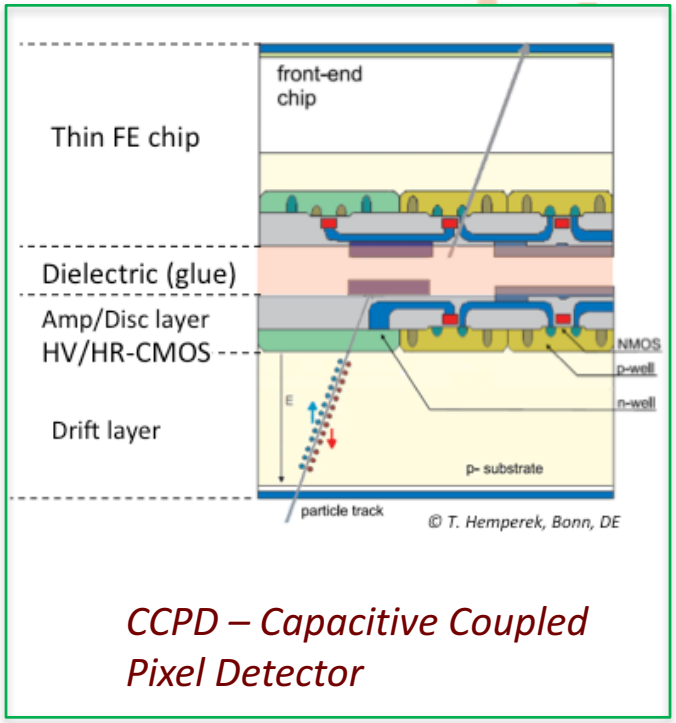
High-density bump deposition on 12” wafers

On 12” wafer deposition of bumps only (without resistive chains)

- Wafer has been visually analyzed and bumps height measured with a profilometer
  - Preliminary results on bump height (~10 µm), uniformity good (~1 µm)
- Next step is to repeat the same deposition and tests done for 6” wafers on 12" wafers with resistive chains
  - Repeat tests also on thin wafers

Studies on Capacitive Couplings





CCPD – Capacitive Coupled Pixel Detector

Studies on Capacitive Couplings

Capacitive couplings could be a real good option to reduce cost and simplify the hybridization process

At the moment R&D is ongoing with the following requirements:

- Uniformity and repeatability of the process
- Evaluation of radiation tolerance of the coupling medium (typically glues)
- **Evaluation of cost effectiveness**
  - ↘ Time per chip assembly
    - ↘ Wafer to wafer processes are excluded: R/O chip are typically 12” wafers, HV-CMOS are 8”-wafers
- Control of thickness the coupling medium and making of the spacers between the sensor and the FE

First hybridization Studies

Basic process

Spin SU-8 photoresist
Pattern pillars by mask

Glue deposition

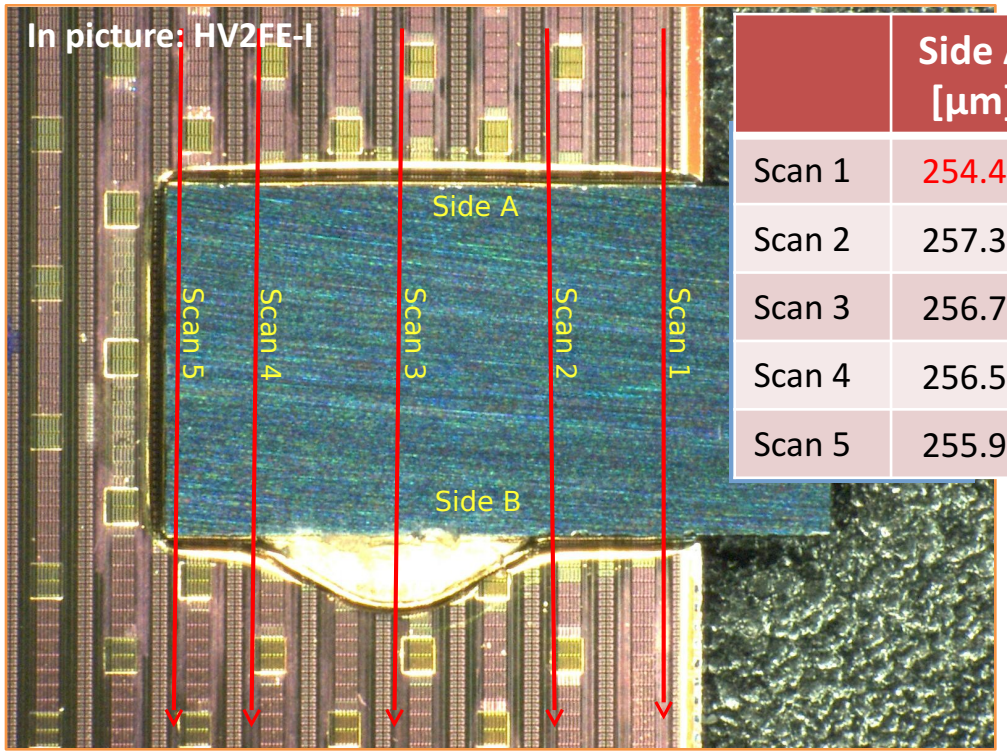
Align & pressure

Deposition of SU8 photoresist by spinning

Credits: Giovanni Darbo

In 2014 and mid 2015 test on "in-house" hybridization

➘ Successful single chip assemblies and learnt on glue and SU8 deposition (spacers)



	Side A [µm]	Side B [µm]
Scan 1	254.40	257.04
Scan 2	257.31	257.91
Scan 3	256.77	257.83
Scan 4	256.55	257.55
Scan 5	255.97	257.23

Now systematic test on large chips (FE-I4 size) and wafer process for pillars

Pillars and Procedure for Controlled Glue Thickness

Basic process

Spin SU-8 photoresist
Pattern pillars by mask

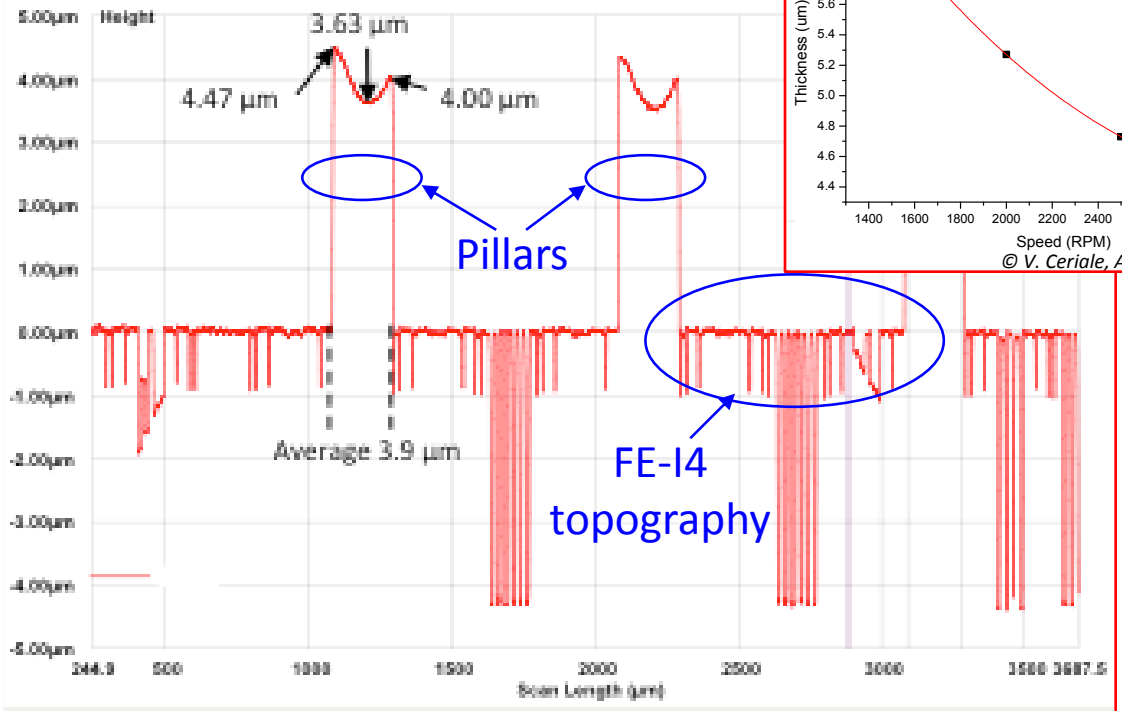
Glue deposition

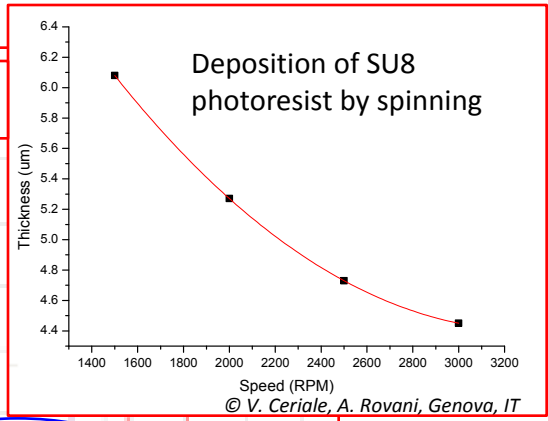
Align & pressure

Deposition of SU8 photoresist by spinning

- Deposit uniform layer of SU8 photoresist on R/O chip wafer (or single chip) by spinning – tune for 5 µm layer by controlling RPM speed
- Pattern pillars using lithographic process

Profile of pillars on top of a FE-I4 chip





Credits: Giovanni Darbo

Studies on Capacitive Couplings

Basic process

Spin SU-8 photoresist
Pattern pillars by mask

Glue deposition

Align & pressure

Deposition of SU8 photoresist by spinning

Credits: Giovanni Darbo

In 2014 and mid 2015 test on "in-house" hybridization

↘ Successful single chip assemblies and learnt on glue and SU8 deposition (spacers)

Now systematic test on large chips (FE-I4 size) and wafer process for pillars

A batch of dummy wafer produced at FBK (Trento) with capacitive structures to test uniformity of glue thickness layer 6-inch wafers, 24-32 capacitors (3-7 pF) per chip

Studies on Capacitive Couplings

Basic process

Spin SU-8 photoresist
Pattern pillars by mask

Glue deposition

Align & pressure

Deposition of SU8 photoresist by spinning

Credits: Giovanni Darbo

In 2014 and mid 2015 test on "in-house" hybridization

↘ Successful single chip assemblies and learnt on glue and SU8 deposition (spacers)

Now systematic test on large chips (FE-I4 size) and wafer process for pillars

A batch of dummy wafer produced at FBK (Trento) with capacitive structures to test uniformity of glue thickness layer 6-inch wafers, 24-32 capacitors (3-7 pF) per chip

- **The 6 wafers are at Selex together with pillar deposition mask**
- **Also blank wafers provided to Selex to test SU8 spinning and photolithography**

↘ **measurements of pillar uniformity has been performed in July**

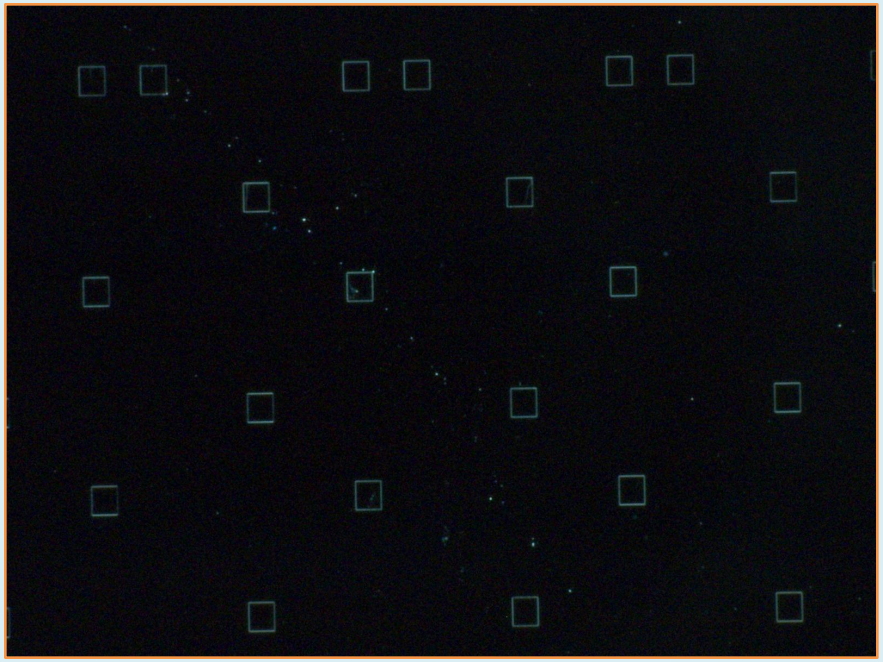
Studies on Capacitive Couplings

Basic process

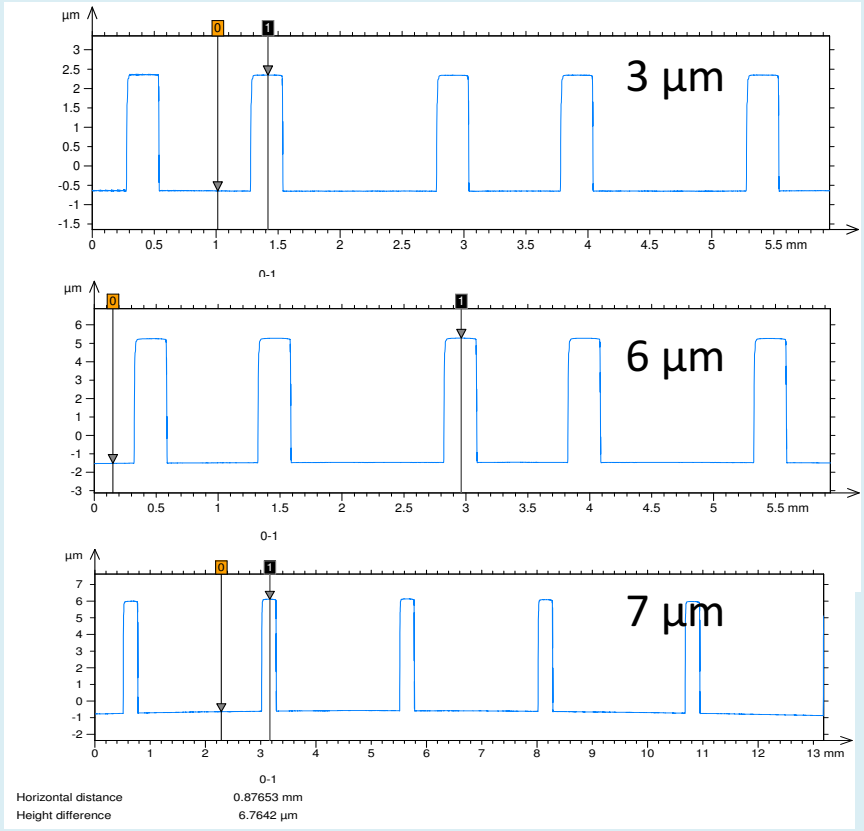
In 2014 and mid 2015 test on “in-house” hybridization

Pillars deposition only @ Selex: Very promising results!

- 3 wafers with pillars at 3,6 and 7 µm
- Good planarity



Credits: Giovanni Darbo



Studies on Capacitive Couplings

Basic process

Spin SU-8 photoresist
Pattern pillars by mask

Glue deposition

Align & pressure

Deposition of SU8 photoresist by spinning

Credits: Giovanni Darbo

In 2014 and mid 2015 test on "in-house" hybridization

↘ Successful single chip assemblies and learnt on glue and SU8 deposition (spacers)

Now systematic test on large chips (FE-I4 size) and wafer process for pillars

A batch of dummy wafer produced at FBK (Trento) with capacitive structures to test uniformity of glue thickness layer 6-inch wafers, 24-32 capacitors (3-7 pF) per chip

- **The 6 wafers are at Selex together with pillar deposition mask**
- **Also blank wafer provided to Selex to test SU8 spinning and photolithography**

↘ **measurements of pillar uniformity has been performed in July**

Flip-chip at Genova and other labs – thermal/UV glue curing (preliminary studies done)

Glues in Evaluation

	Araldite 2011	Araldite 2020	Epotek 301-2	EPOLITE FH-5313	Master Bond UV15DC80LV
Viscosity [Pas]	30 ÷ 45	**0.15**	**0.22 ÷ 0.45**	1.97	**0.15 ÷ 0.50**
Relative dielectric constant	3.4/3.2/3.2 50Hz/1kHz/10kHz	?	3.8 1kHz	4.06 100Hz	3.49 60 Hz
Loss tangent [%]	1.7/1.8/2.6 50Hz/1kHz/10kHz	?	1.2 1kHz	100Hz	
Pot life [min]	100	40÷50	480	30	
Curing time [min]	30 @ 60º	90 @ 60º	180 @ 80º	60 @ 65º	UV Curing + 40 ÷ 60 @ 80º
Air bubbles	Many	Some	None	Many	To test
Rad-hard	**3 MGy**	**3 MGy**	**?**		**?**
	CERN 2001-006	TOB-NOTE 00.03 (Sep.2000)	Studied for optical properties under limited radiation doses (BaBar)	10 Mrad Test at FNAL Extensively Qualified by SCT	dual cure epoxy In principle should be rad-hard

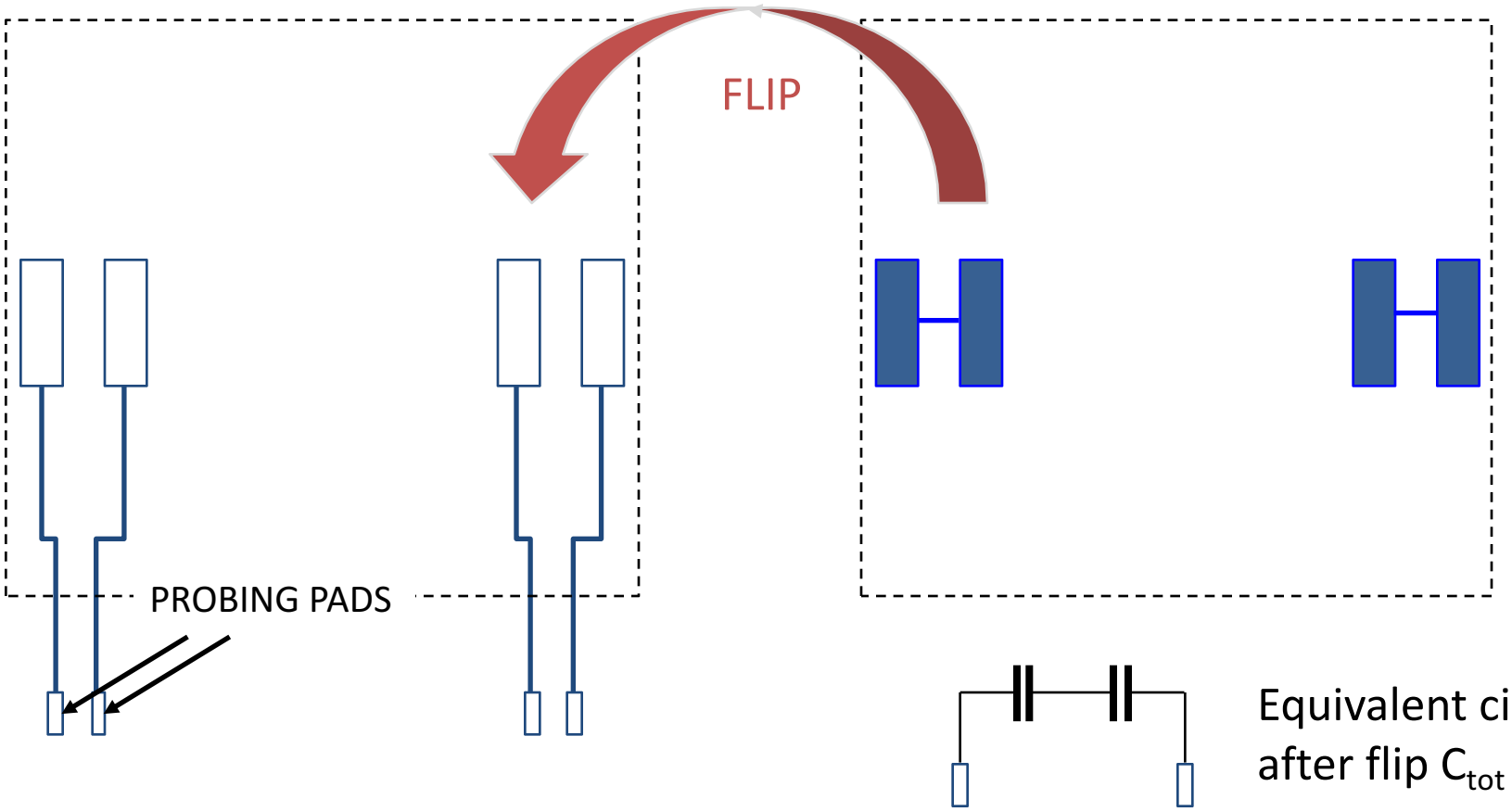
Critical parameters for the process

By G. Darbo

Dummy Assembly

Test pillar and glue process on dummy wafers/chips

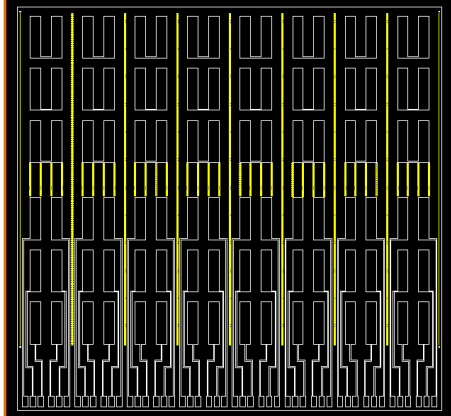
Design a 6-inch wafer with FE-I4 size dummies – place 32 (24) capacitors of 1 (2) mm^2 to test glue thickness uniformity over all surface



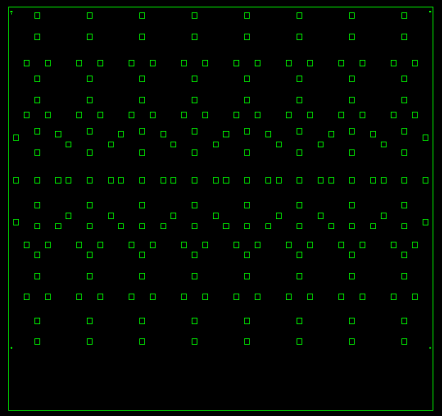
Equivalent circuit after flip C_{tot} = ½ C

Dummy Assembly

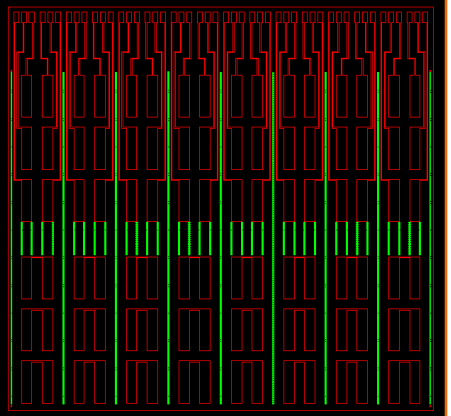
Bottom metal

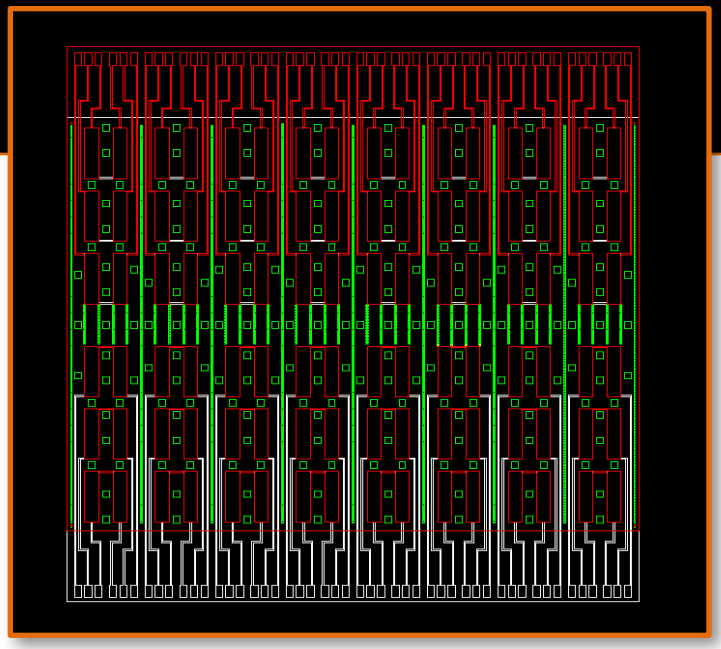


SU8 pillars Mask



Top metal





Conclusions

Bump Bonding

From the results obtained, Selex seems to confirm its abilities in good quality bump deposition also at high densities

- **Very promising results in the first tests from resistive chains of high density bump bonding on 6" wafers:**
  - No "open" amongst 64k bumps (3 chips)
  - No indications of shorts
  - Still flip-chip planarity and matching space accuracy to be improved

Concerning 12" wafers more tests are needed:

- At the moment is ongoing a new design of the resistive chains layout on 12".

Capacitive Couplings

R&D processes look very promising but a lot of work is necessary to come to a mature industrial process, cheaper than bump-bonding

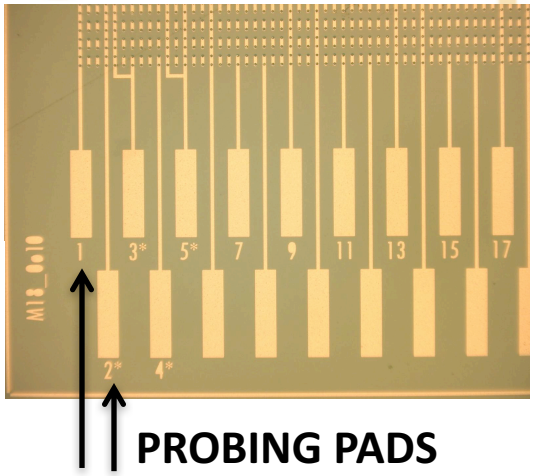
- **Wafer-to-wafer processes** seems ruled out by different size of R/O and HV-CMOS wafers
- **First dummy assemblies will be tested soon**

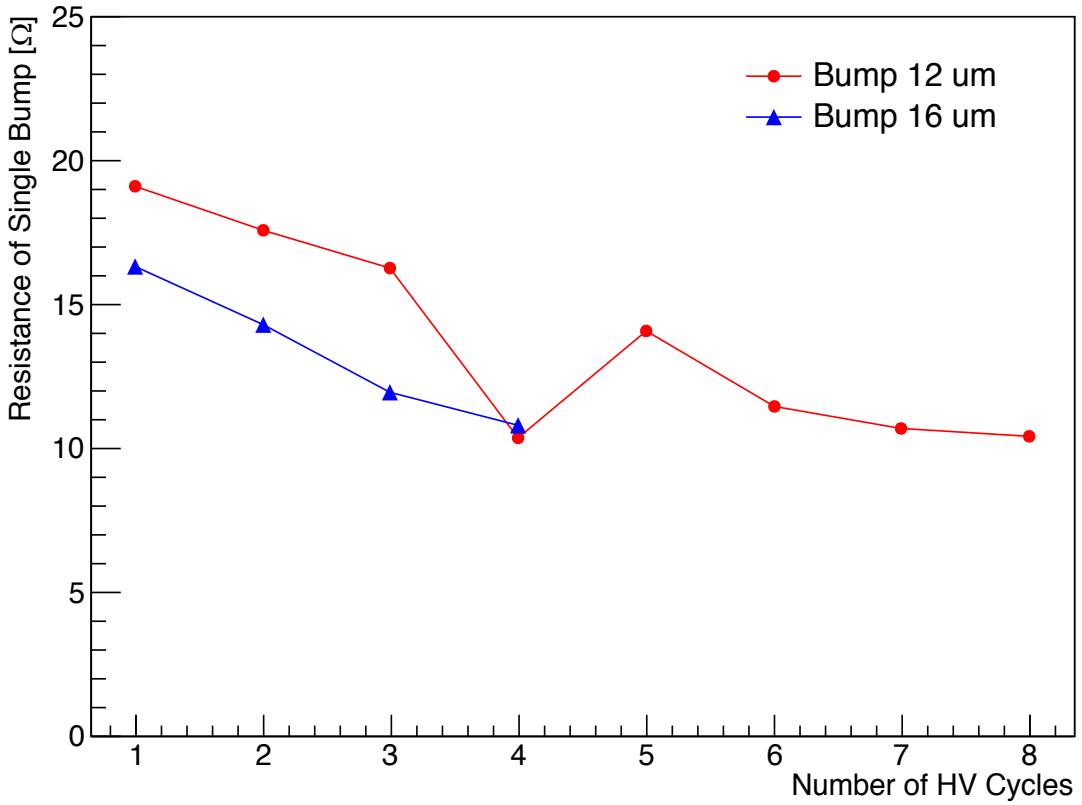
Conclusions

Spare

Flip-Chip Results with 50x50 μm² pitch bumps on 2x2 cm² chips

Measure 124 chains with 172 bumps in series.
Must apply 150 V (I_{max}= 100 μA) to break the native Indium oxide before R-measurement.

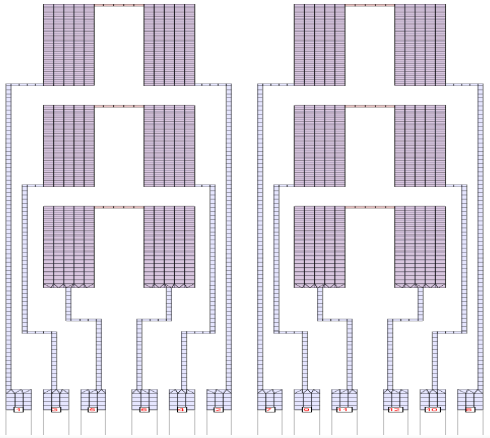


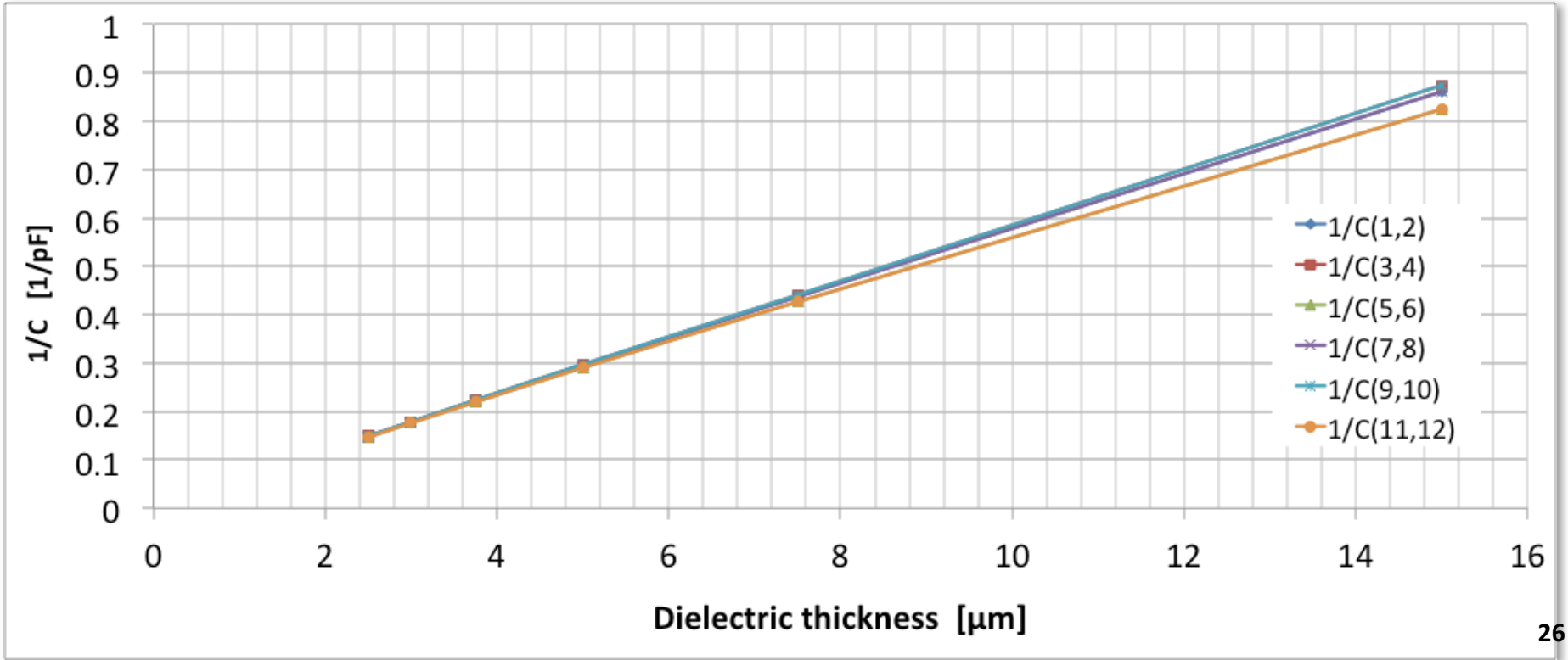


R_{bump}~ 20/17 Ω, it goes down to ~10 Ω after few HV_{150V} cycles

Dummy Assembly

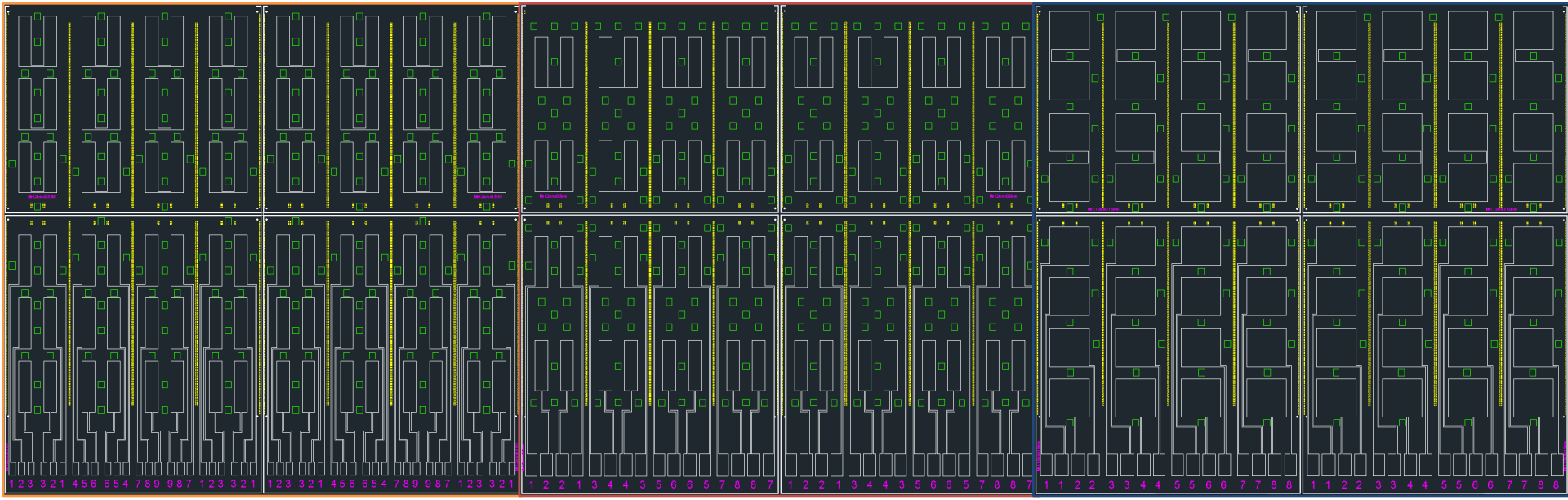
Dielectric	2.5um	3um	3.75um	5um	7.5um	15um
C(1,2)	6,7485	5,6125	4,4937	3,3829	2,2878	1,1613
C(3,4)	6,7267	5,5912	4,4731	3,363	2,268	1,1436
C(5,6)	6,8096	5,6761	4,5565	3,4424	2,3444	1,2124
C(7,8)	6,7485	5,6125	4,4937	3,3829	2,2878	1,1613
C(9,10)	6,7267	5,5912	4,4731	3,363	2,268	1,1436
C(11,12)	6,8096	5,6761	4,5565	3,4424	2,3444	1,2124





Dummy Assembly

Different Layouts



DESIGN 1
48 capacitors
3.6 fF @ 5µ dielectric (ε_r = 3.8)

DESIGN 2
32 capacitors
3.6 fF @ 5µ dielectric (ε_r = 3.8)

DESIGN 3
24 capacitors
~7 fF @ 5µ dielectric (ε_r = 3.8)