Development of n⁺-in-p planar pixel sensor flip-chip modules with quad FE-I4 readout ASIC's

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ATLAS Tracker Layouts



- Current inner tracker
 - Pixels: 5-12 cm
 - Si area: **2.7** m²
 - IBL(2015): 3.3 cm
 - Strips: 30-51 (B)/28-56 (EC) cm
 - Si area: **62** m²
 - Transition Radiation Tracker (TRT): 56-107 cm
 - Occupancy is acceptable for <3x10³⁴ cm⁻²s⁻¹
 - Phase-II at HL-LHC: 5x10³⁴ cm⁻²s⁻¹

- Phase-II upgrade (LF Step1 e.g.)
 - Pixels: 4-27 cm, 5 layers
 - Si area: **16.4** m²
 - Strips: 40.-100 (B) cm, 4 layers
 - Si area: 122 (B)+71(EC)=138 m²
 - Major changes from LHC
 - All silicon tracker
 - Large increase of Si area
 - Pixels: ~ 6 × LHC ATLAS
 - Strips: ~2.2 x LHC ATLAS

Quad FE-I4 ASIC FC module

- Less assembly cost
 - Less parts == larger objects
- ASIC
 - Full reticle size ~ 20 x 20 mm² (in 6-in. wafer)
 - ATLAS IBL: FE-I4 ASIC ^{Ref.[1]} (50x250 μm² pixel, 330x80 pixels, 19x20.2 mm2)
 - Phase-II upgrade: RD53 ASIC (50x50 μm² pixel, 330x400 pixels(?))
- Sensor
 - Large enough but not too large(?)
 - Size: quad FE-I4 ASIC,
 - ≥ 34x41 mm², depending on edge space
- Bumpbonded object
 - called "quad-sensor flipchip (FC)" modules





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Hybrid Planar Pixel Sensor Module



- Advantages:
 - ASIC and Pixel sensor can be optimized independently.
 - Versatility of sensor material
 - could be a real advantage in industry, e.g. infra-red light detection with InGaAs pixels
 - in turn, we (HEP) benefit from the industrialized technology

R&D of Bumpbonding (BB)

- PIXEL2010 Ref.[2]
 - Lead (PbSn) solder bumps
 - Thick Sensor/ASIC: 320 $\mu m/^{\sim}700~\mu m$
 - Basically, no issue
- HSTD8-2011 Ref.[3]
 - Lead-free (SnAg) solder bumps
 - Lead-free is mandatory in industry
 - Observed large bump-resistance
 - Solved with
 - new under-bump-metalization (UBM)
 - together with the removal of surface oxide layer with Plasma etching (top-right Figure)
- 2012-2015
 - Thick sensor/Thin ASIC: 320 μm/150 μm has been successful, but
 - Thin sensor/Thin ASIC: 150 μm/150 μm, and four ASIC's
 - Observed disconnected bumps in large area
 - Then, sequence of R&D's ... this report



Bumpbonding technology in HPK

- BB objects:
 - ASIC's with UBM+bumps
 - Sensor with UBM
- BB steps:
 - Vacuum-chuck jig (top&bottom) to hold and flatten the object
 - Jig size: 20 x 20 mm² = one FE-I4 size
 - ASIC's are bump-bonded one-by-one, with heat process while bumping
- Issues identified:
 - Warpage of objects
 - Surface oxidation
 - Application of plasma-etching (PE) was effective but oxidated after certain time after PE, then observed BB deficiency
 - Not only of SnAg bumps but also of the UBM on sensor
 - UBM of sensor experiences several times of heating – multi-chip bumpbonding



Warpage

• Bi-metal effect

- Coeff. of thermal exp.:
 - Bulk (Si):Surface passivation (SiO2)= 2.8-7.3 : 0.51-0.58 ppm/K
 - Oxidation process (high temp.) → room temp
- Warpage ~ (thickness)~³
 - Sensor: 320 \rightarrow 150 µm : 3 \rightarrow 25 µm
- Flatness in BB
 - HPK's BB uses vacuum-chuck jig to flatten the object
 - cf. Temporarily support wafer (thick glass) attachment and removal
 - Warpage needs to be <<BB gap (~20 μ m)
 - ASIC (150 μm , after reflow of bump deposition) ~40 μm
 - Another way of helping flattening Deposition of compensation layer to backside of ASIC – effective but seems unnecessary

(Active face top)	Free	After reflow	Vacuum chuck
Sensor (150 μm)	~30 µm凸	N/A	~5 µm凸凹
Sensor (320 μm)	~3 µm凸凹	N/A	N/A
ASIC (150 μm)	~10-15 µm凹	~50 µm凹	~5 µm凹
ASIC (150 μm)+Backside compensat'n	~10 µm凸凹	~10 µm凸凹	~8 µm 凸凹





Identifying and solving the issue of surface oxidation

• R&D's

- Using solder flux, Indium BB, Hydrogen-reflow

	Method	Quad samples (#ASIC's)	Bump (ASIC)	ASIC
1	Solder flux, with/without	2 (8), 1 (4)	SnAg	Bump
2	Indium BB	3 (12), 4 (16)	ln, Ni-In	UBM
3	Hydrogen-reflow	4 (16)	SnAg	Sensor

- Validation
 - Thermal cycling (TC): [-40, +40]°C, 5 times
 - Irradiation (IR): $3x10^{15}$ neq/cm² at -15 °C
 - Irradiated spot is heated to several 10 °C, induces thermal stress
 - ⁶⁰Co β source response for bump connection test (SS)

Solder flux

- Solder flux is known to remove surface oxidation
 - in retrospect, both surfaces (ASIC and sensor)
- Validation
 - Sample of "No flux" showed large-area bump disconnection in number of chips.
 - Samples "With flux" developed no largearea bump disconnection, in 2 quadsensor FC's (8 ASIC's)
- Additional validation
 - Concerns:
 - Amount of flux issue of BB QC
 - Residue after cleaning ditto
 - tested in another one sample
 - TC [-40,+85]°C, 100 times passed
 - Temp-Humidity test [+40°C, RH90%], 1000 hrs passed, no short between pixels

SS after irrad. KEK98 (No flux)





Indium BB

- Indium BB is a well-established technology.
 - (relatively) insensitive to surface oxidation
- Two indium bumps tried:
 - (1) Indium ball (abbreviated as "In")
 - (2) Ni-pillar + Indium cap ("Ni-In")
 - Reducing amount of In. for reducing cost and chance to capturing sharp-angle debris
- Validation
 - No large area bump disconnection in 7 quad-sensor FC's (28 ASIC's)

SS after irrad. – KEK97



Hydrogen-reflow SnAg

- No solder flux
- Hydrogen-radical reflow process
 - A technology to deoxidize the surface with Hydrogen-radicals (H*)
 - $4H^* + SnO_2 \rightarrow Sn + 2H_2O$
 - $2H^*+SnO \rightarrow Sn + H_2O$
 - Applied to the objects just before BB
 - Equipment is small enough to use at next to BB machine (No with plasma-etching)
- Validation
 - No large-area bump disconnection in 4 quad-sensor FC's (16 ASIC's)
 - In addition, we have had additional 16 single-sensor FC's (16 ASIC's) – No large area disconnections.
- HPK has established a technology for large-volume production of thin/ thin (150/150 μm) with SnAg bumps successfully.

SS after irrad. – KEK107



Evaluation with beams



Quad: TypeB Pixel: Type19 Gang: 3

- POSTER by K. Nakamura
- Irrad.: 2.7x10¹⁵ neq/cm²
- Under the traces ganging pixels, efficiency loss is confirmed at the boundary of pixels; little loss over pixels, as expected.
 - − still eff. loss $\leq 1\%$
- Also, little loss in non-irrad. module.
- Explanation:
 POSTER by Y. Unno and R. Hori

Summary

- We have produced 5th-1 wafer layout in a 6-in. wafer with 7 large-format of quad-FE-I4 n⁺-in-p pixel sensors.
 - Pixel structures are adapted the designs of PolySi biasing resistor network mitigating the efficiency loss at the pixel boundary, together with those without biasing network for a reference.
- We have worked on the bumpbonding of thin (150 μm) sensor and thin (150 μm) ASIC's with lead-free (SnAg) bumps.
 - We have encountered BB deficiency of large-area bump disconnections, after thermal stress including irradiation.
 - The deficiency is identified to be caused by several factors: warpage, surface oxidation, multi-chip bumpbonding.
 - Warpage is mitigated with a better vacuum-chuck jig, without support wafer.
 - The surface oxidation is identified as a fundamental source of the issue with sequence of R&D's and solved, with using solder flux, with indium BB, or applying Hydrogen-radical reflow to the objects just before the bumpbonding in SnAg Bumps.
 - We have established a technology for large-volume production of thin/thin ASIC/sensor multi-chip flux-less SnAg bumbponding.

References & Contributors

References

[1] M. Garcia-Siveres et al., Nucl. Instr. Meth. A636 (Suppl.) (2011) S155-S159
[2] Y. Unno et al., Nucl. Instr. Meth. A650 (2011) 129-135
[3] Y. Unno et al., Nucl. Instr. Meth. A699 (2013) 72-77
[3] Y. Unno et al., Nucl. Instr. Meth. A831 (2016) 122-132

ATLAS-Japan Silicon Group

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Corniglia, Cinque Terre, photo by Y. Unno

Backup Slides

Particle fluences in ATLAS

- ATLAS detector to design for
 - Instantaneous lum.: 7x10³⁴ cm⁻²s⁻¹
 - Integrated lum.: 6000 fb⁻¹ (including safety factor 2 in dose rate)
 - Pileup: 200 events/crossing
- PIXELs (HL-LHC)
 - Inner: r=3.7 cm ~2.2x10¹⁶
 - Medium: r = 7.5 cm, ~6x10¹⁵
 - Med/Out: r=15.5 cm ~2x10¹⁵
 - Outer: r = 31 cm (?) 15
 - Charged:Neutrons ≥ 1
- STRIPs (HL-LHC)
 - Replacing Strip and TRT
 - Short strip: r = 30 cm, e.g.
 ~1x10¹⁵
 - Long strips: r = 60 cm,
 ~5×10¹⁴
 - Neutrons: Charged ≥ 1
- IBL (LHC)
 - Insertable B-layer pixel
 - r = 3.3 cm
 - Flunece ~3x10¹⁵ neq/cm²
 - at Int.L~300 fb⁻¹



Towards "Flux-less" SnAg BB

- Issue in making good solder wetness is "removing surface oxide at the time of bumpbonding (BB)"
 - How can it be done?
 - Panasonic in literature:
 - M. Matsumoto et al., "High-Speed Reduction of Oxide Film Using Atmospheric-Pressure Inductively Coupled Microplasma Jet", Panasonic Technical Journal Vol. 57 No. 2 Jul. 2011
 - Perhaps, the Panasonic Bumpbonder is equipped with this device



Ar plasma \rightarrow Ar/H₂ \rightarrow H* radical SnO₂ + 4H* \rightarrow Sn + 2H₂O SnO + 2H* \rightarrow Sn + H₂O

HPK has a similar device and will try in the next SnAg BB.

第1図 誘導結合型大気圧マイクロプラズマジェット

Fig. 1 Atmospheric-pressure inductively coupled microplasma jet