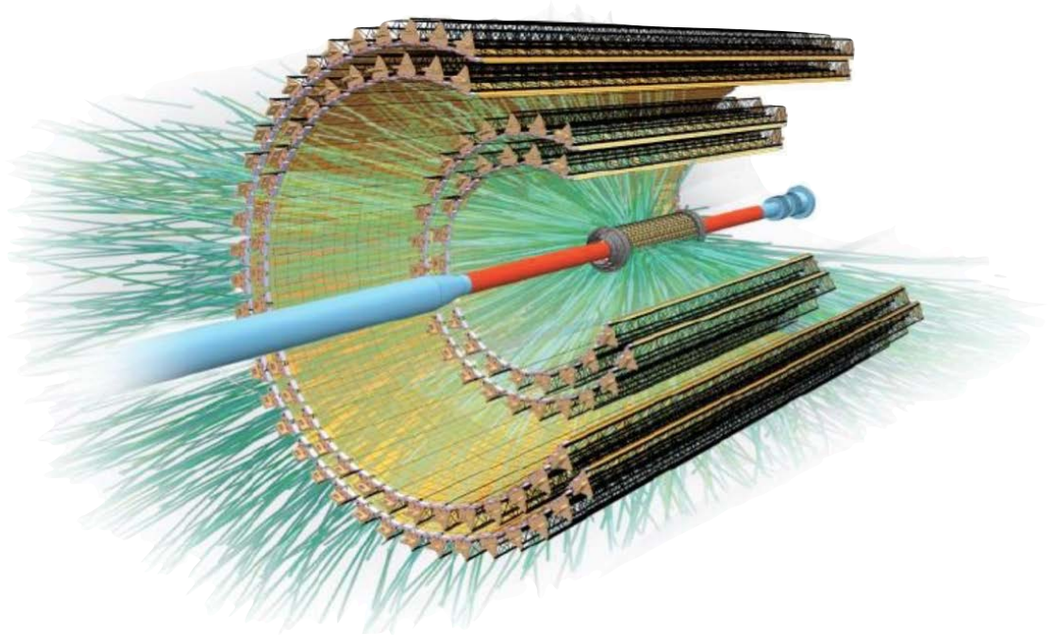
ALICE



The ALICE Inner Tracking System Upgrade

Felix Reidt
CERN

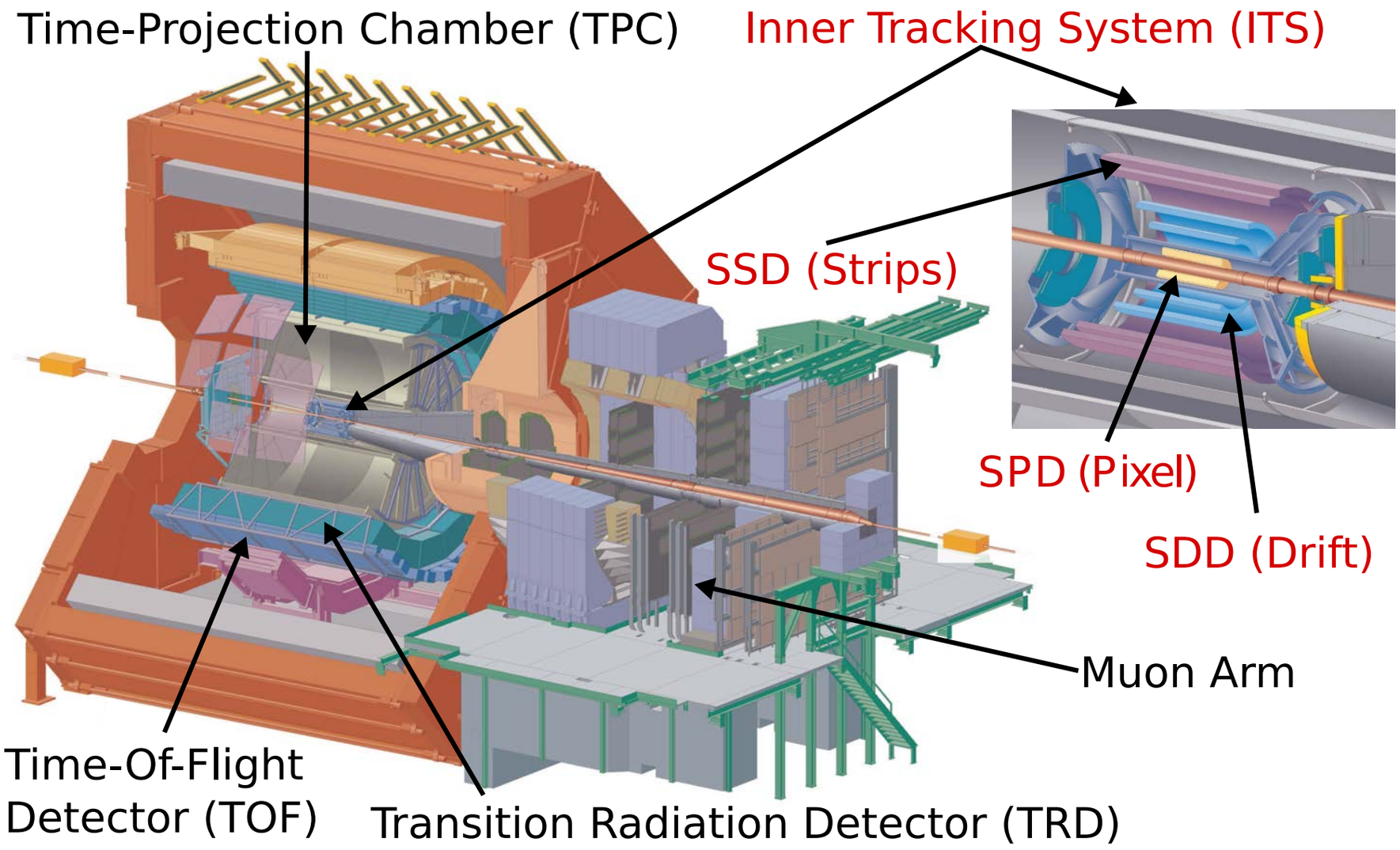
on behalf of the ALICE collaboration

CERN

Outline

- ALICE
- Inner Tracking System (ITS) Upgrade
- Pixel Chip
- Detector Staves
- Production
- Readout Electronics
- Project Timeline
- Summary and Outlook

A Large Ion Collider Experiment (ALICE)



- ALICE is the heavy-ion focussed experiment at the LHC
- Its main goal is to study the Quark-Gluon Plasma (QGP)
- 2 layers each of silicon pixel, silicon drift and silicon strip detectors

Upgrade Strategy for LS2 (2019/2020)

Motivation:

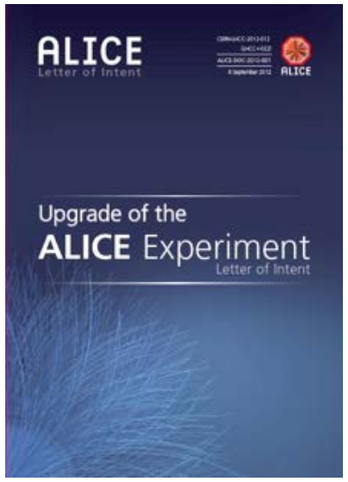
High-precision measurements of rare probes at low p_T
- Cannot be selected by hardware triggers
- Need to record large minimum-bias data sample
  ⇒ read out all Pb-Pb interactions up to the maximum LHC Pb-Pb collision rate of 50kHz

Goal:

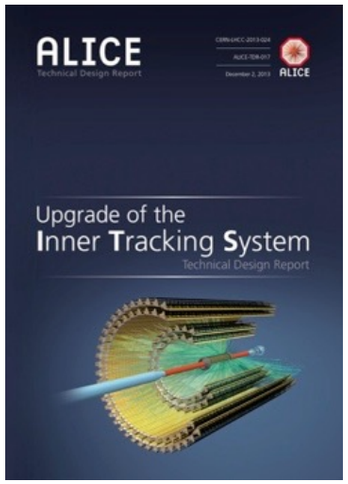
- Pb-Pb recorded luminosity: 10 nb^{-1} (plus pp and p-A data)
  → gain factor 100 in statistics for minimum-bias trigger
- Improved vertexing and tracking capabilities

Strategy:

- New silicon trackers:
  - New, smaller beam pipe
  - Inner Tracking System (ITS) covering mid-rapidity
  - Muon Forward Tracker (MFT) covering forward rapidity
- Further upgrades:
  - TPC (readout planes and electronics)
  - Forward trigger detectors (FIT) and ZDC
  - Readout electronics (TRD, TOF, PHOS, Muon Arm)
  - Upgrade of online and offline systems (O^2 project)



ALICE upgrade LoI: March 2013

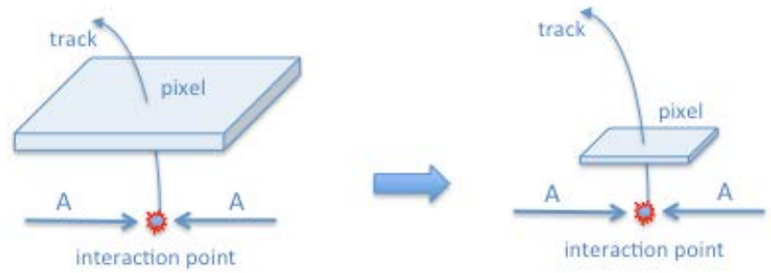


ITS upgrade TDR: March 2014

ITS Upgrade Design Objectives

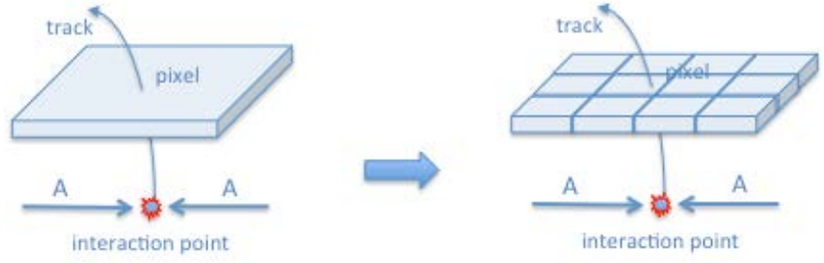
Improve impact parameter resolution by a factor ~3 in rφ and ~5 in z at p_T=500MeV/c

- get closer to IP: 39mm ➔ 23mm (innermost layer)
- reduce material budget: ~1.14% X_0 ➔ ~0.3% X_0 (inner layers)
- reduce pixel size: 50x425μm² ➔ O(30x30μm²)



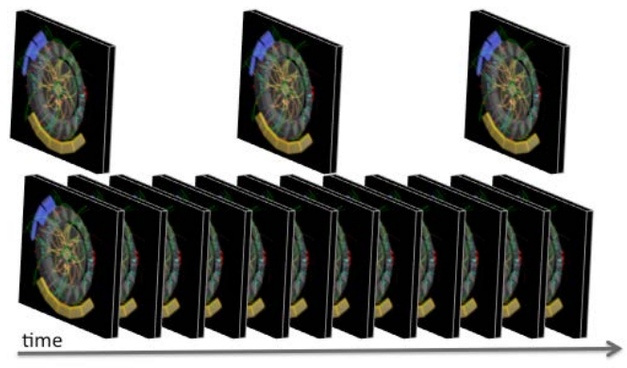
Improve tracking efficiency and p_T resolution at low p_T

- increase granularity: 6 layers ➔ 7 pixel layers



Fast readout

- readout of Pb-Pb at up to 100 kHz (presently 1kHz) and 400kHz for pp

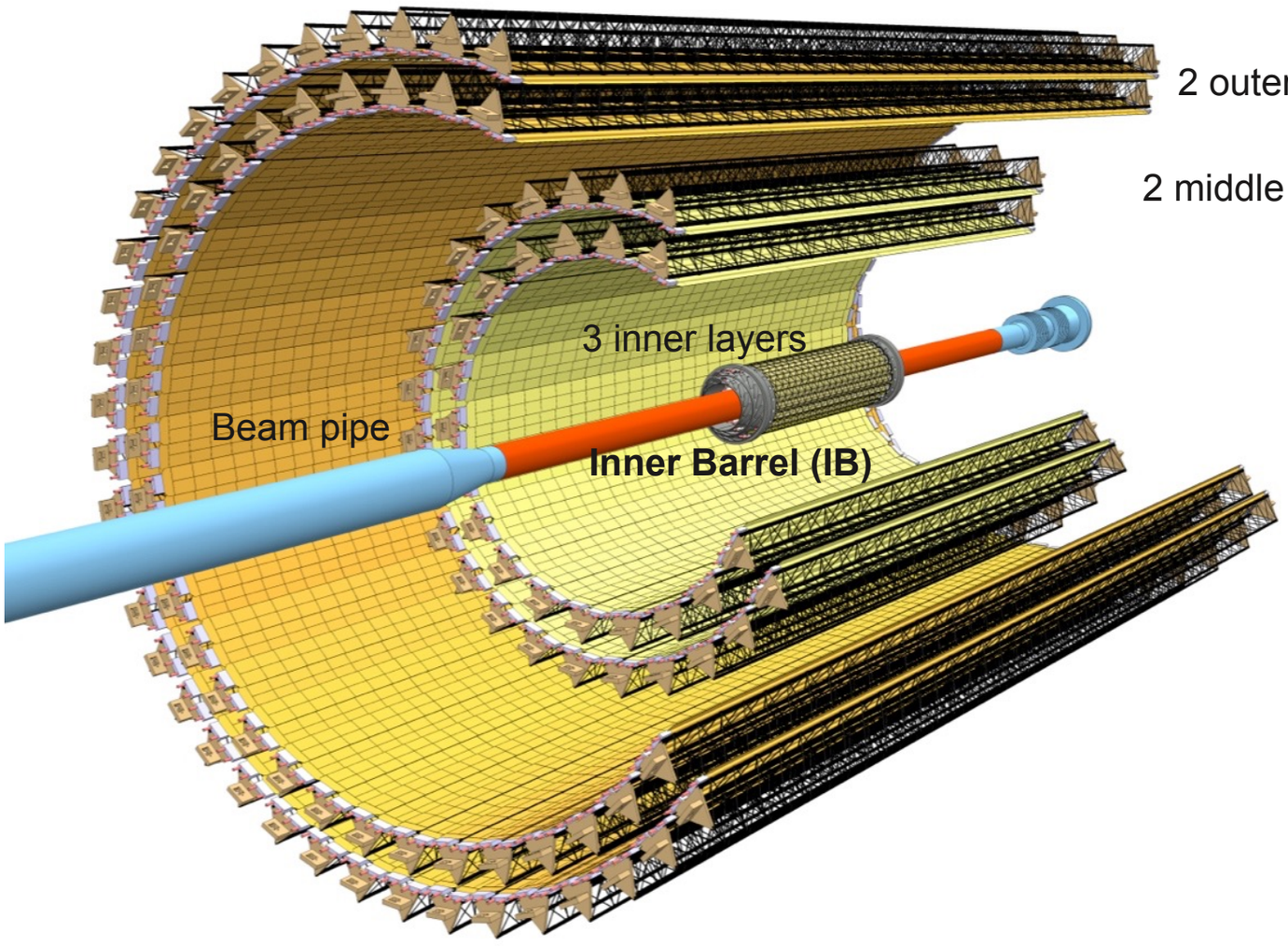


Fast insertion and removal

- possibility to replace non-functioning detector modules during yearly shutdown

➔ present ITS will be fully replaced!

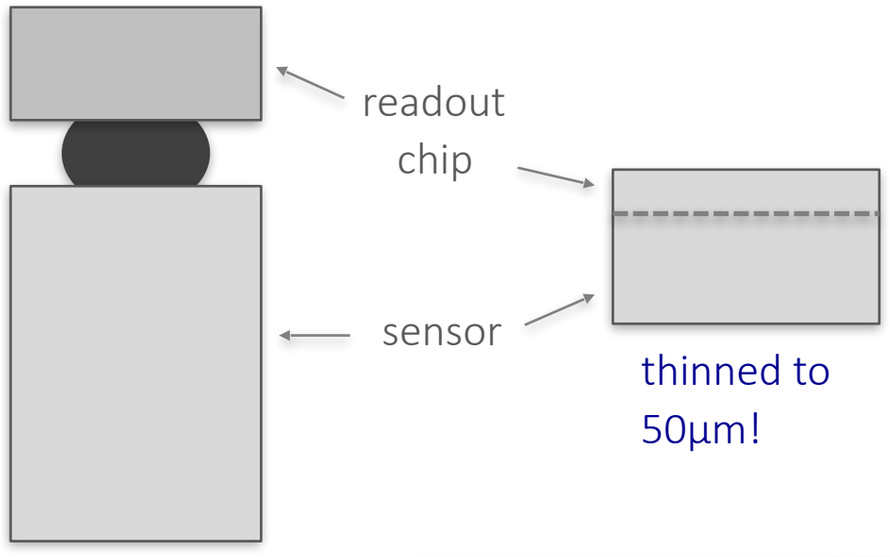
The Upgraded ITS



- 7 layers
- 12.5 Gigapixels
- Binary readout
- ~ 10 m^2 active surface

Fully equipped with Monolithic Active Pixel Sensors (MAPS)

hybrid → monolithic



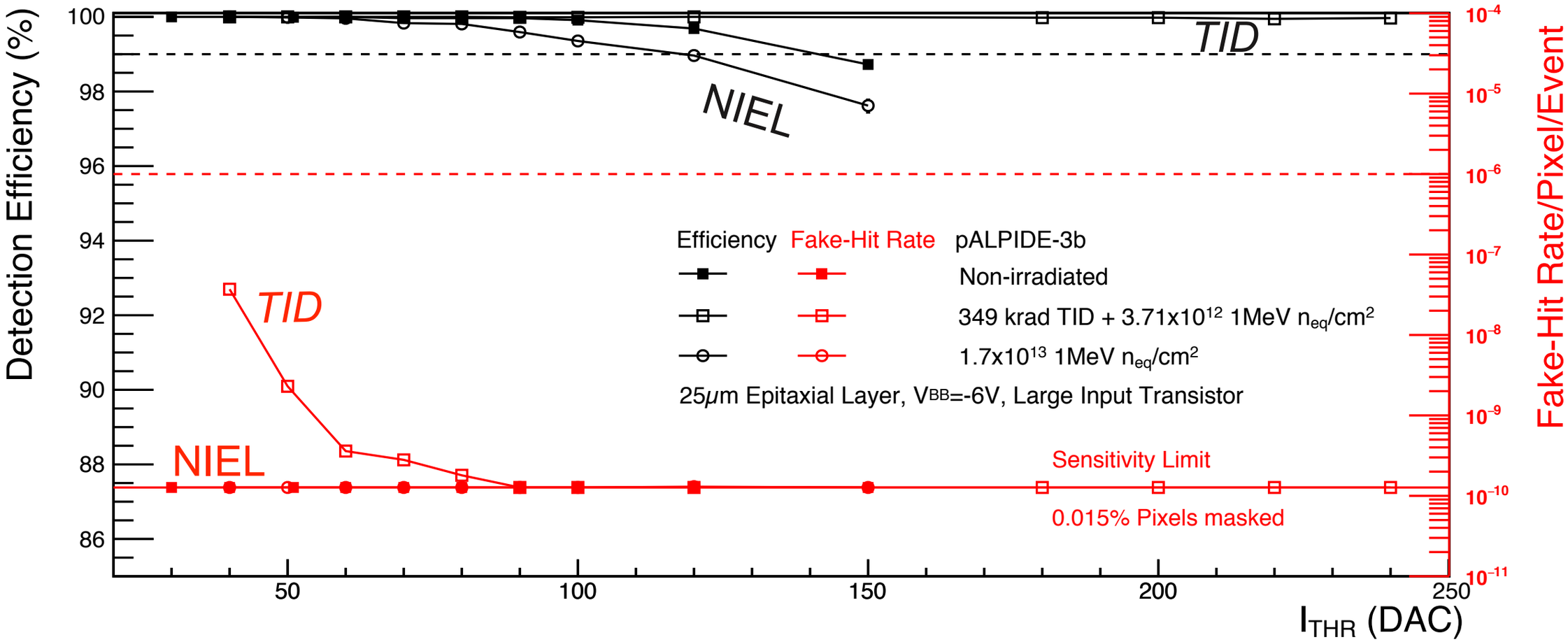
Pixel Chip Requirements

Pixel chip development for the ITS Upgrade

Parameter	Inner Barrel	Outer Barrel	ALPIDE
Silicon thickness	50µm	100µm	✔
Spatial resolution	5µm	10µm	~ 5µm
Chip dimension	15mm x 30mm		✔
Power density	< 300mW/cm^2	< 100mW/cm^2	< 40mW/cm^2
Event-time resolution	< 30µs		~ 2µs
Detection efficiency	> 99%		✔
Fake-hit rate *	< 10^{-6}/event/pixel		<<< 10^{-6}/event/pixel
NIEL radiation tolerance **	1.7x10^{13} 1MeV n_{eq}/cm^2	10^{12} 1MeV n_{eq}/cm^2	✔
TID radiation tolerance **	2.7Mrad	100krad	tested at 350krad

* revised numbers w.r.t. TDR
** including a safety factor of 10, revised numbers w.r.t. TDR

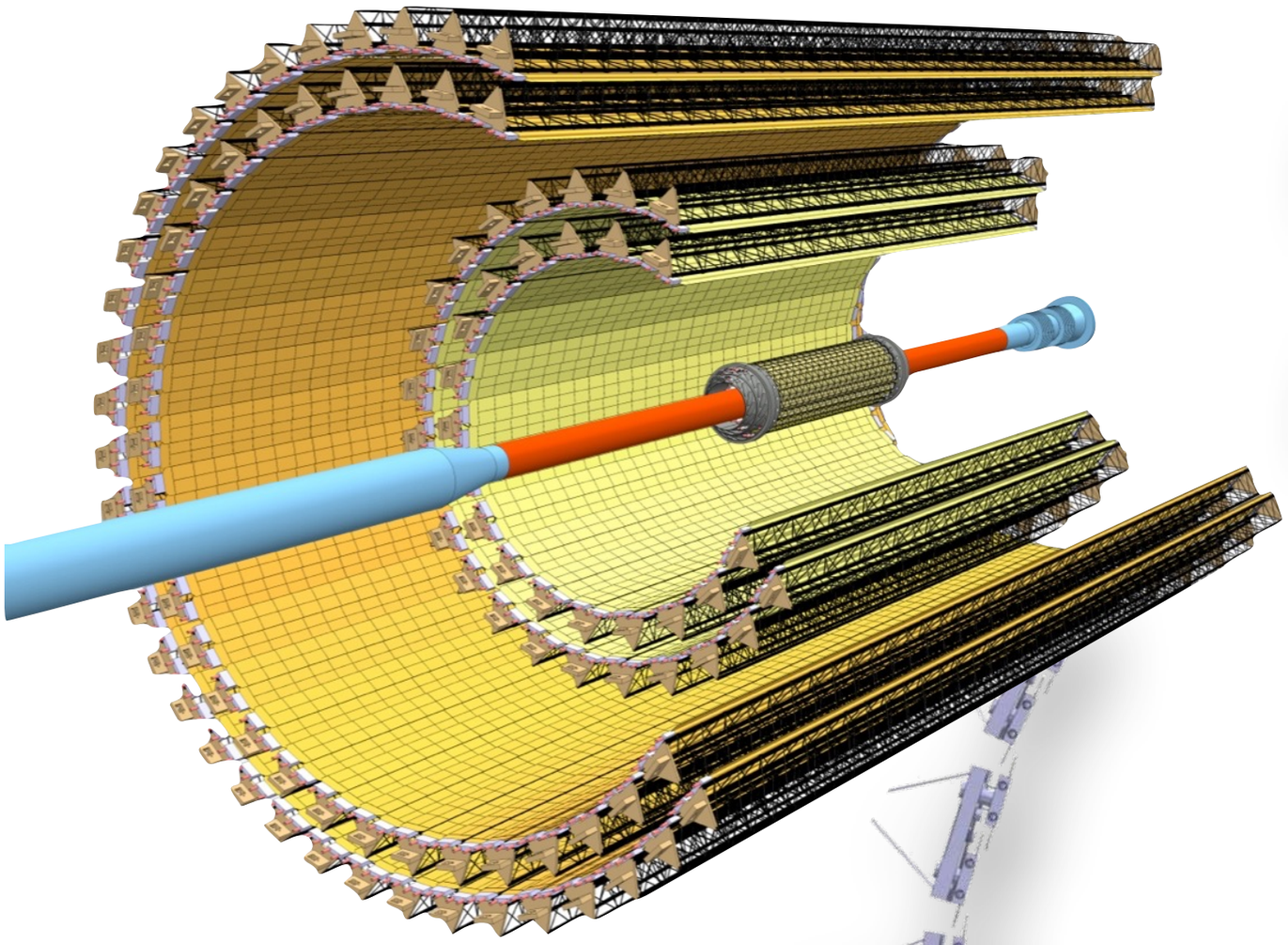
Test Beam Result of a Full-Scale ALPIDE Prototype

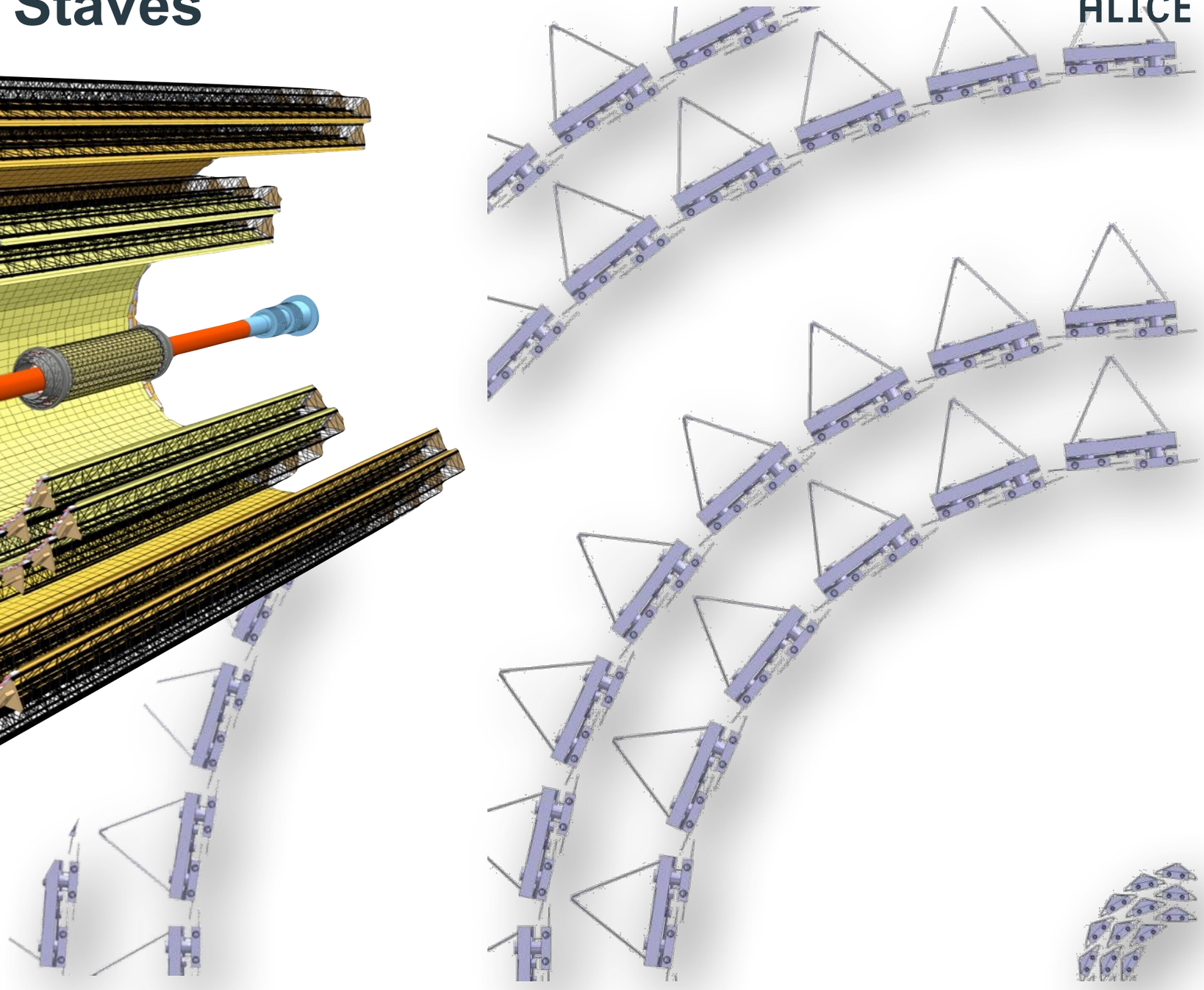


- Final pixel layout and front-end circuit selected
- Radiation effects visible
- Large operational margin maintained after NIEL and TID irradiation

Further details in **Miljenko Šuljić's talk** on Thursday

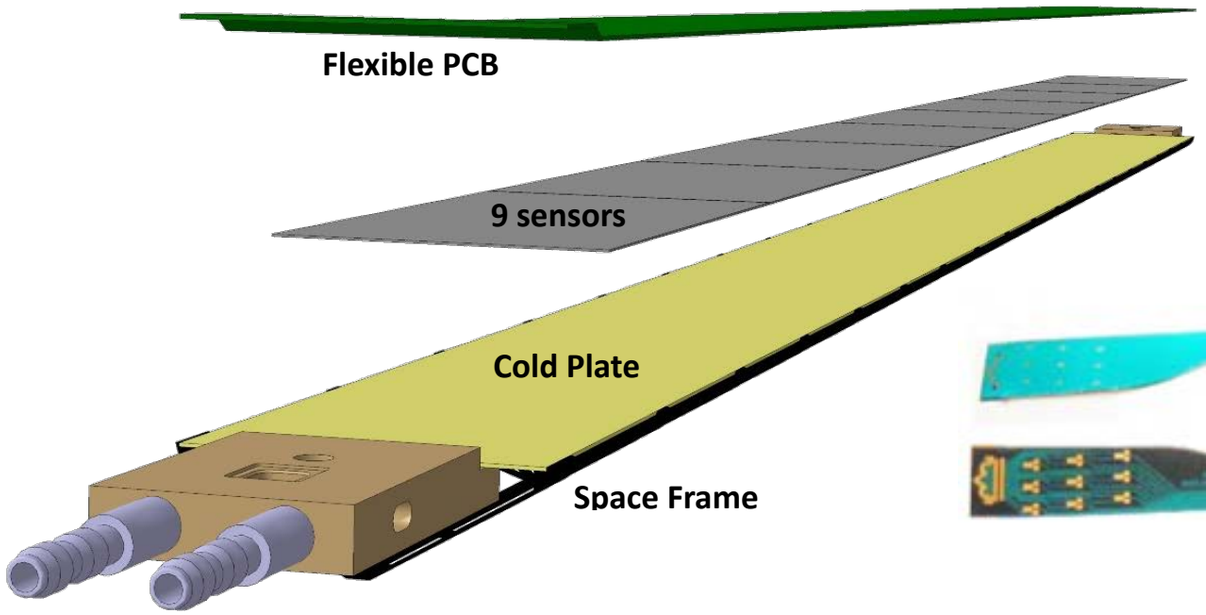
Detector Barrel Staves



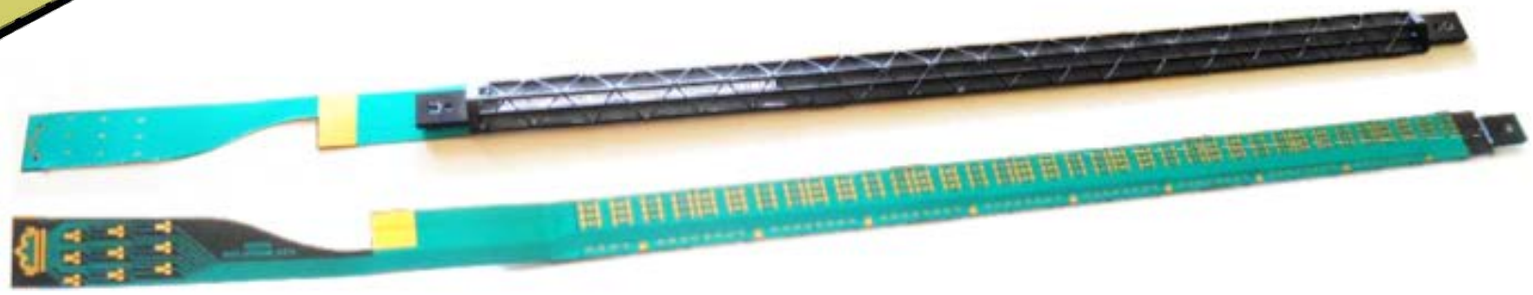


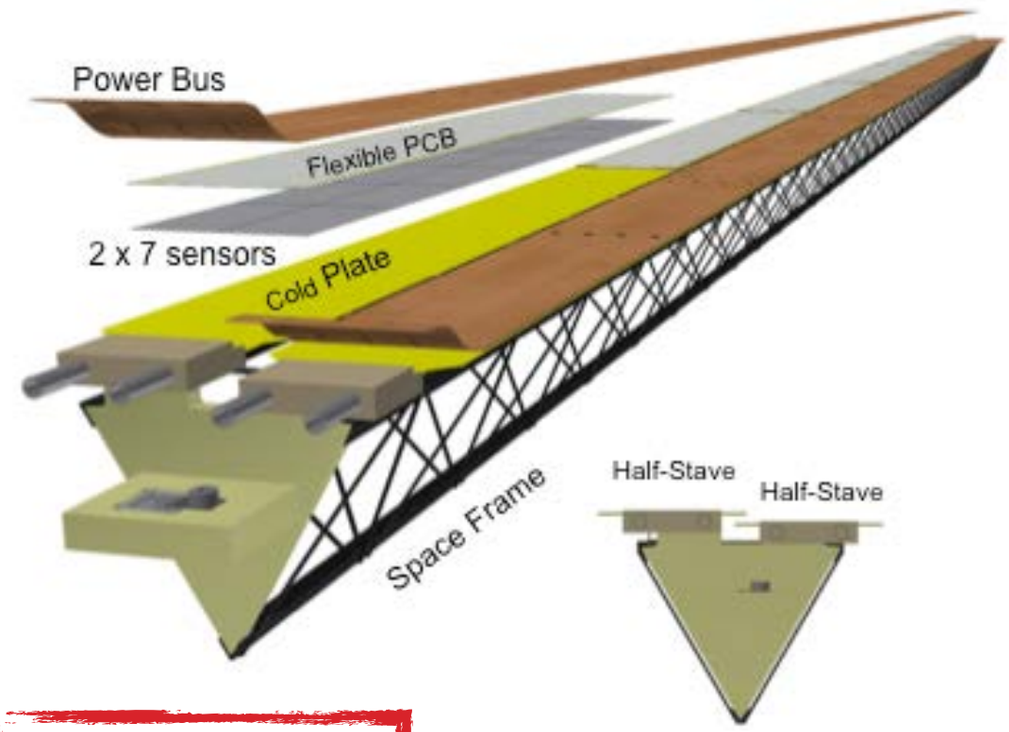
Layer #	6	5	4	3	2	1	0
n. of Staves	48	42	30	24	20	16	12

Stave Layout

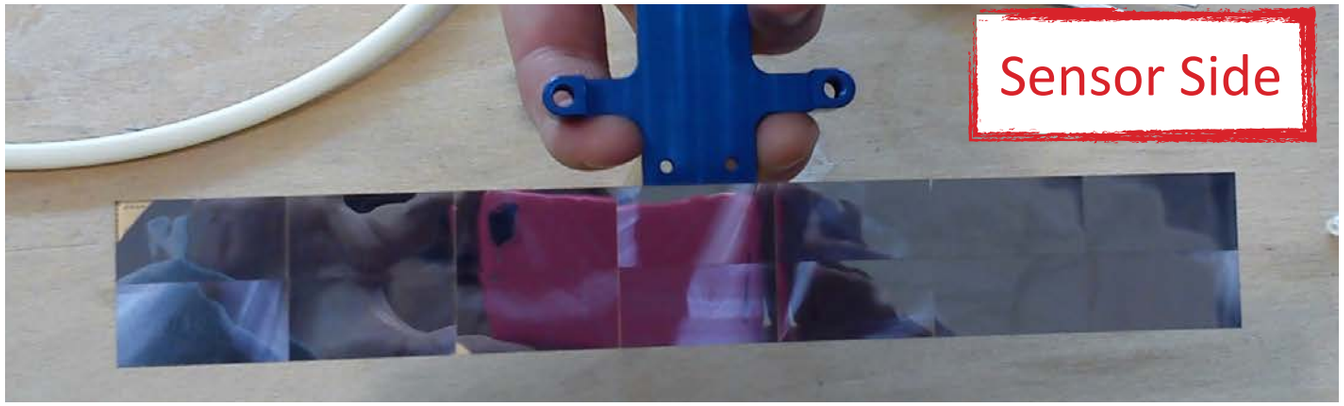


Inner Barrel

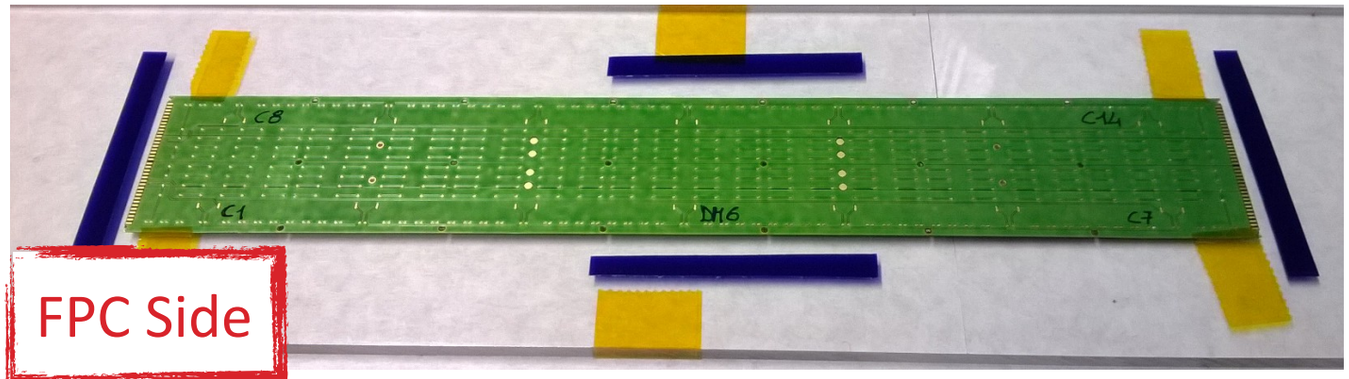




Outer Barrel



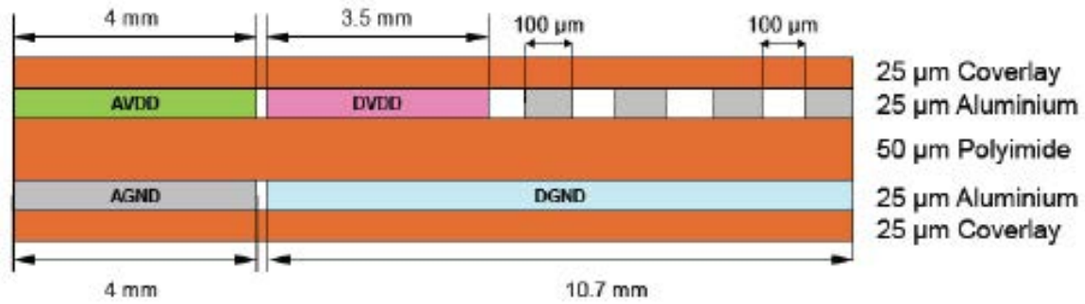
Sensor Side

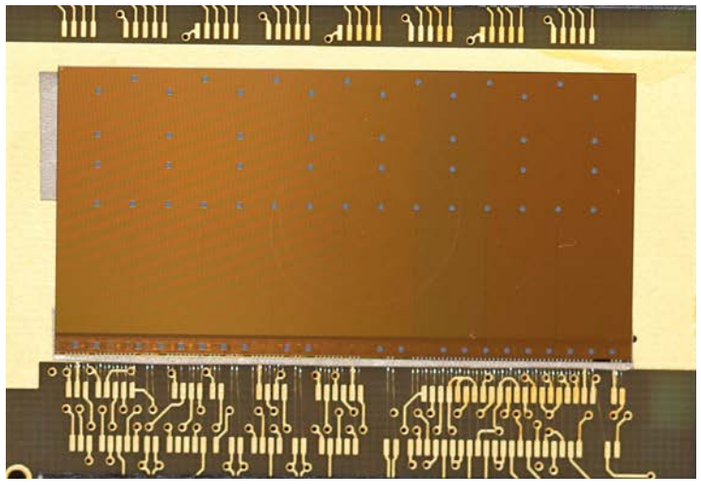


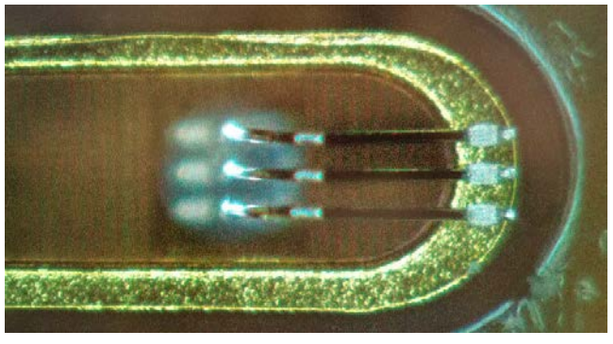
FPC Side

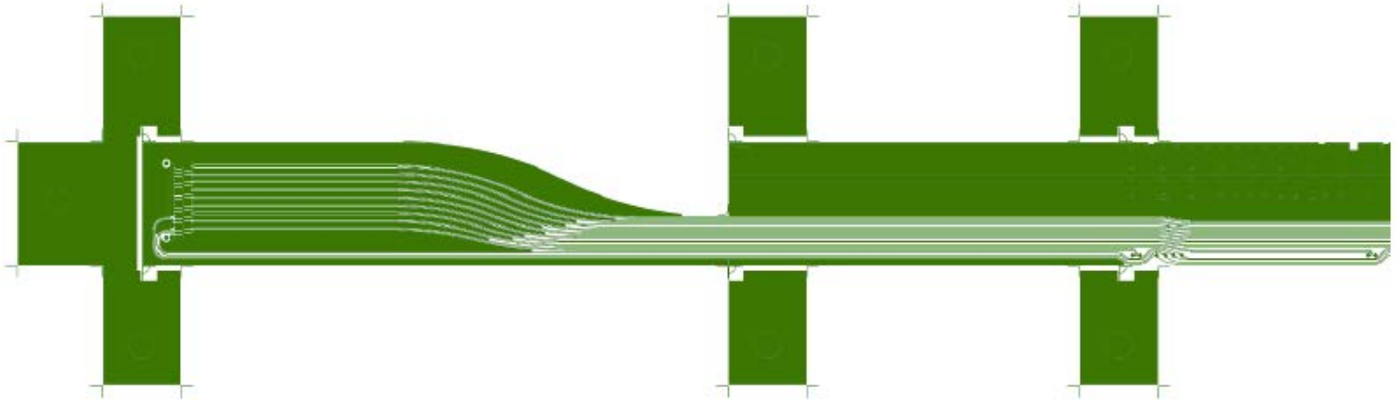
IB Flexible Printed Circuit

- Flexible printed circuit (FPC) of low-CTE polyamide and aluminium
- Power planes for digital and analogue voltage
- 11 differential pairs (clock, configuration, 9 data lines)
- Pads distributed over the full chip
- Connection with wire bonds through vias in the FPC





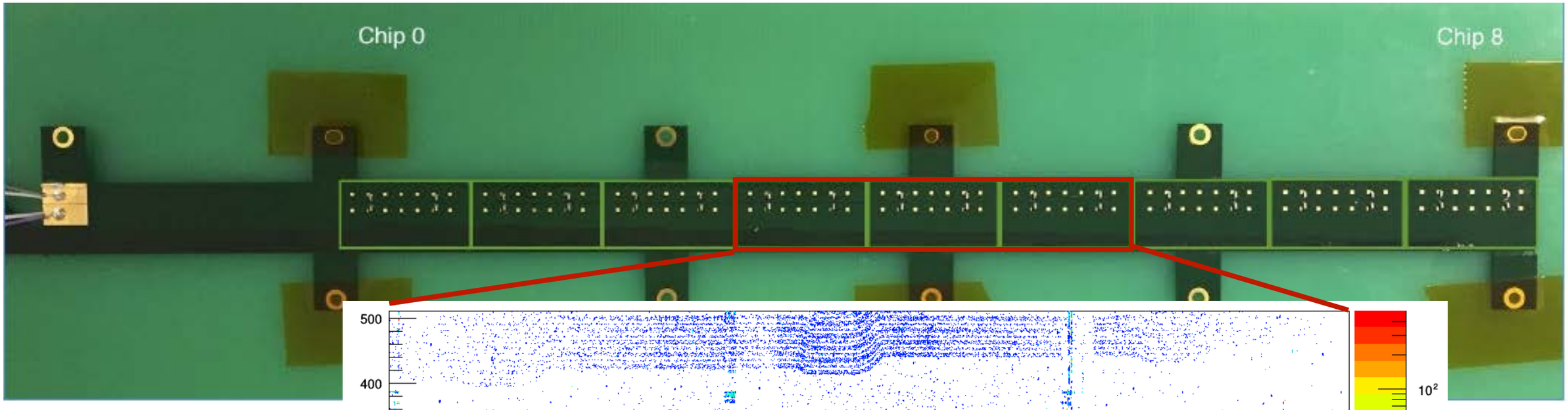


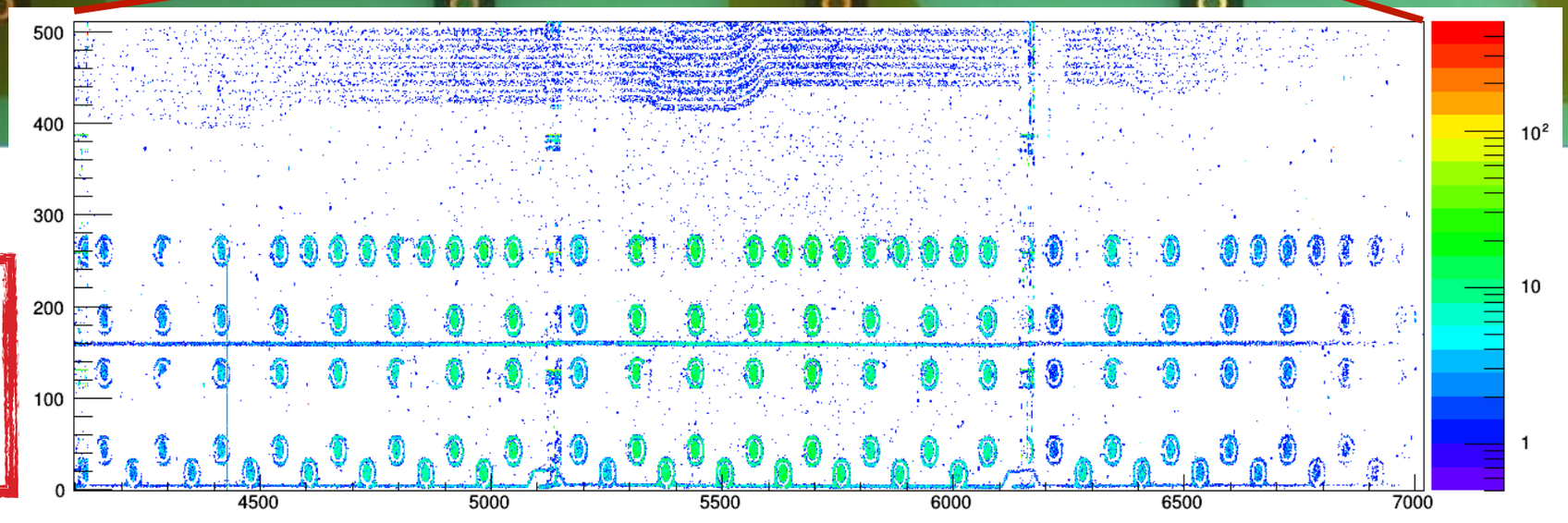


IB Hybrid Integrated Circuit Prototypes

Small series of Inner Barrel Hybrid Integrated Circuit (HIC) prototypes built using pALPIDE-3 chips

- 4 HICs and 2 staves
- Full characterisation with different modes of operation, readout rates and environmental conditions (supply voltages and temperature)
- Sensor performance comparable to single chip

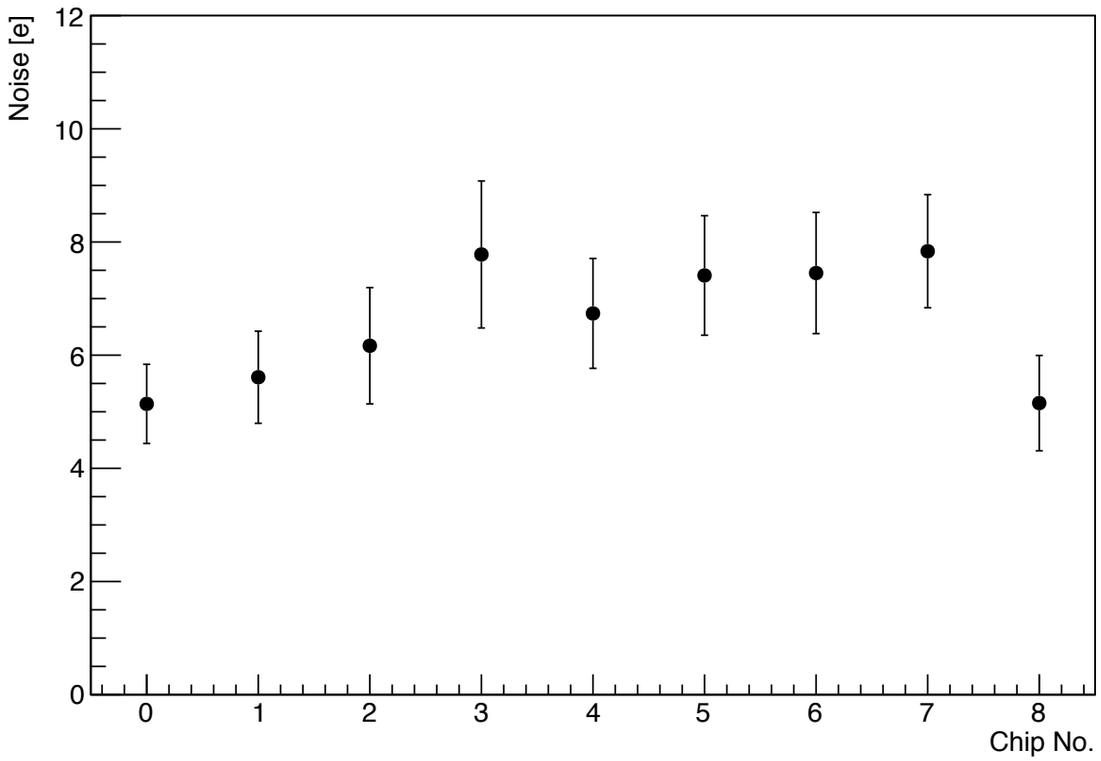


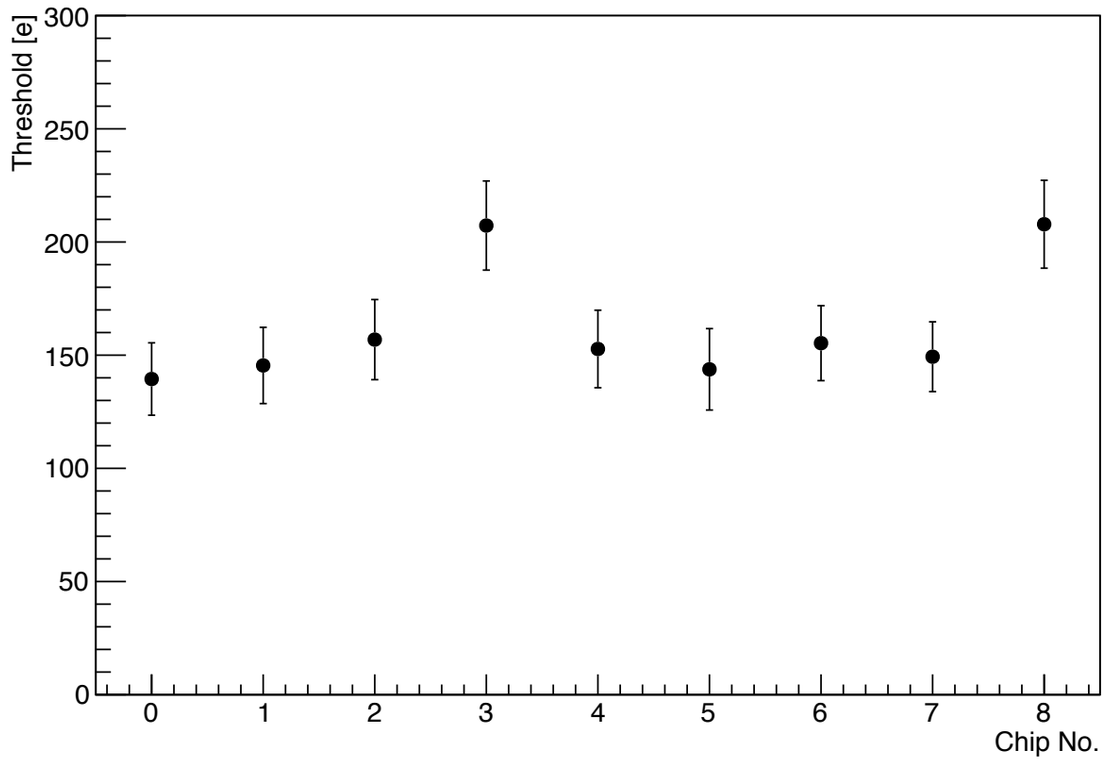


X-ray (^{55}Fe) image of the HIC

IB HIC Test Results - Threshold and Noise

- Average threshold and noise values from S-Curve scans for all chips on the IB HIC
- Error bars indicate RMS of the distributions

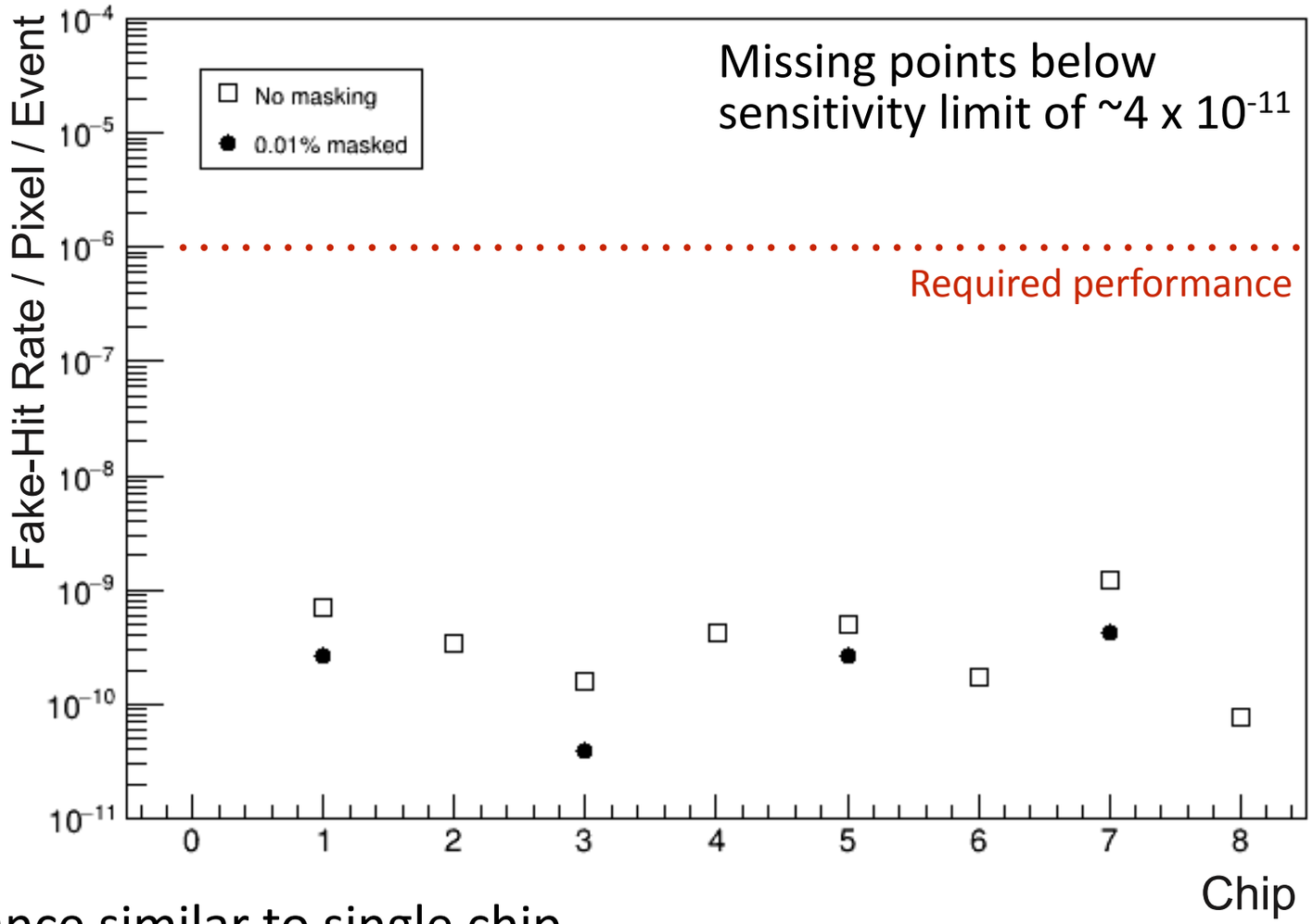




- Performance compatible to single chips
- Noise of about 7 electrons also on the HIC
- No systematic effect due to the presence in a module observed

IB HIC Test Results — Fake-Hit Rate

- Measurement of fake-hit rate
- Different levels of masking:
  - no masking
  - 0.01% of pixels masked

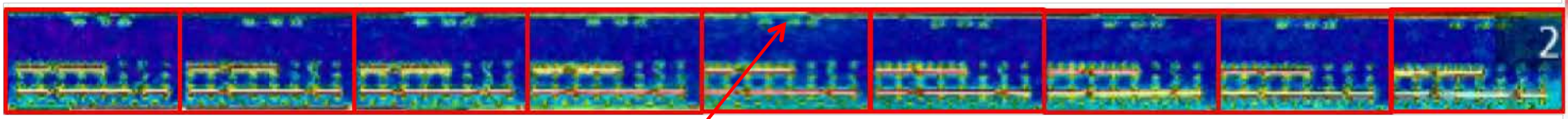


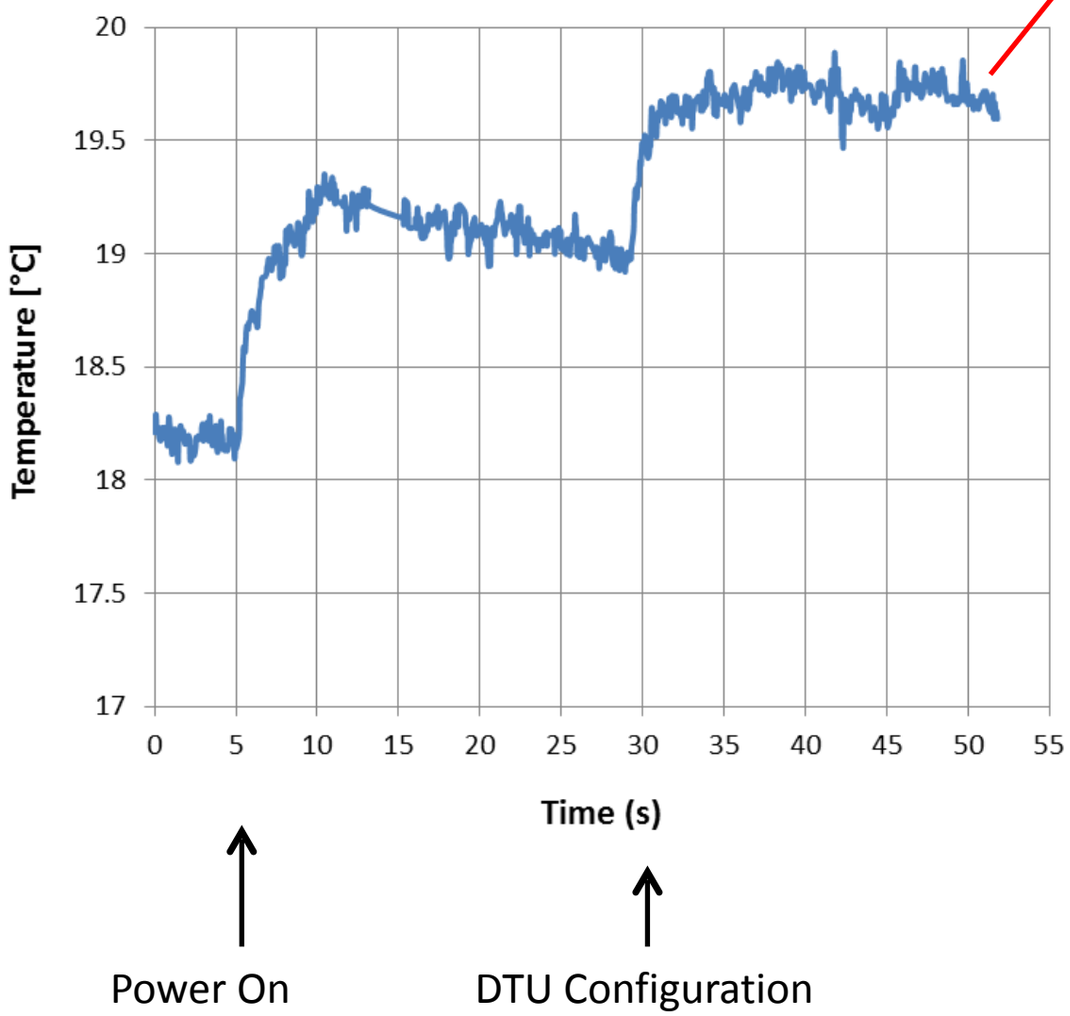
- Performance similar to single chip
- Noise occupancy orders of magnitude better than the requirement

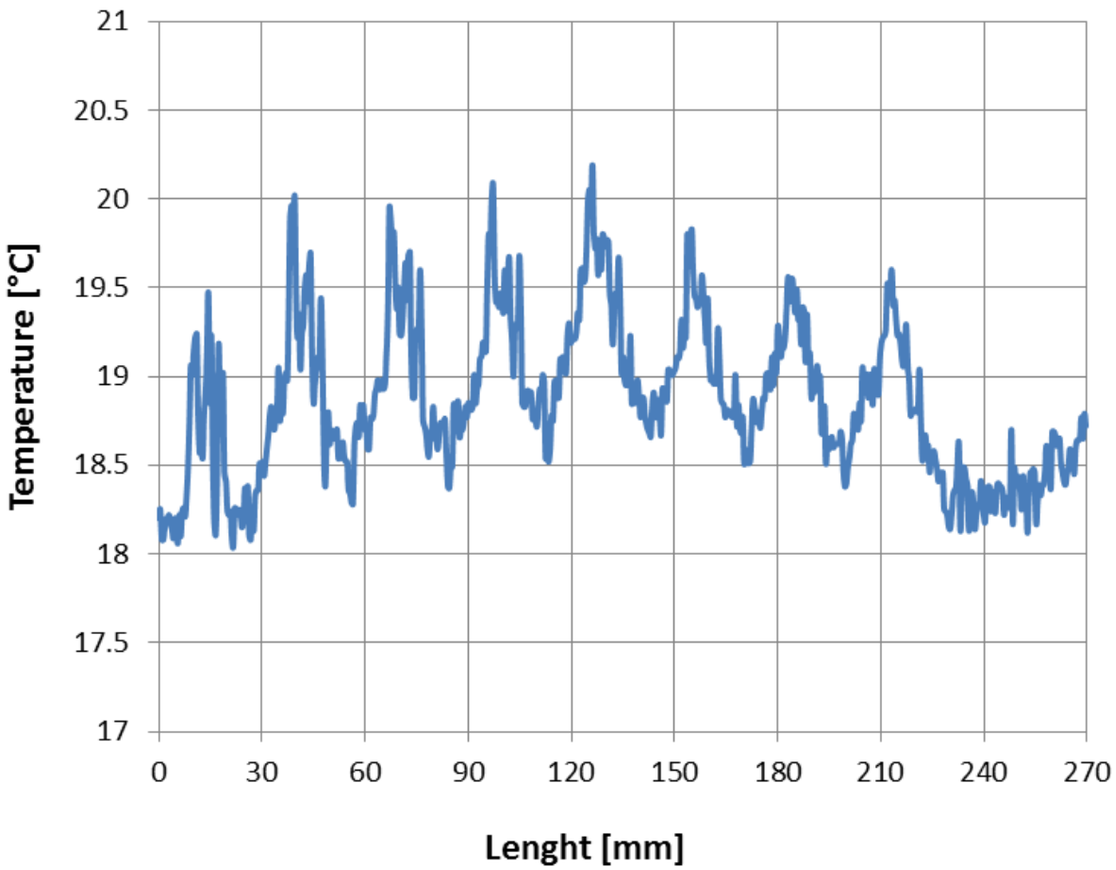
IB Stave — Thermal Characterisation

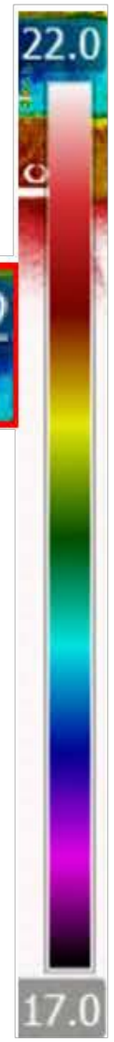
Stave temperature measurements while powering on stave in two steps

1) Power on (with CLK): ~ 80 mW digital + 20 mW analogue / chip
2) Configuration of DTU: ~ 160 mW digital + 20 mW analogue / chip







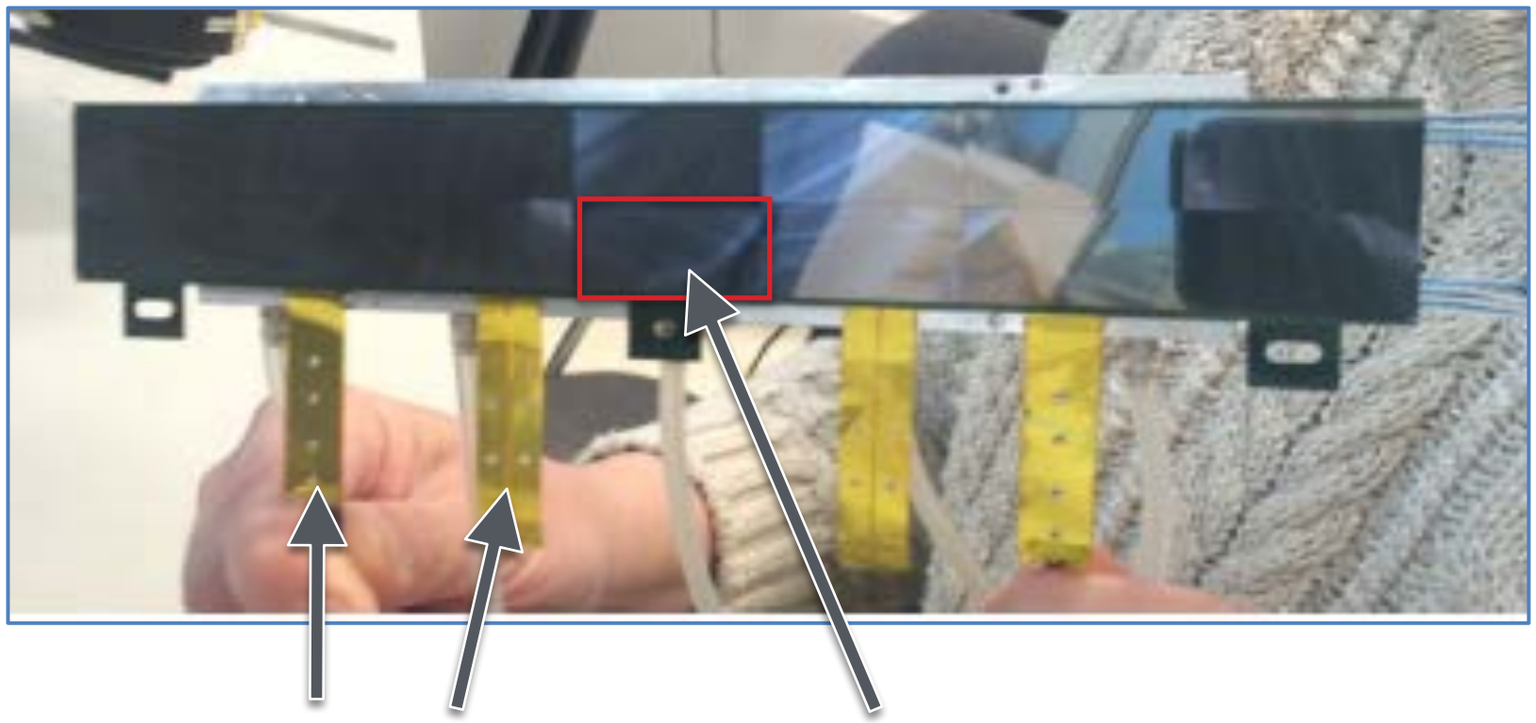


OB HIC Prototypes

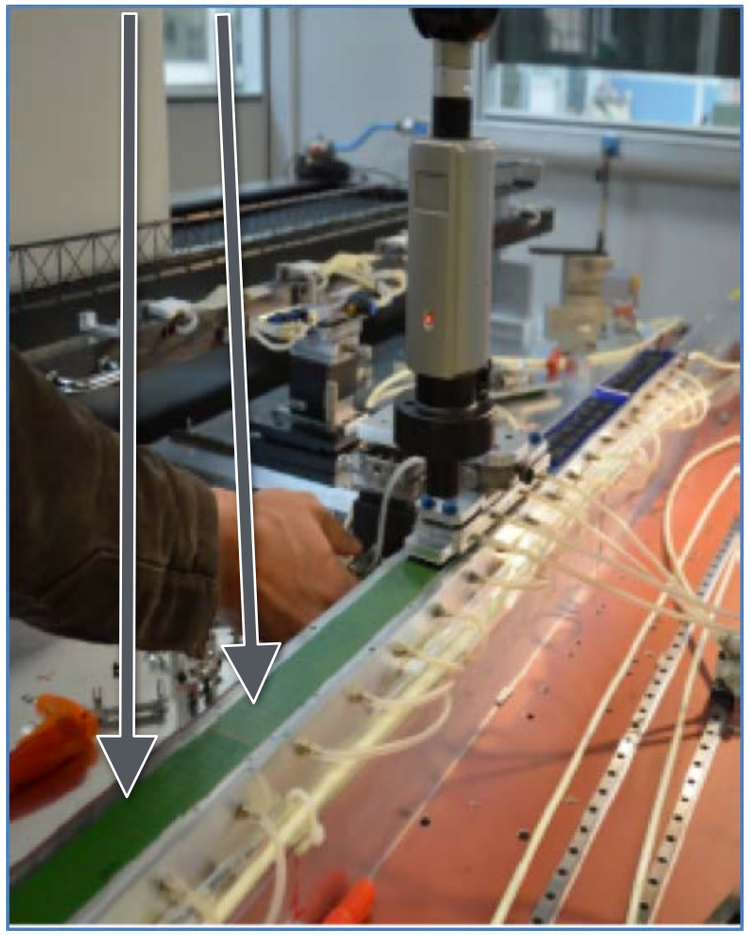
Small series of OB HIC prototypes built using pALPIDE-3 chips

- 6 HICs and 1 stave (with 2 modules)
- Full characterisation with different modes of operation, readout rates and environmental conditions (supply voltages and temperature)
- Sensor performance comparable to single chip

OB Module

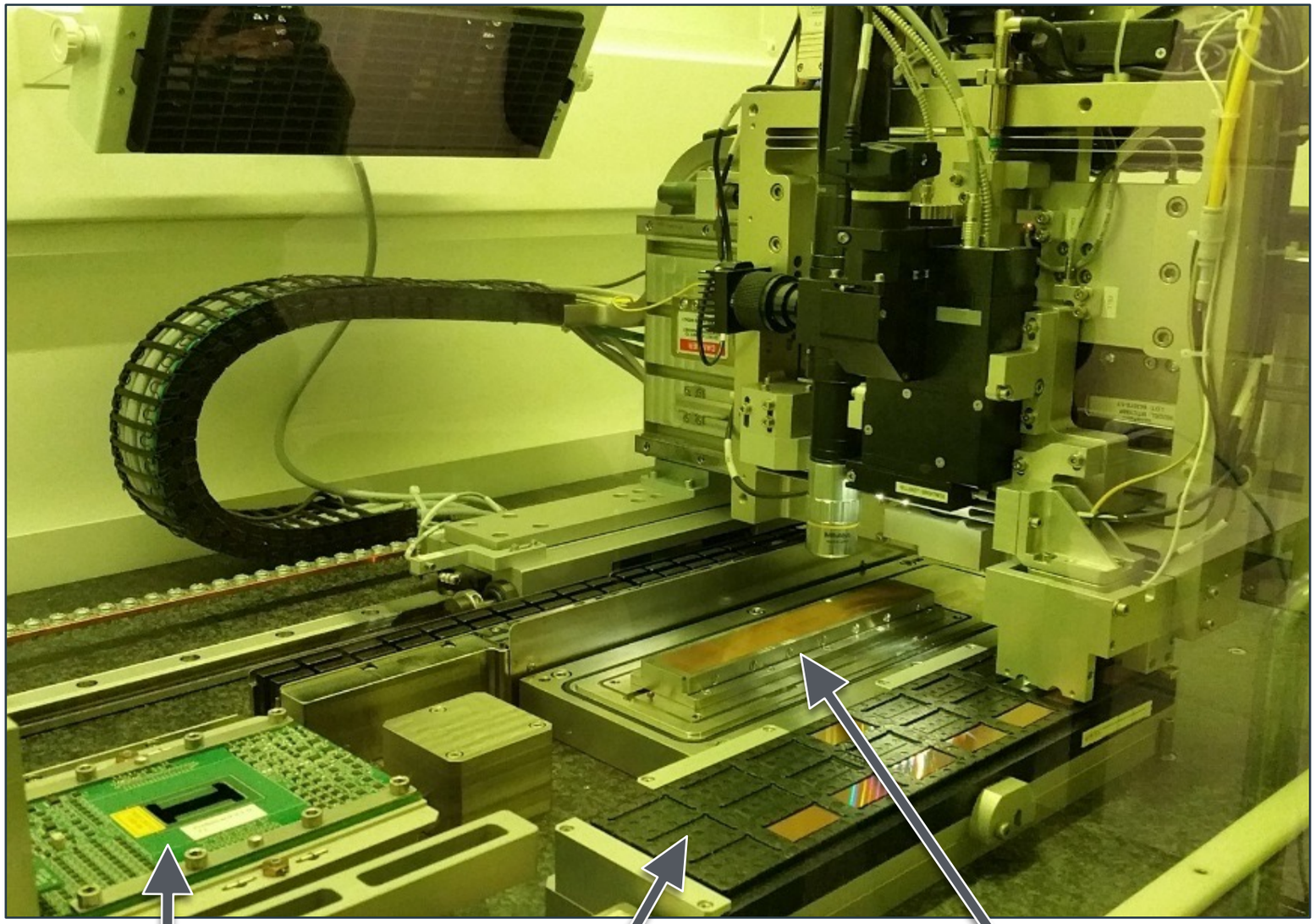


modules

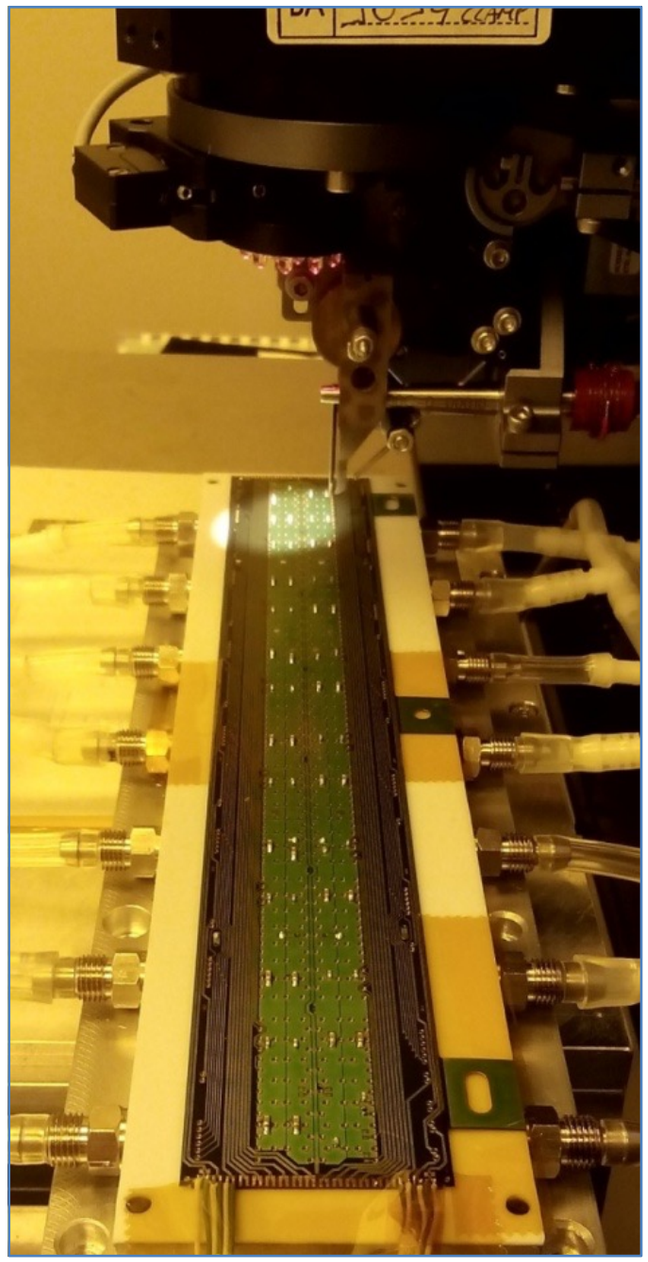


Module Assembly Machine

Automated module assembly (custom-made machine)



Electrical interconnection (wire bonding)



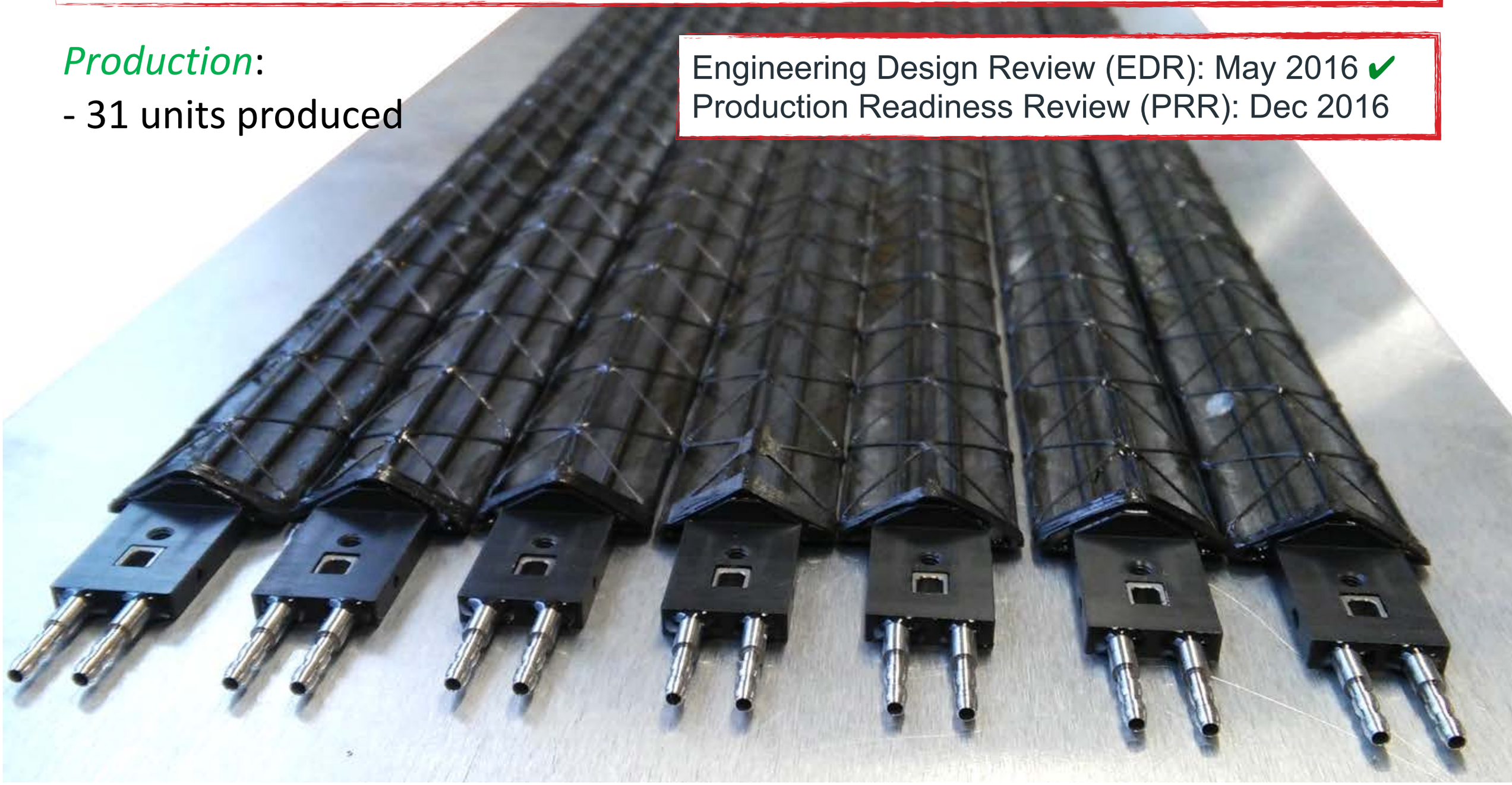
IB Stave Production

Materials, manufacturing process, tooling and thermo-mechanical performance fully qualified

Production:

- 31 units produced

Engineering Design Review (EDR): May 2016 ✔
Production Readiness Review (PRR): Dec 2016



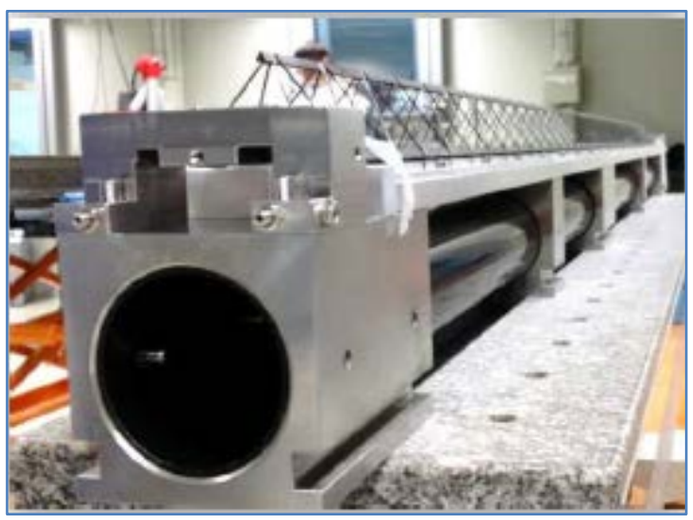
OB Spaceframe & Coldplate Production

Materials, manufacturing process, tooling and thermo-mechanical performance fully qualified

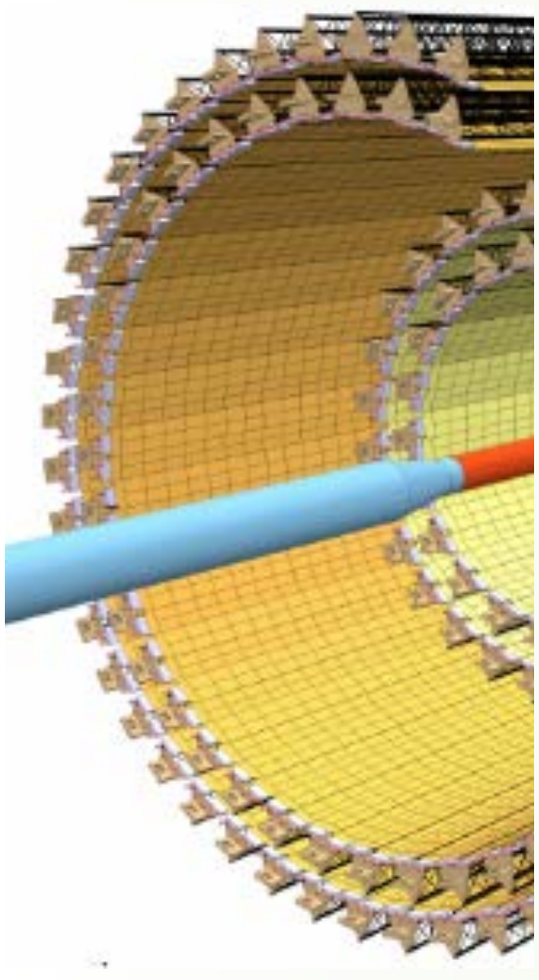
Production:

Space Frame
- 21 units 1.5m (OL) produced
- 14 units 1.m (ML) produced

Cold Plate
- 23 units 1,5m (OL) produced
- 9 units 1m (ML) produced



Readout Electronics — Global Architecture



~ 1 Mrad
~ 10^{13} 1 MeV n_{eq} / cm^2

Central Trigger Processor (**CTP**)

Cavern

GBT link

< 10 krad
< 10^{12} 1 MeV n_{eq} / cm^2

Copper links

Copper links

Copper links

Readout Units

GBT links

GBT links

GBT links

no radiation

Detector Control System (DCS)

First Level Processor (FLP)

PCIe

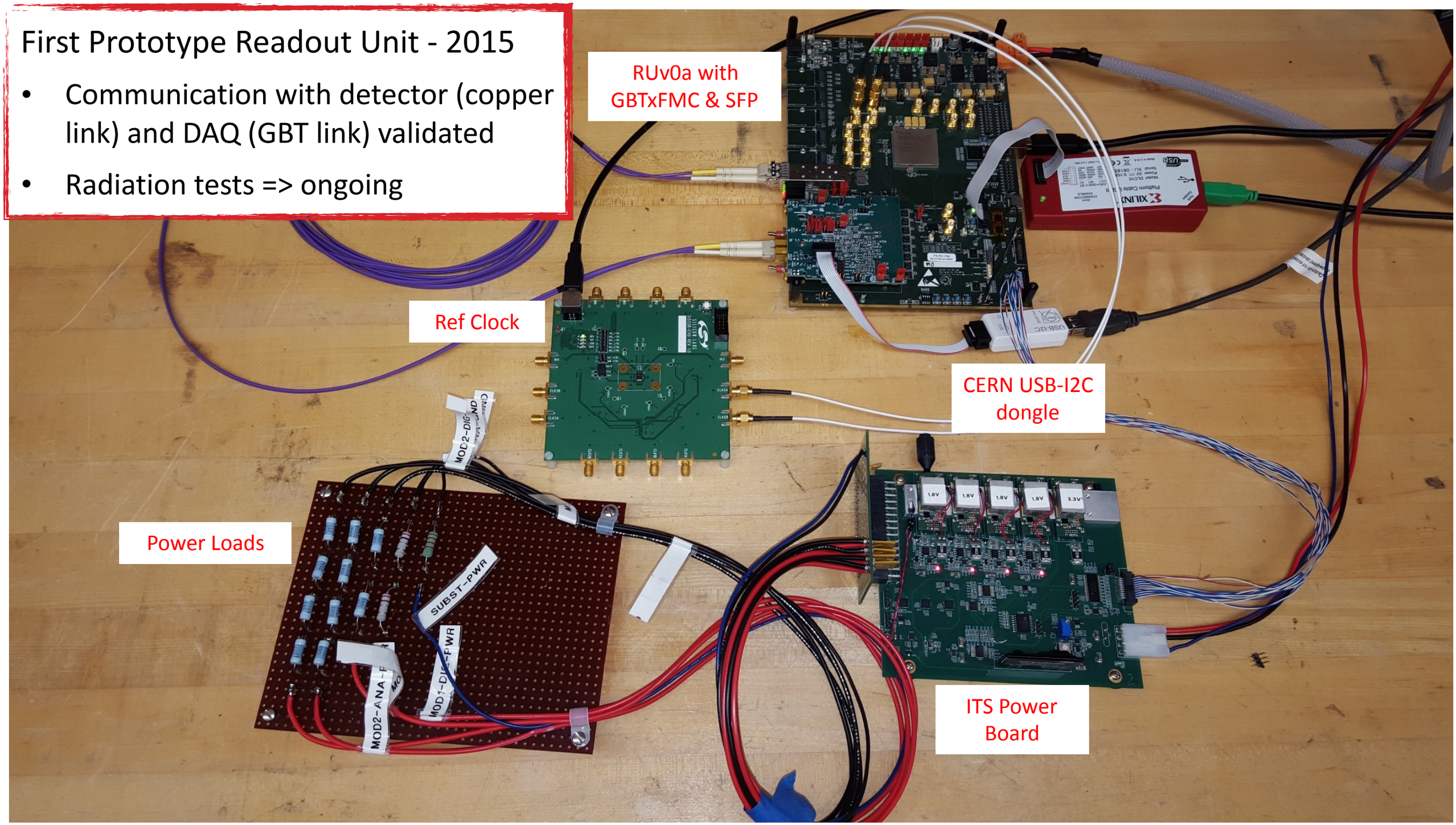
Common Readout Unit (CRU)

Counting Room

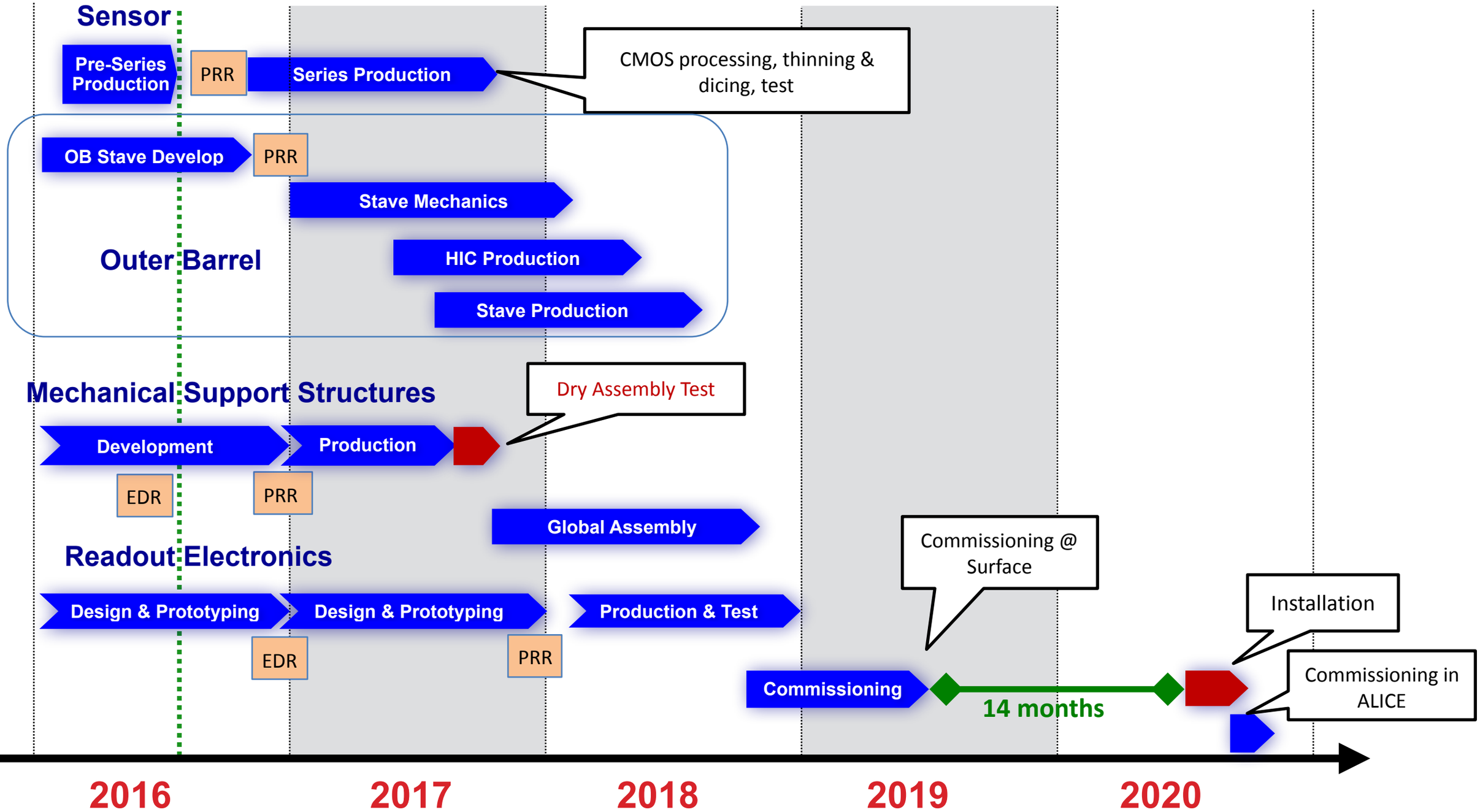
Readout Unit — Prototype

First Prototype Readout Unit - 2015

- Communication with detector (copper link) and DAQ (GBT link) validated
- Radiation tests => ongoing

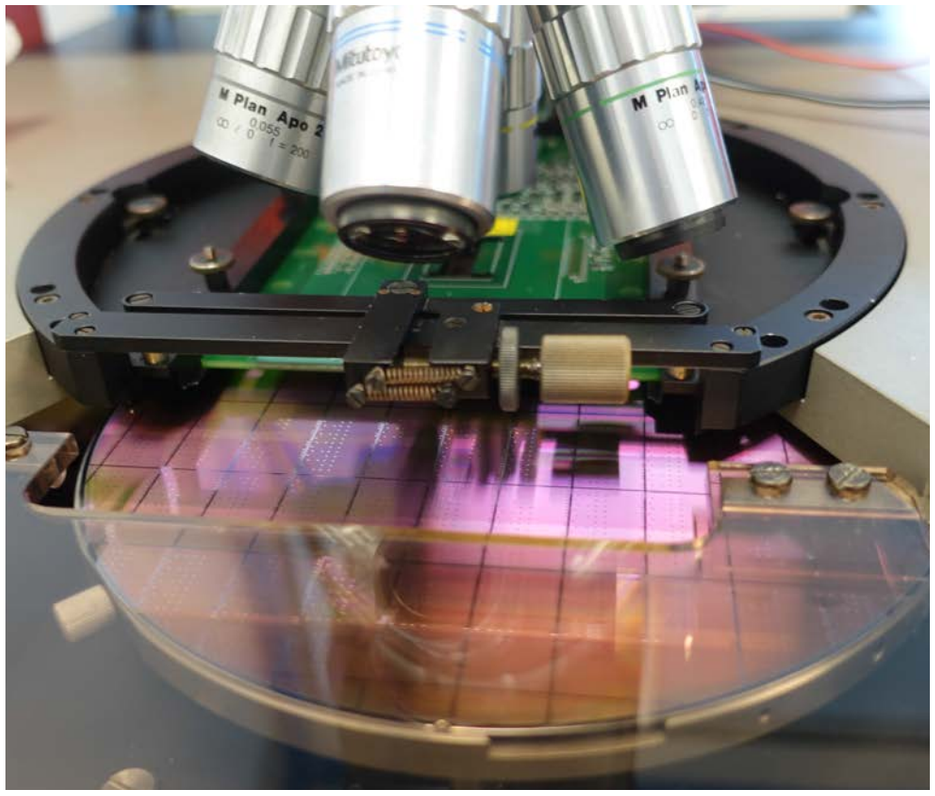


Overall ITS Upgrade Schedule



Summary and Outlook

- Pixel chip prototypes qualified and shown to satisfy the requirements
- First IB staves and OB modules built
  - no showstoppers found
  - some design optimisation ongoing
  - pre-production with the final chip starting soon
- Mechanics design and prototyping well on track
- Global readout architecture determined
- Wafers of final pixel-chip ‘ALPIDE’ delivered, currently being tested



ALPIDE wafter during probe testing

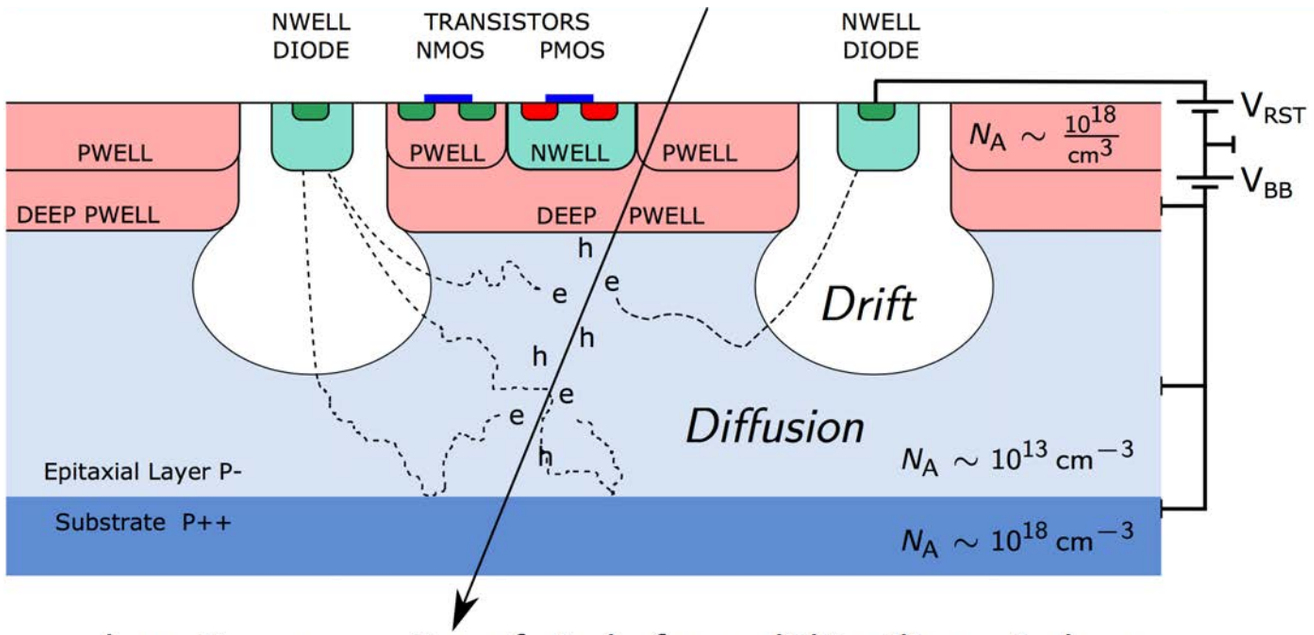
Thank you for your attention!

Spare Slides

ALICE

Pixel Chip

Pixel Chip Technology



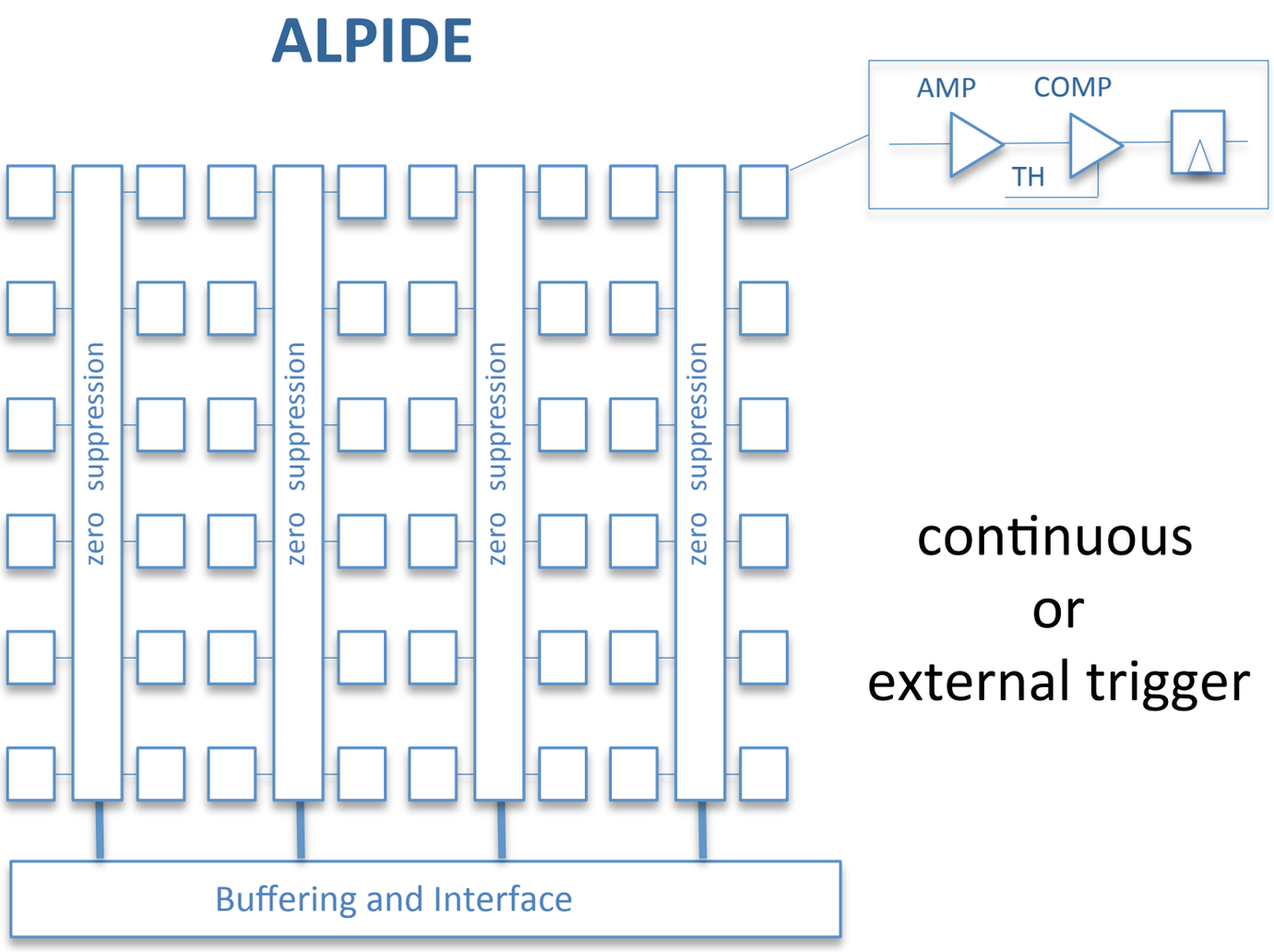
schematic cross section of pixel of monolithic silicon pixel sensor

TowerJazz 180nm CMOS Imaging Process

- 180nm feature size
- 6 metal layers
- 3nm gate oxide
- Deep p-well

- 25µm high-resistivity epitaxial layer (>1kΩcm), not fully depleted:
  - Charge collection: **drift** in depletion zone (white) and **diffusion** (light blue)
  - Charge collection times: **1ns to 100ns**
- Small **n-well diode (2µm to 3µm)**, small compared to pixel ⇒ low capacitance
- Moderate (up to 8 V) **reverse substrate bias V_{BB}** increasing depletion zone around the collection diode
- Deep p-well shields n-well of PMOS transistors to allow for **full CMOS within the active area**

ALPIDE Architecture



continuous
or
external trigger

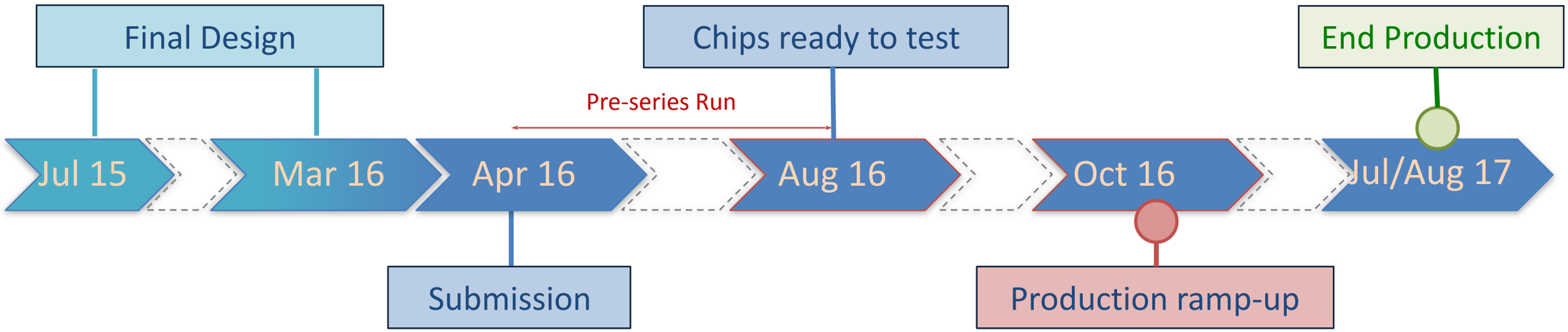
Concept

- In-pixel amplification
- In-pixel discrimination
- In-pixel multi-hit buffer
- In-matrix sparsification using priority encoder

Key features

- Continuously active, ultra low-power front end (40nW/pixel)
- No clock propagation to the matrix
- Only hits propagate to end-of-column logic
- Global shutter
  → continuous or triggered acquisition

Pixel Chip — Status & Plans



Pixel Chip Finalization and Production Timeline

- Engineering Design Review — Oct 15 ✔
- Complete design of final ALPIDE — Mar 16 ✔
- Pre-series Run: Apr – Aug 16 — ongoing
- Production Readiness Review — Sep 16
- Series Production (~25 wafer/week): — Oct 16 – Jul/Aug 17

Pixel Chip — Manufacturing, QA and Test

Selection of industrial suppliers almost completed

Raw Wafers
MEMC (Italy)

~5%

Raw Wafers QA
TMEC (Thailand)

~ 1500 raw wafers
(epi-layer > 1kOhm cm)

CMOS Manufacturing
Tower (Israel)

~8%

Wafer Probe Testing
CERN

~ 1200 CMOS wafers
(25 wafers /week)

Thinning & Dicing
FUREX (South Korea)

~ up to 60,000 pixel chips
(50μm for IB, 100μm for OB)

ATE for chip series test: IBS (Pusan, CERN), C-On (Seoul)
Custom hardware & software (CERN, Yonsei)

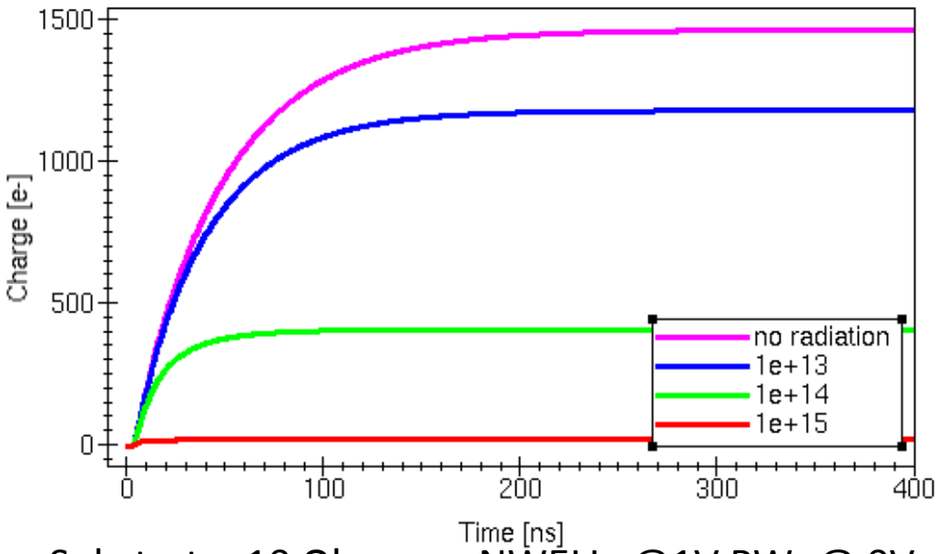
Pick & Place
(on custom trays)
TBD

Pixel Chip Series Test
Yonsei Uni. **Pusan** Uni (South Korea)

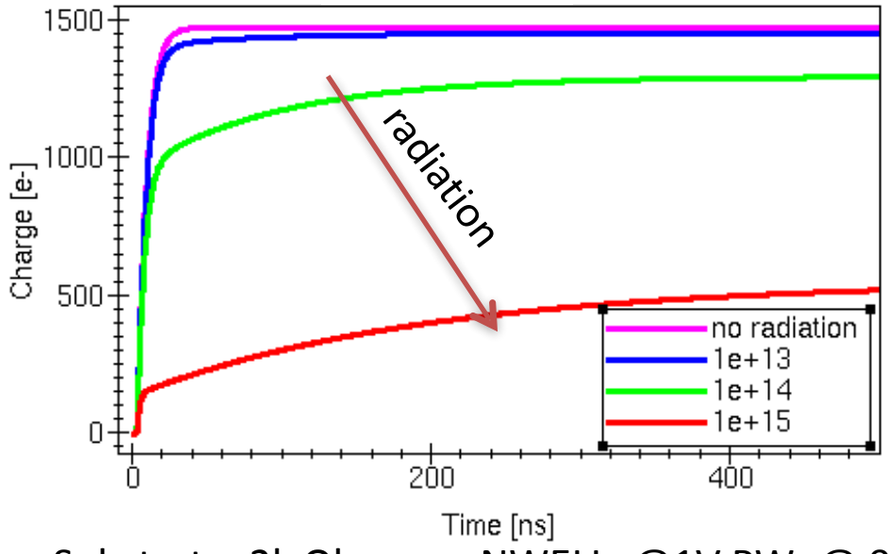
ITS Pixel Chip — Epitaxial Layer

Charge collection time and recombination depend on doping concentration (Si resistivity) and radiation induced dislocations

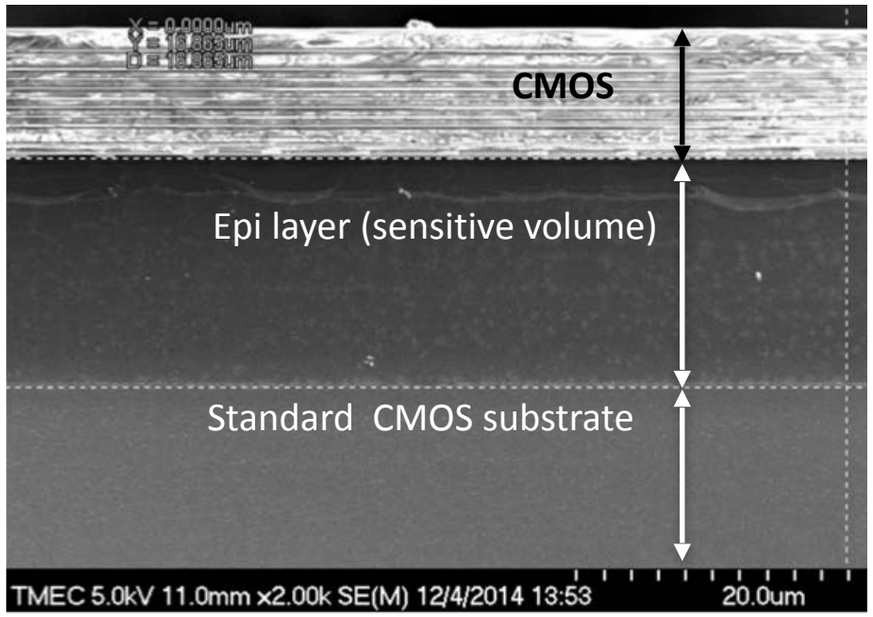
T. Hemperek (Uni Bonn) – CPIX 2014



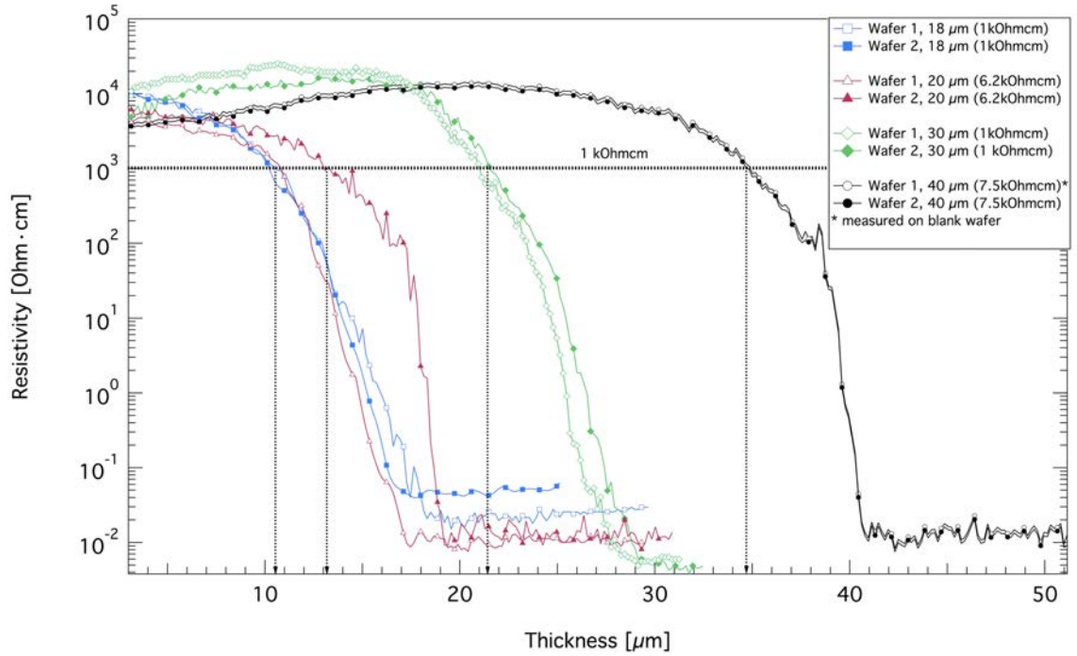
Substrate: 10 Ohm cm, NWELL: @1V PW: @ 0V



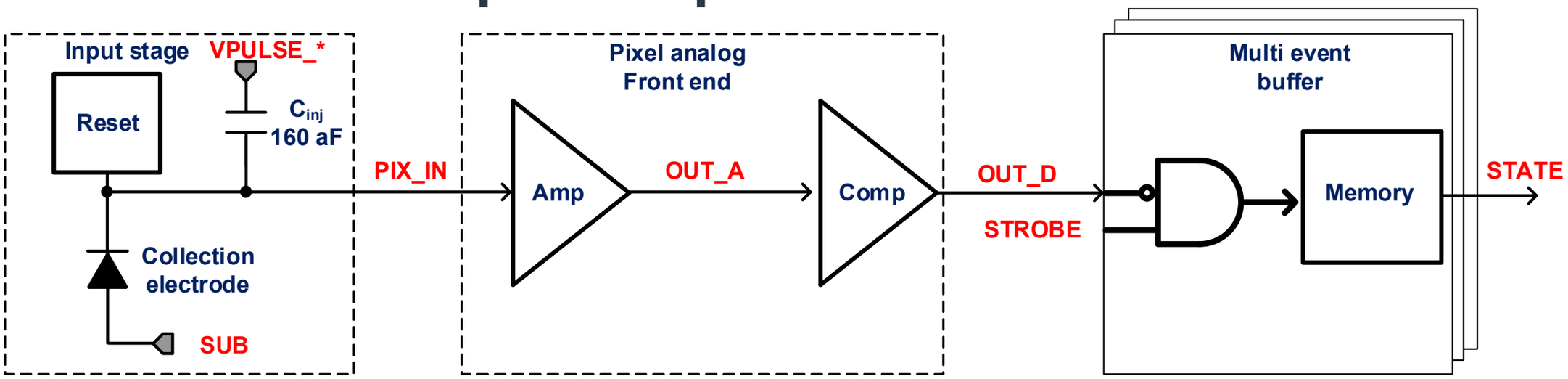
Substrate: 2k Ohm cm, NWELL: @1V PW: @ 0V

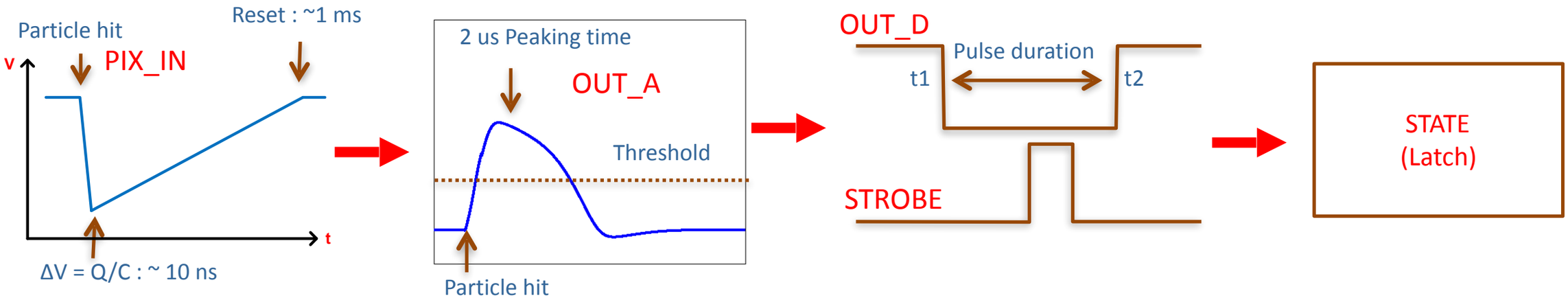


ALICE ITS, SEM picture of prototype chip



ALPIDE — Principle of Operation



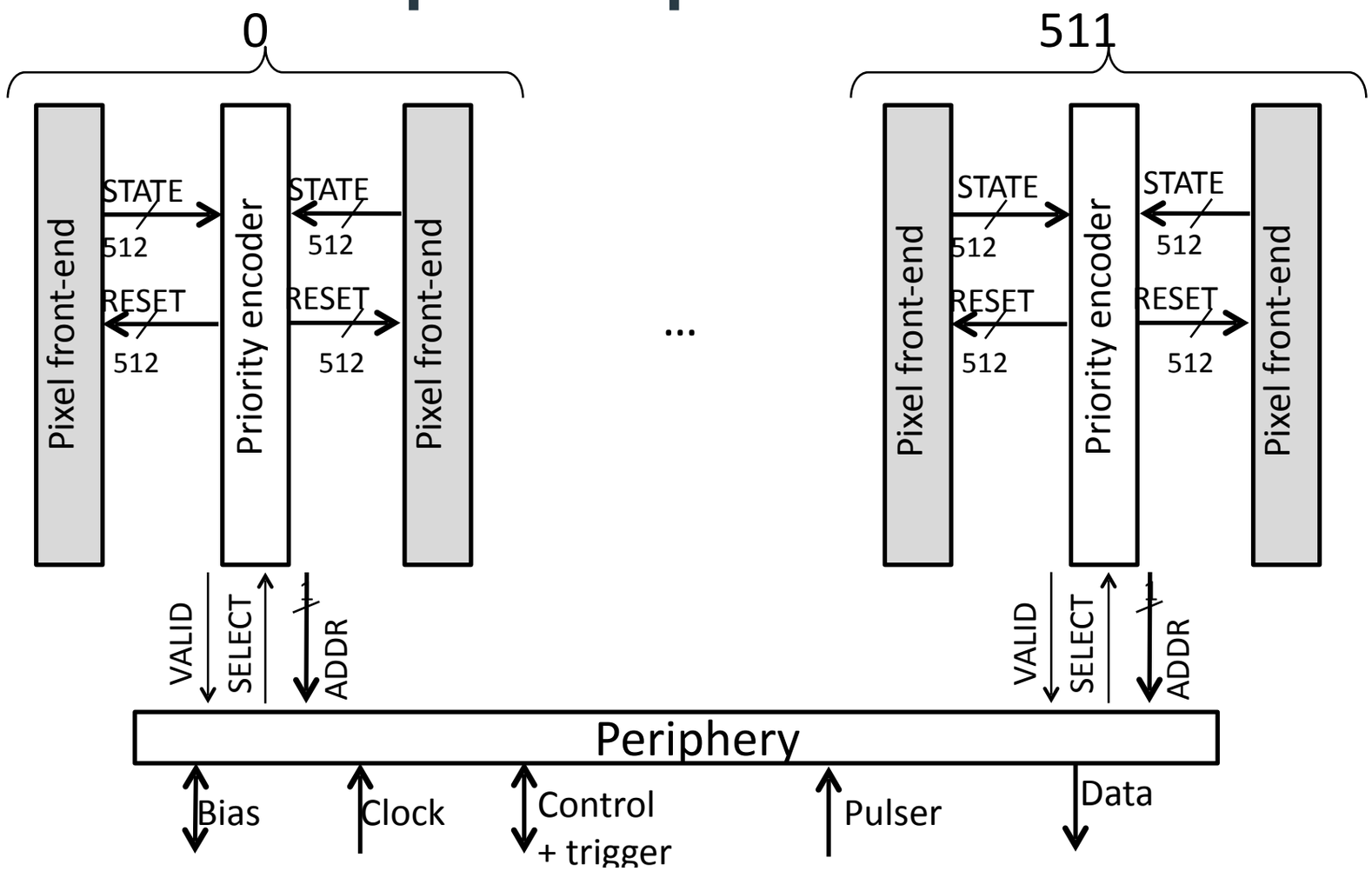


Front-end acts as delay line

ultra low-power front-end circuit
40nW / pixel

- Sensor and front-end continuously active
- Upon particle hit front-end forms a pulse with ~1-2µs peaking time
- Threshold is applied to form binary pulse
- Hit is latched into memory if strobe is applied during binary pulse

ALPIDE — Principle of Operation



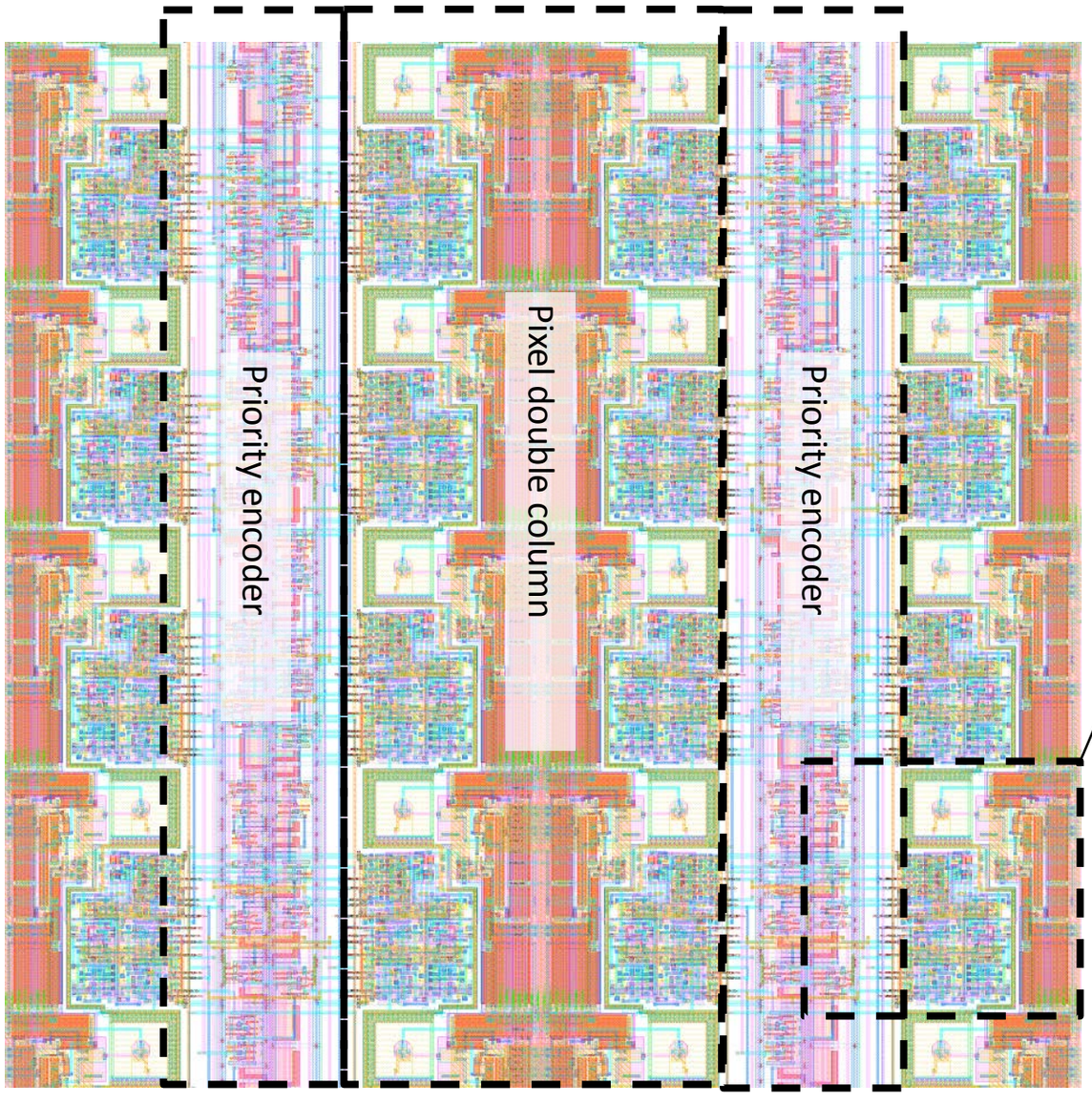
Pixel Matrix - Hit driven architecture

low-power matrix readout ~ 2mW

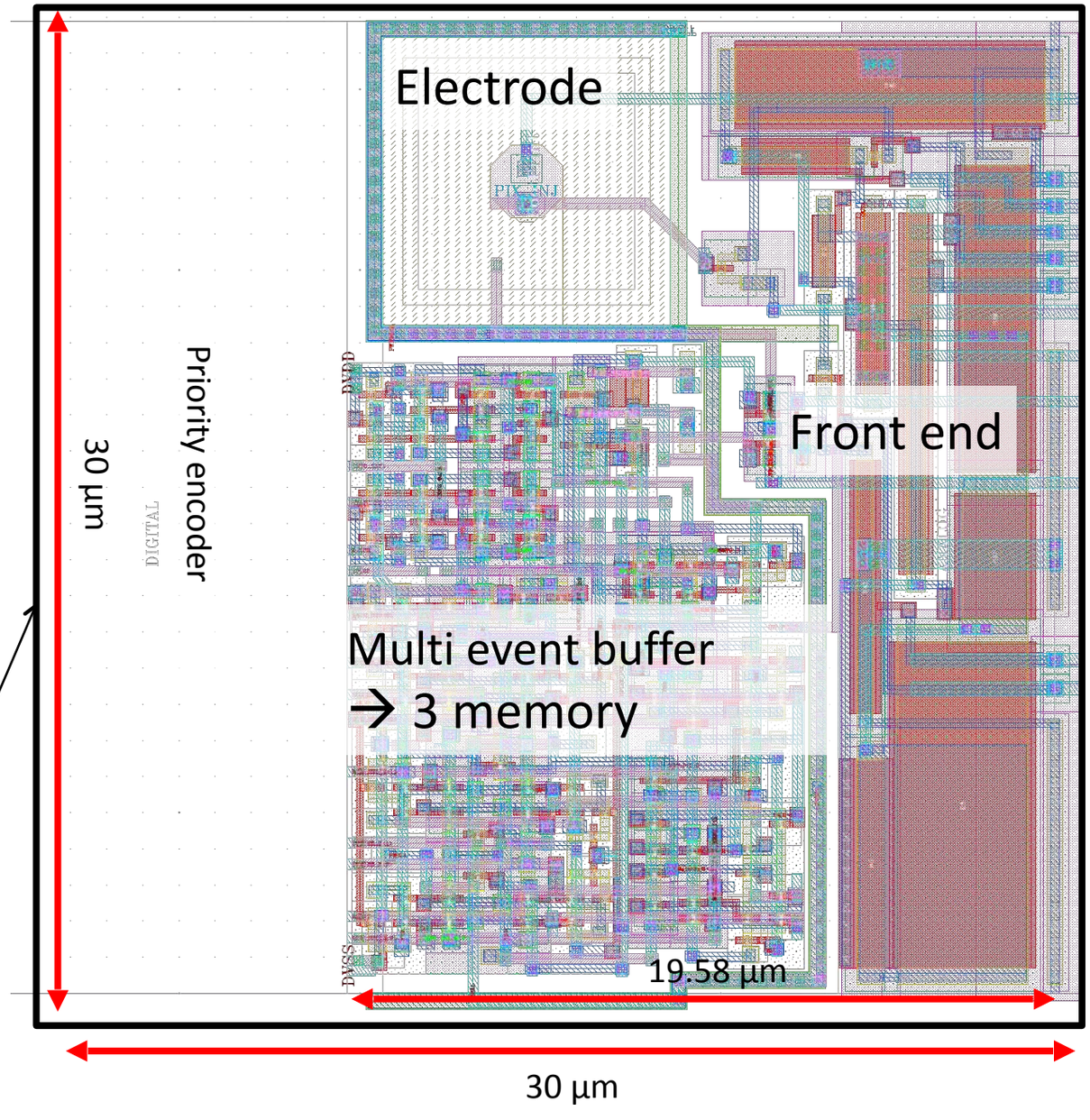
- Priority encoder sequentially provides addresses of all hit pixels present in double column
- No activity if no hit (**no free running clock**) ➔ low power

ALPIDE — matrix and pixel layout

Pixel matrix layout



Pixel layout



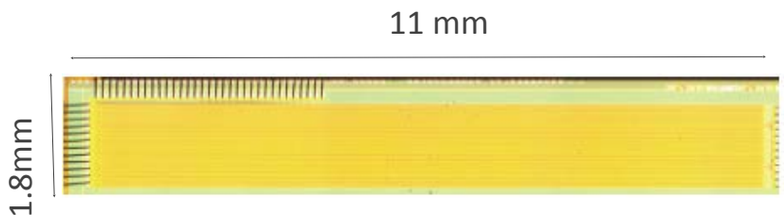
ALPIDE —Development

2012 — **Explorer**

- 20μm x 20μm and 30μm x 30μm pixels (analogue readout)
- pixel geometry, starting material, sensitivity to radiation

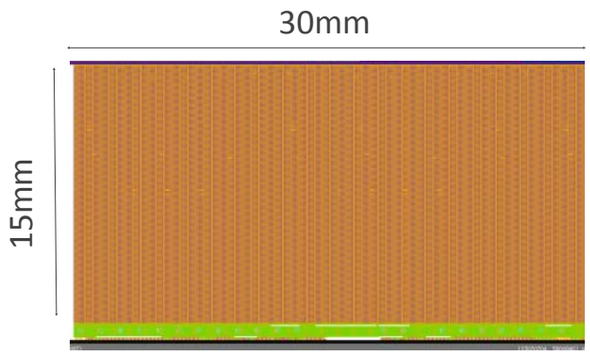
2013 — **pALPIDEss-0**

- Matrix with 64 columns x 512 rows
- 22μm x 22μm pixels
- (in-pixel discrimination and buffering)
- zero suppression within pixel matrix



May-2014 — **pALPIDE-1**

- **Full-scale prototype:** 1024 x 512
- 4 sectors with different pixels
- pixel pitch: 28μm x 28μm
- 1 register/pixel, no final interface



Apr-2015 — **pALPIDE-2**

- Optimization of some circuit blocks
- final interface: allows integration into ITS modules
- NO high-speed output link (1.2 Gbit/sec replaced by a 40Mb/s)

Oct-2015 — pALPIDE-3

- Optimization of some circuits
- all final functionalities

IB Stave & OB Stave — Milestones

- Pre-series production (final components)
  - > 8 IB staves , > 4 OB staves — Sep 16 – Dec 16

  ➔ based on final ALPIDE

- Production Readiness Review — **Dec 16**

- IB Stave Production
  - Space-frame & cold plate — Jan 17 – Sep 17
  - FPC Production — Jan 17 – Sep 17
  - **Stave** — **Apr 17 – Jan 18**

- OB Staves Production
  - Space-frame & cold plate — Jan 17 – Jan 18
  - FPC — Jan 17 – Jan 18
  - **HIC** — **May 17 – Apr 18**
  - **Stave** — **June 17 – July 18**

ALICE

OB Mechanics

OB Stave Mechanics — Production Site and Personnel

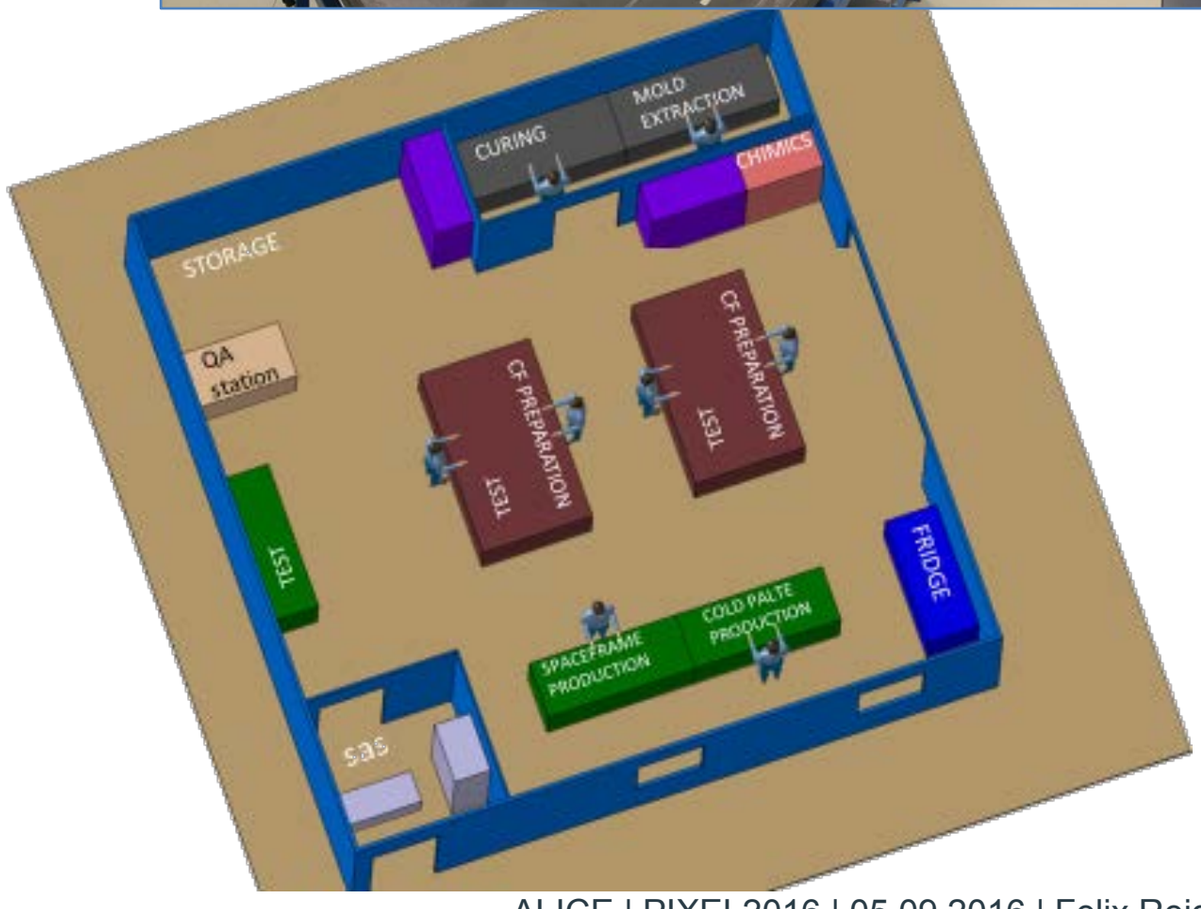
Manufacturing site and personnel

Clean room CERN-Meyrin Bld 167
90m^2 clean environment,
22±2°C, 50% humidity

Personnel
3 FTE production
2 FTE test and QA

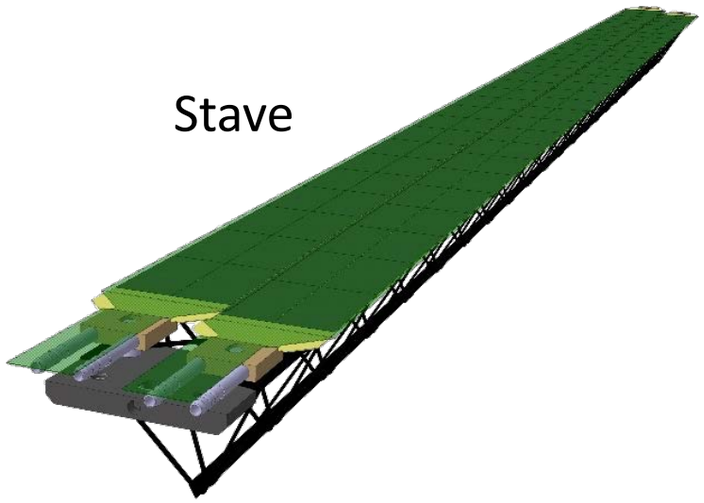
EDR May 2016
PRR Dec 2016

Production start Jan 2017
Production end Sept 2017



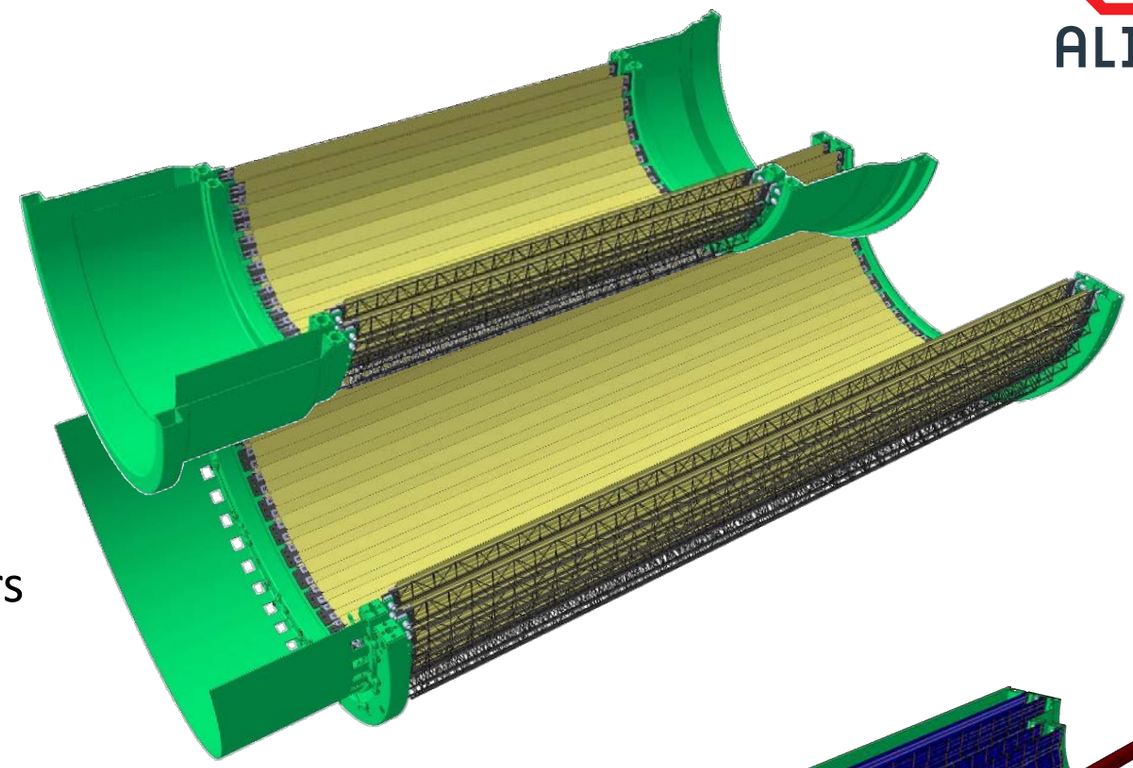
OB Mechanics

Stave



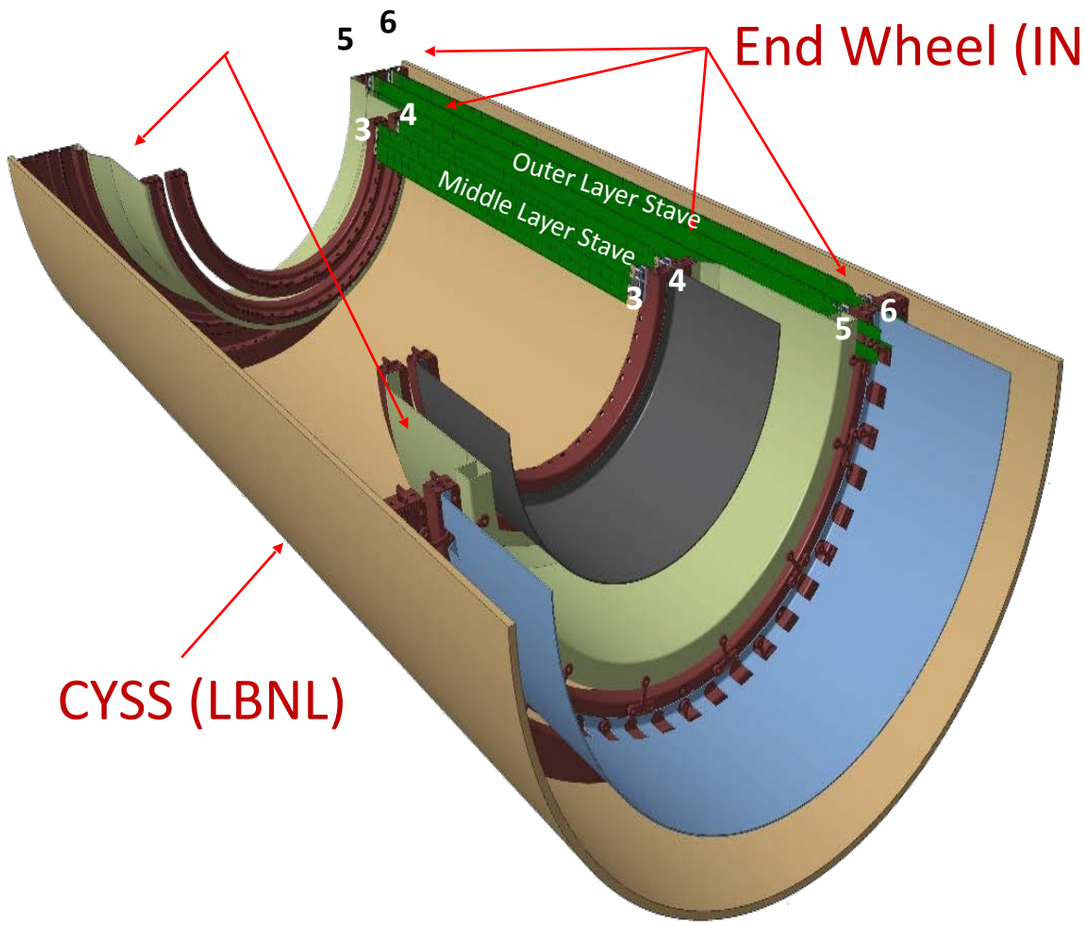
2 Middle Layers

2 Outer Layers



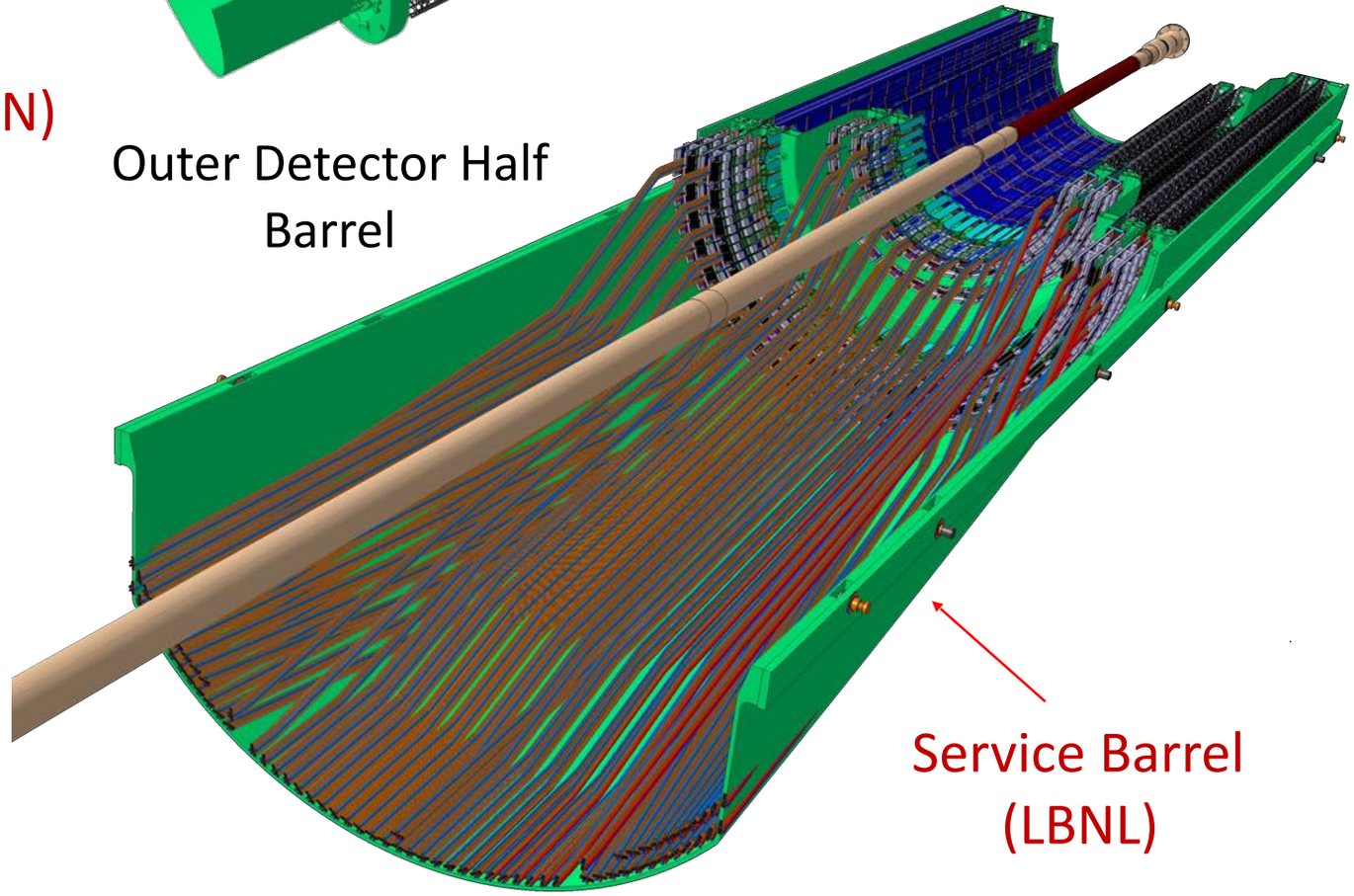
COSS (INFN)

End Wheel (INFN)



CYSS (LBNL)

Outer Detector Half Barrel



Service Barrel (LBNL)

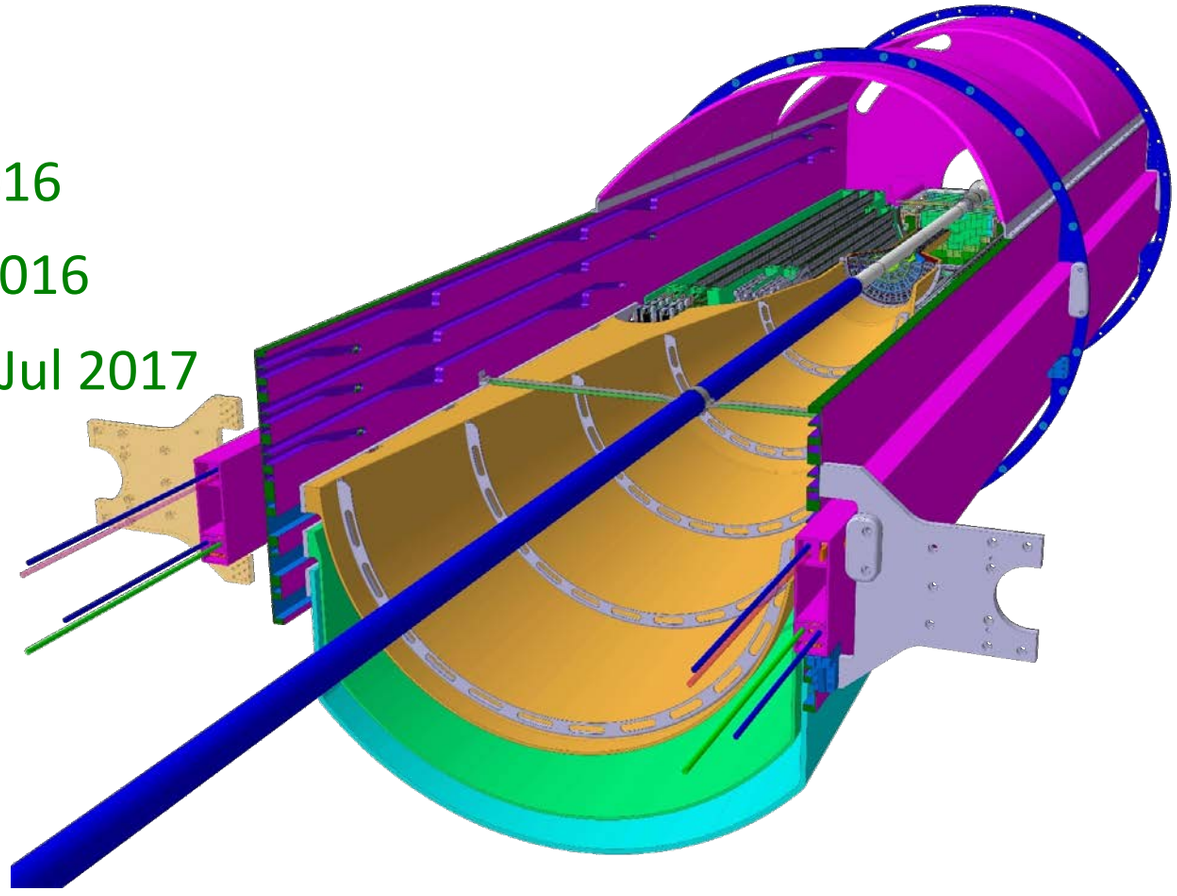
OB Mechanics — Milestones

Detector Barrel Mechanics

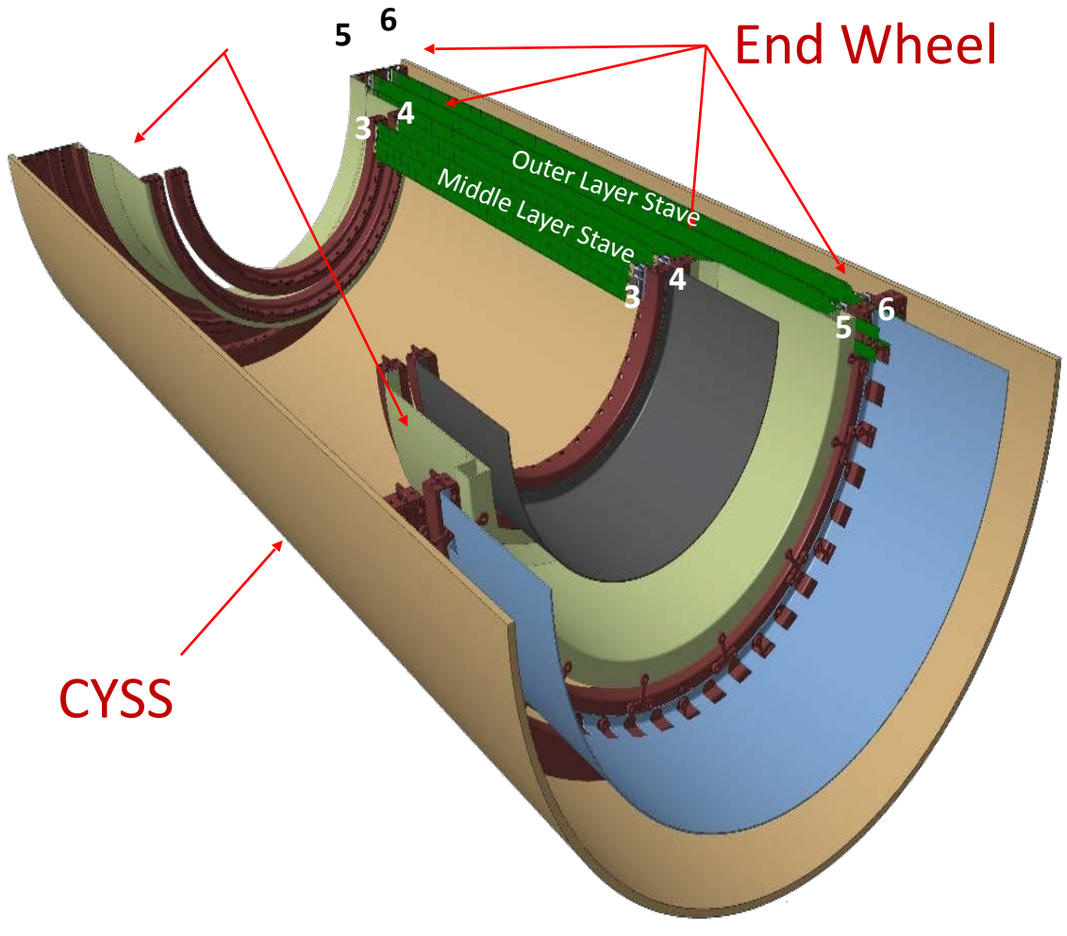
① Engineering Design Review — Jul 2016

② Production Readiness Review — Dec 2016

③ Production — Jan – Jul 2017



COSS



Service Barrel / Cage

① Engineering Design Review Sep 2016

② Production Readiness Review — Feb 2017

③ Production — Mar – Sep 2017

OB Stave Construction Flow

Pixel Chip Series Test

Yonsei Uni, Pusan Uni

FPC Series Test

INFN - Trieste

HIC Assembly and Test

IB: CERN(IB); OB: Bari, Liverpool, Pusan-Inha, Strasbourg, Wuhan

Stave Mechanics

CERN

Power Bus

Kharkov

Stave Assembly and Test

IB: CERN; OB: Daresbury, Frascati, LBNL, NIKHEF, Turin

Outer Barrel Assembly and Commissioning

CERN

ALICE

Readout Electronics

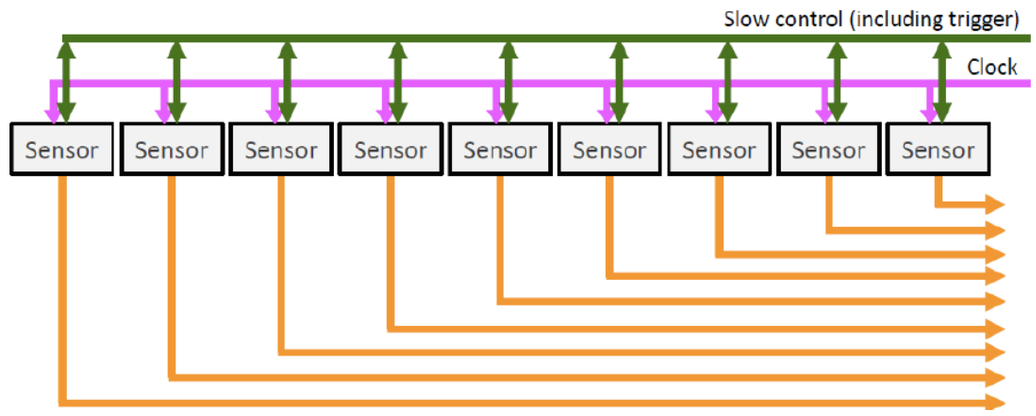
Stave Readout Topology

From the innermost to the outermost layer

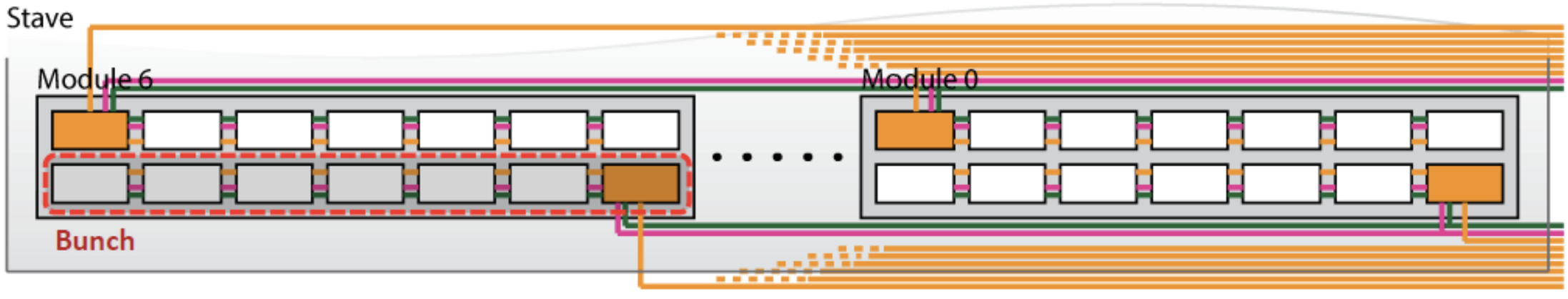
- The expected hit density decreases by a factor of 100
- The number of chips per (half-)stave increases from 9 to 98.

Different readout topologies for inner and outer barrel:

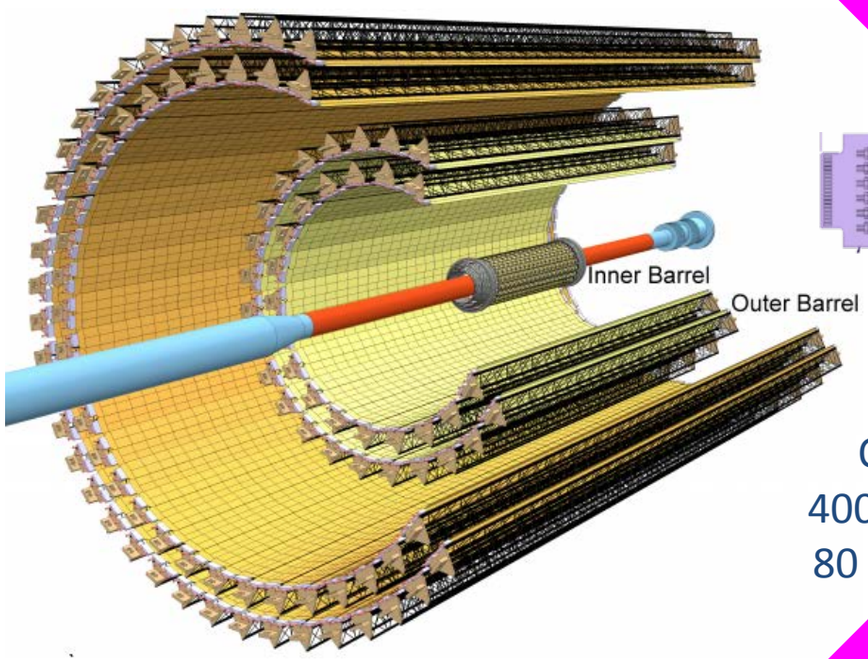
- Inner barrel: each chip drives point-to-point data line to off-detector electronics



- Outer barrel: chips grouped into modules with two master chips; data links from masters to off-detector electronics



Readout Electronics Architecture



Each Readout Unit is connected to one stave, both for in Inner and Outer Barrels

Central Trigger Processor

GBT optical

Trigger

One way, passive optical splitting, no busy back

Inner layer (0,1,2)
1.2 Gb/s high speed data,
80 Mb/s clock and control

Clock

Control

HDR-185770-XX-ECUE
XXXXXX
XXXXX

Data (960 Mb/s max)

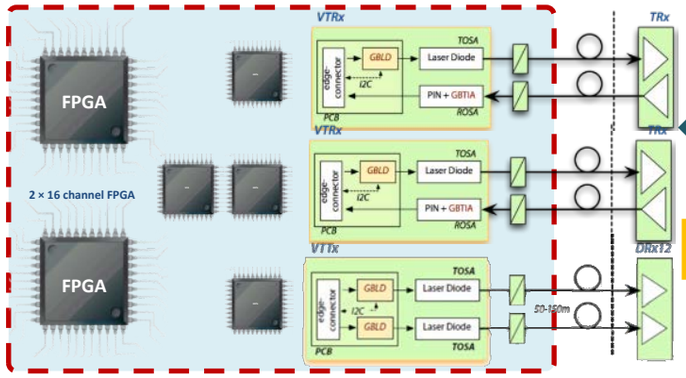
Outer layers (3,4,5,6)
400 Mb/s high speed data,
80 Mb/s clock and control

Clock

Control

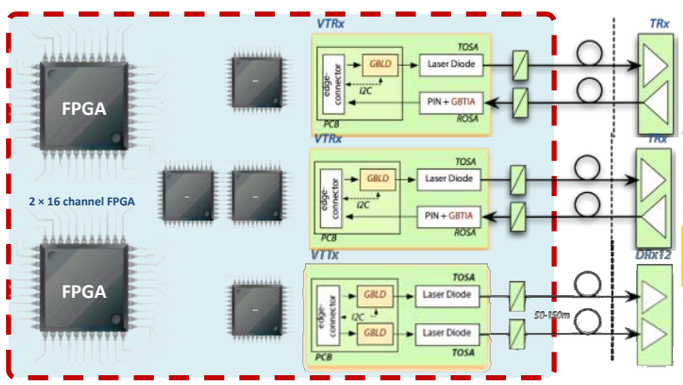
HDR-185770-XX-ECUE
XXXXXX
XXXXX

Data (960 Mb/s max)



× 192

Identical Readout Units (RU) cover the full ITS



GBT optical

Control

Data (9.6 Gb/s max)

GBT optical

Control

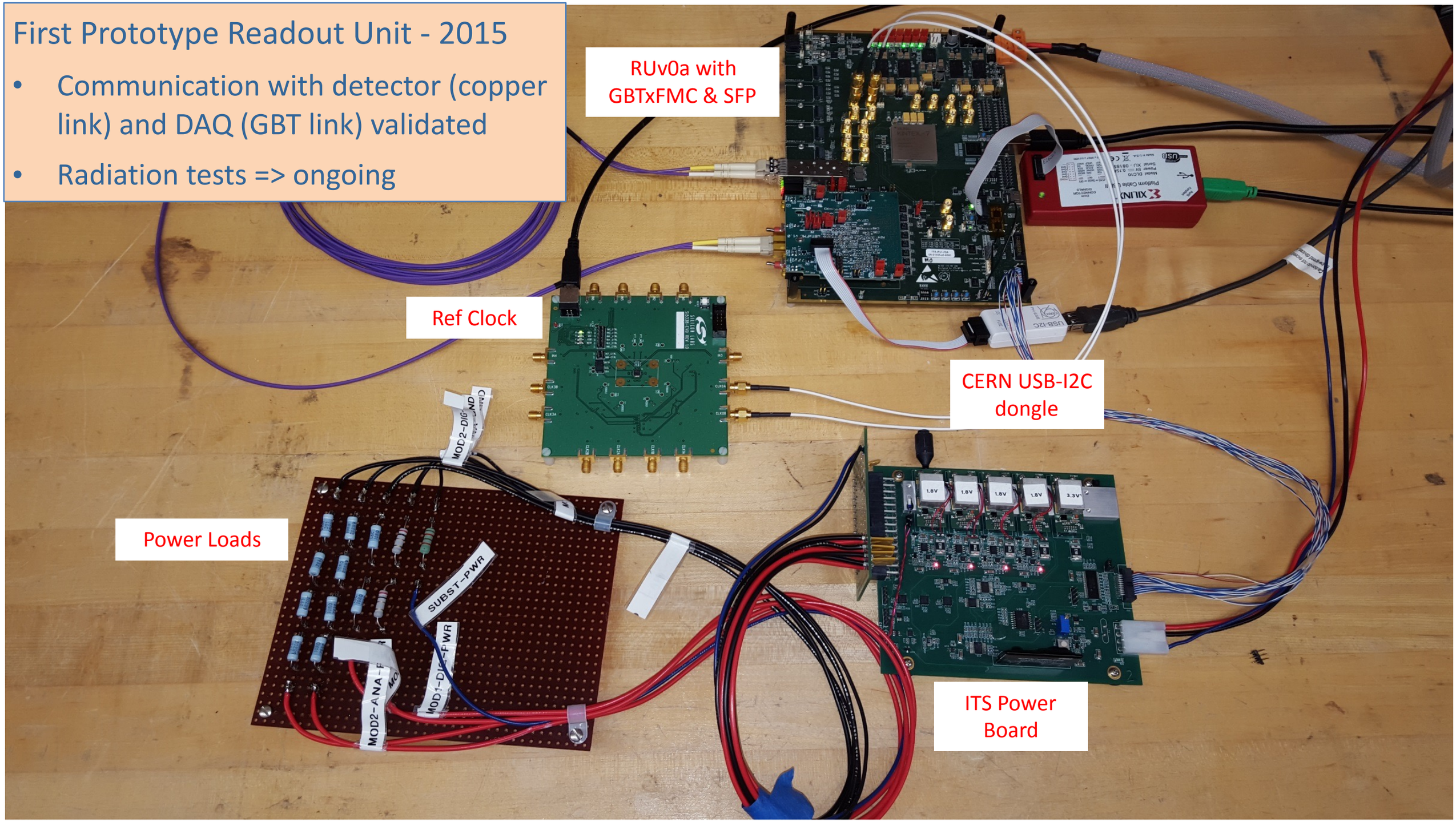
Data (9.6 Gb/s max)

Common Readout Unit & O2

Readout Unit — Prototype

First Prototype Readout Unit - 2015

- Communication with detector (copper link) and DAQ (GBT link) validated
- Radiation tests => ongoing



Readout Electronics — Milestones

- Readout Unit – Prototype I — 2015-2016
  - Selection of technology (radiation tolerance)
  - Validation of full readout chain and components

① Engineering Design Review — **Dec 2016**

- Readout Unit – Prototypes II (& III) — 2016
  - System integration
  - Integration with services (power supplies and crates)

② Production Readiness Review — **Dec 2017**

- Readout Unit – Final Design — Jan – Mar 2018
- Pre-series production — Apr-Jun 2018
- Series Production (220 boards) — Jul – Dec 2018

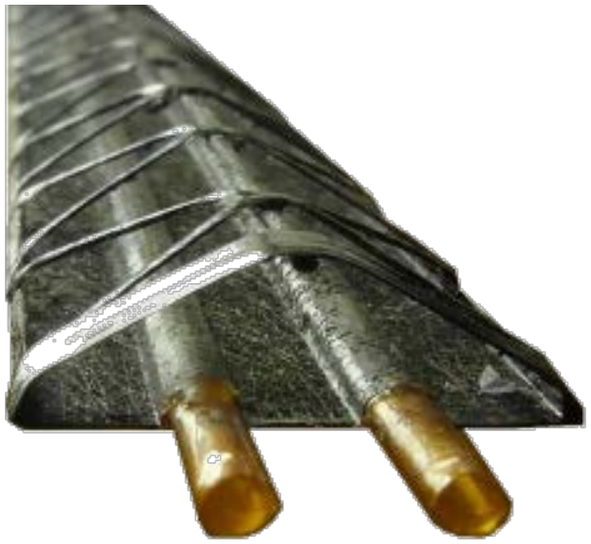
③ Commissioning with detector (on surface) — **Jul 18 – May 19**
  - Full detector + readout electronics + T/DAQ

④ Installation and Commissioning in ALICE — **Jul - Dec 2020**

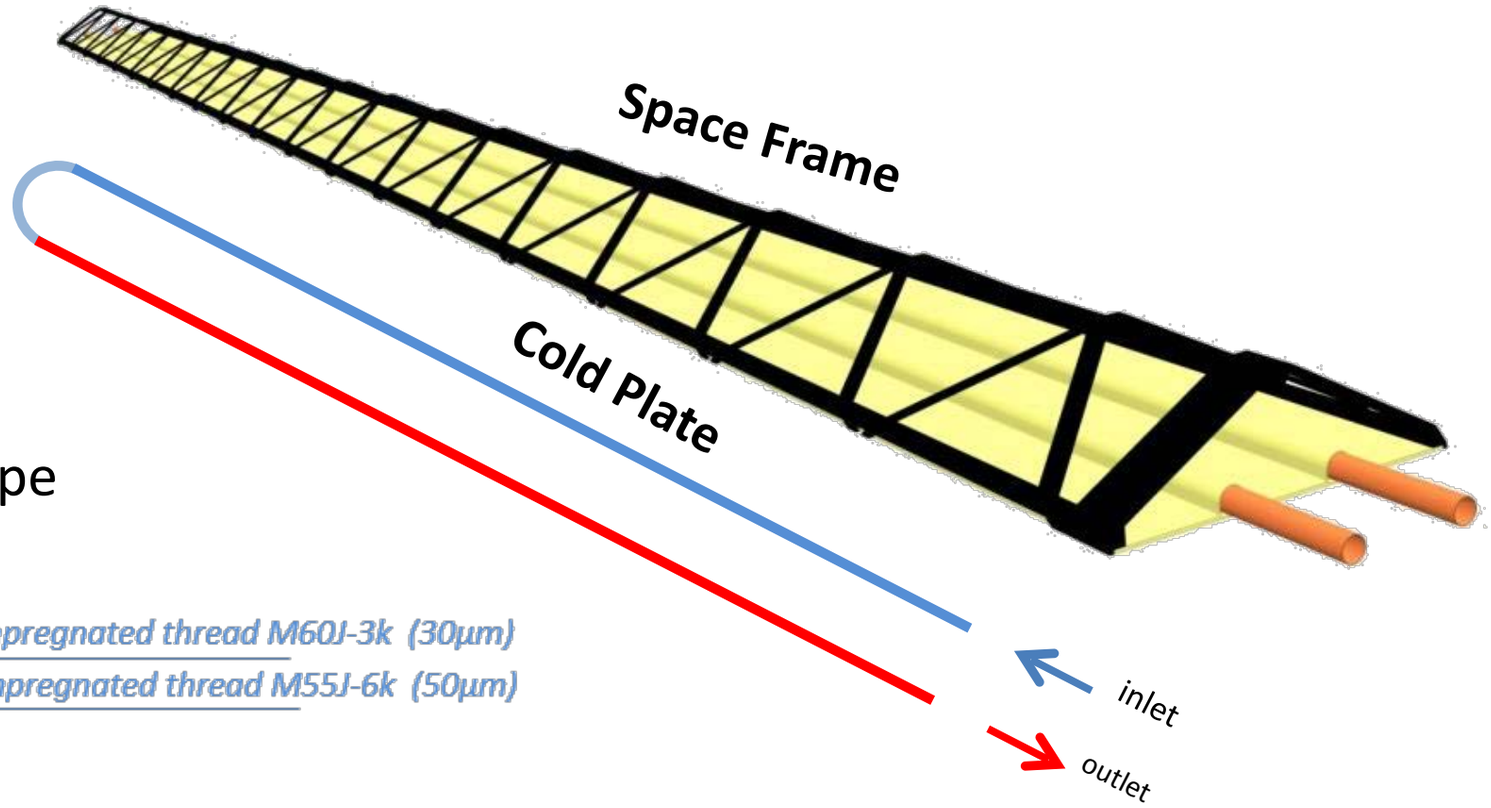
ALICE

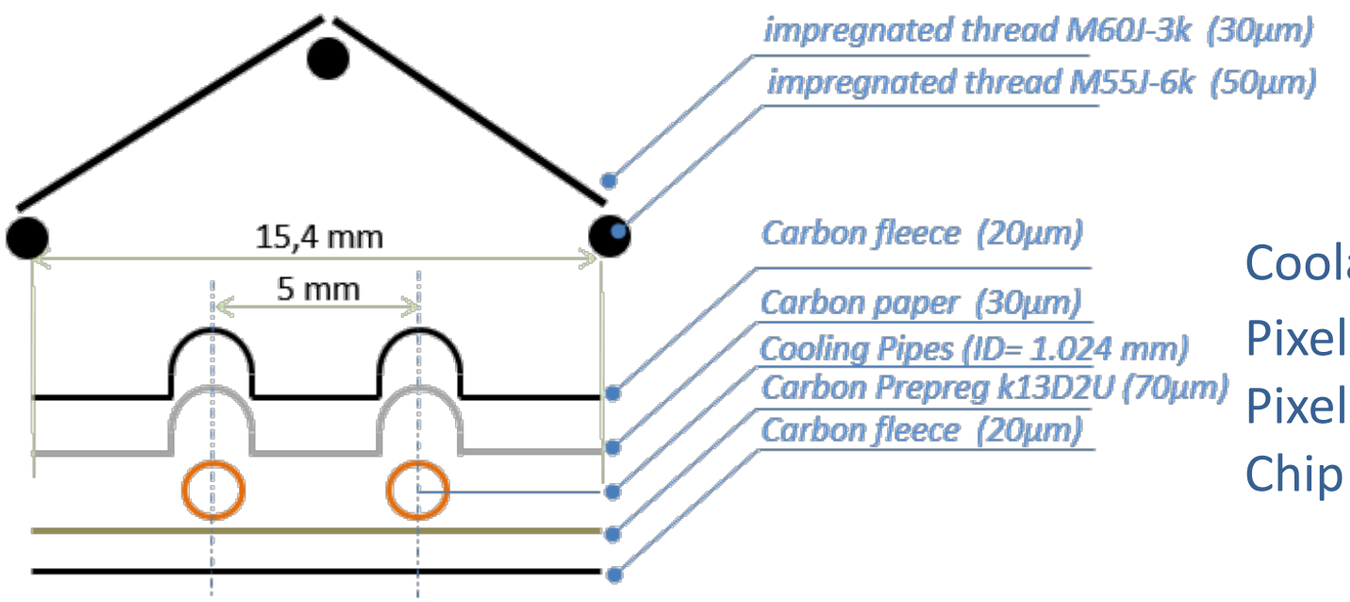
IB Stave

IB Stave — Layout



Prototype





Coolant Single-phase H_2O leak-less

Pixel operational temperature < 30°C

Pixel max temperature non-uniformity < 5°C

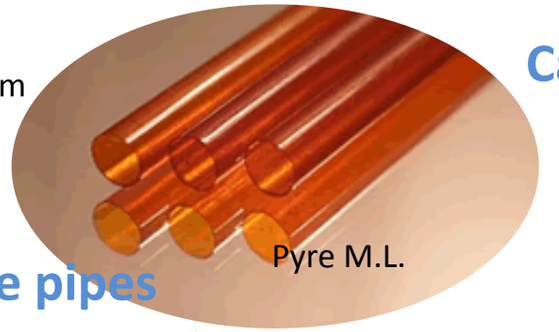
Chip Power dissipation< 100mW/cm^2

Prototype

IB Stave — Materials

- High Thermal Conductive (HTC) material carries the heat to a pipe with coolant
- Pipes are embedded in the HTC material
- HTC= Carbon

D=1.02 mm
wall thick.=24 µm



Polyimide pipes

Carbon peek

Graphite foil

Carbon prepreg

Carbon fleece

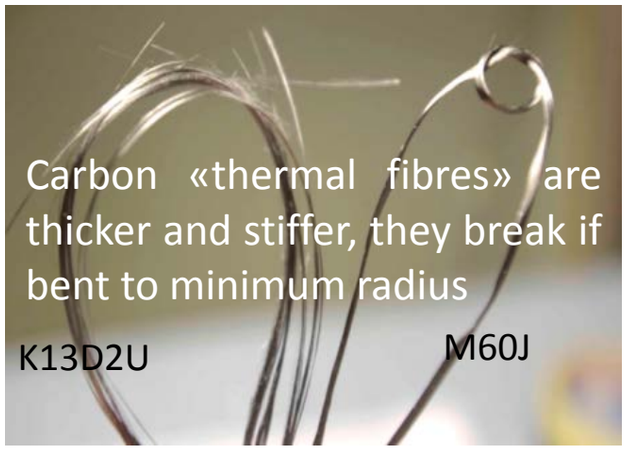
Carbon roving filament wound

IB Stave — Materials

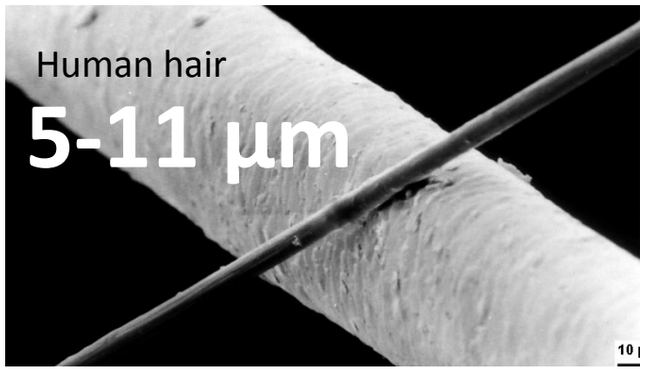
available in different shapes, offer a large range of properties

↑ High stiffness and strenght, fibre E ~ 900GPa, X ~4 GPa
↑ High thermal conductivity, fibre K ~ 1000 W/mK
↑ Minimum thickness, prepreg ~ 45 µm

↓ Limitation on fibres minimum bending radius
↓ Poor mechanical and thermal properties ⊥ fibres



Thermal/ Structural fibres



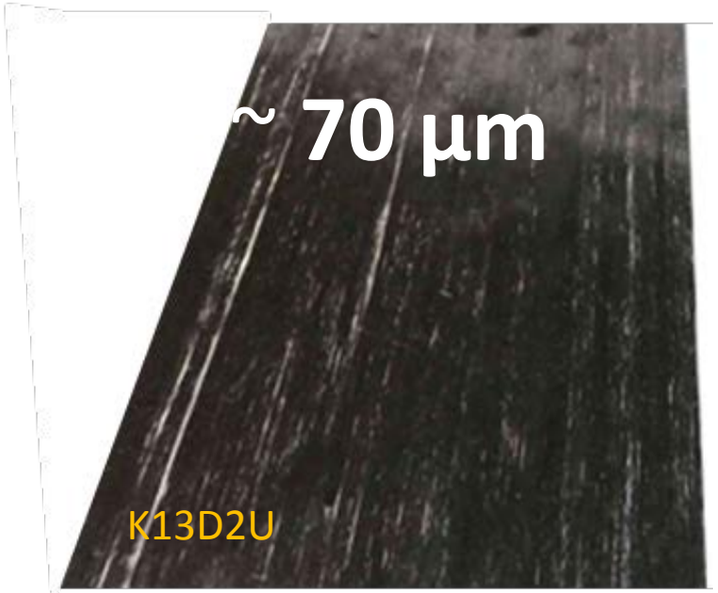
Carbon filament

Cyanate ester resin

Roving

3000 filaments

Fleece

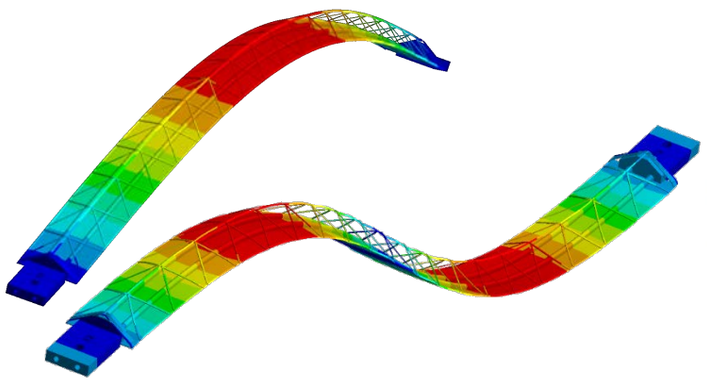


Unidirectional Prepreg

IB Stave — FEA

IB FEA materials

Materials properties and mechanical constraints have been tuned to match the experimental results
Simulation has been used to optimise layout
Stave final characterisation by test



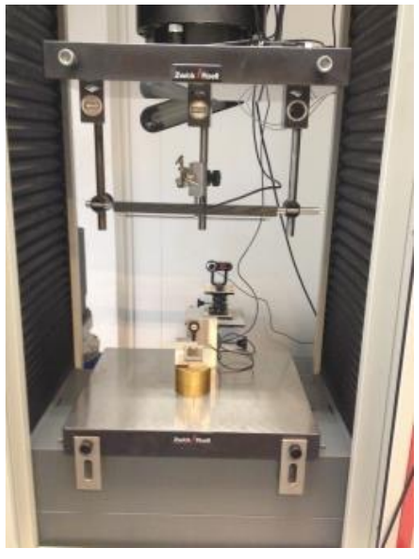
Materials theoretical values

Materials values tuned on test results

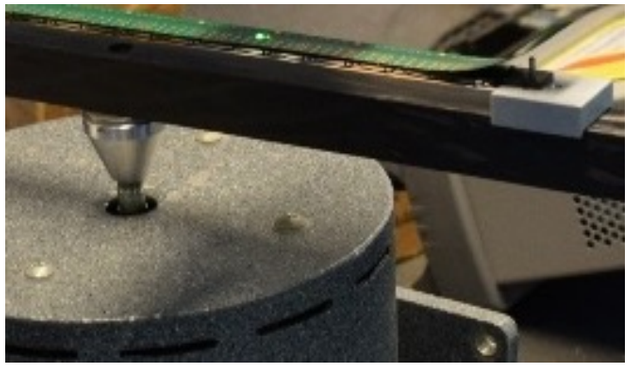
	FAW	fiber/resin [%weight]	Cured thick[µm]	Density [g/ cm3]	Filaments [K=1000]	E1 [GPa]	X_t /X_c [MPa]	E2 [GPa]	Y_t [MPa]	K [W/mK]	CTE [$10^{-6}K^{-1}$]
K13D2U [0]-prepreg		67/33	70	1.86	2K	563	1800/340	6	25	~450	-1,2/ 61
Carbon fleece/Epoxy		30/70	30	0.75(1)	-	134 (70)	150	134(70)	150		
M55J/Epoxy-roving		70/30	-	1.62 (2)	6k	340 (200)	2010/880	6		155	-1.1
M60J/Epoxy- roving		70/30	-	1.62 (2)	3k	365 (200)	2010/785	6		151	-1.1
Carbon paper		-	20	1.6	-	10	-	10		1000/15	
Polyimide tube		-	24	1.42	-	2.5	305	2.5		0.205	40
Carbon peek		-	-	1.41	-	7.7	130	7.7	130	0.92	25

IB Stave — Mechanical Characterisation

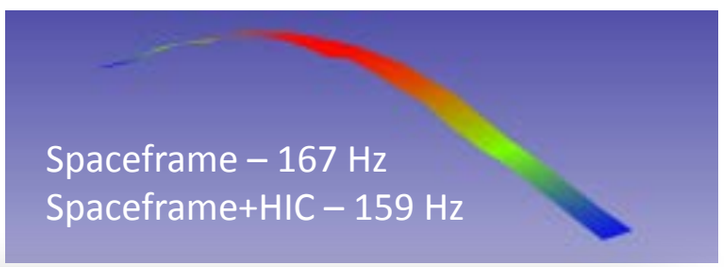
Bending test:
sag 2-9 μm

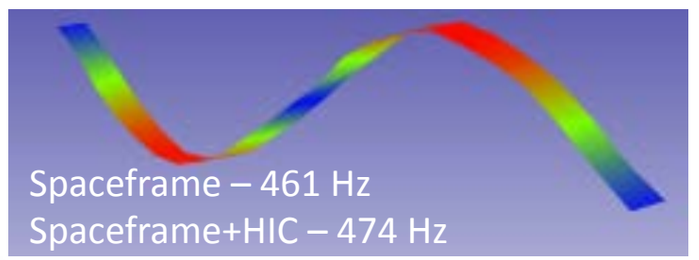


Torsion test:
torsional stiffness: Glp ~0.33 Nm^2



Vibration test:
first natural frequency - 159 Hz
second natural frequency – 461 Hz





Started tests
at wind gallery

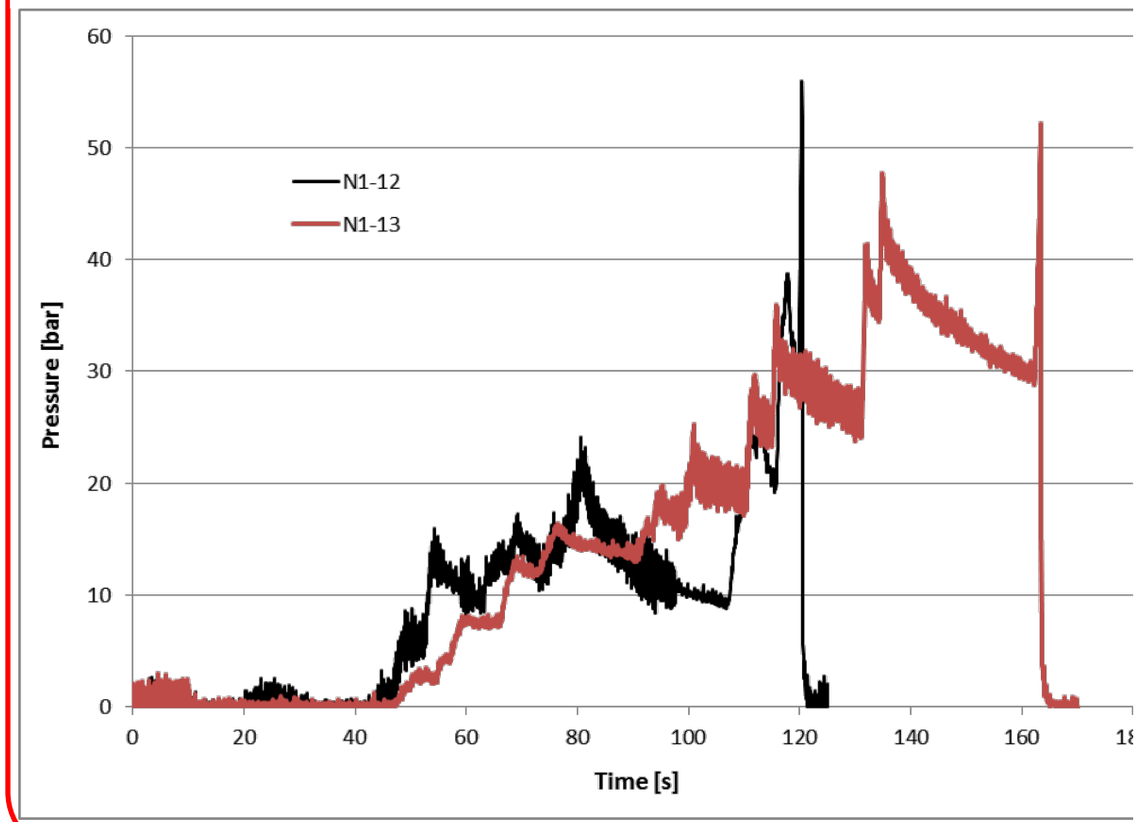
vibration < 3.6 micron for 3.2m/sec speed (foreseen airflow <1m/sec)

IB Stave — cooling lines test

- **Burst pressure** IB

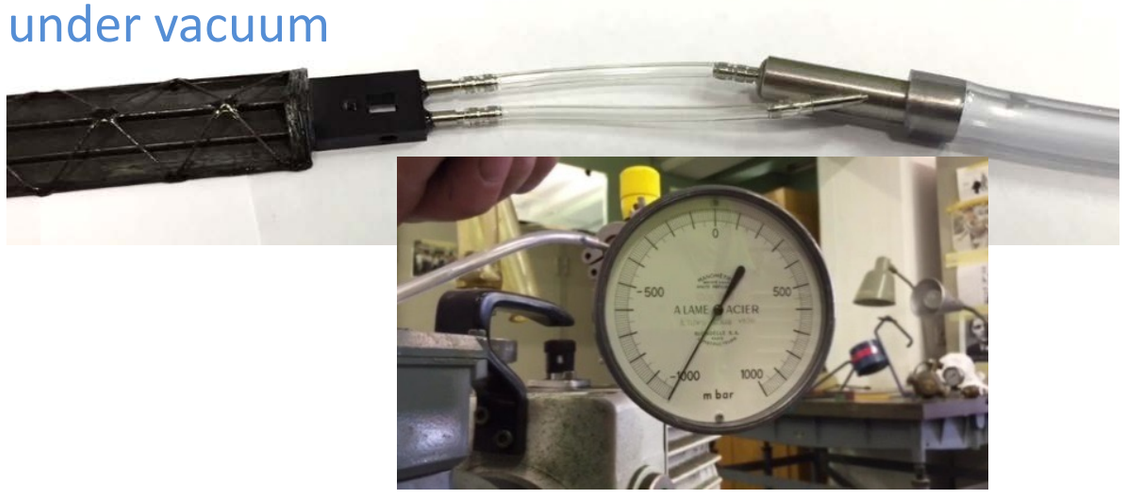
Objective: The maximum inside pressure that a stave can withstand before burst

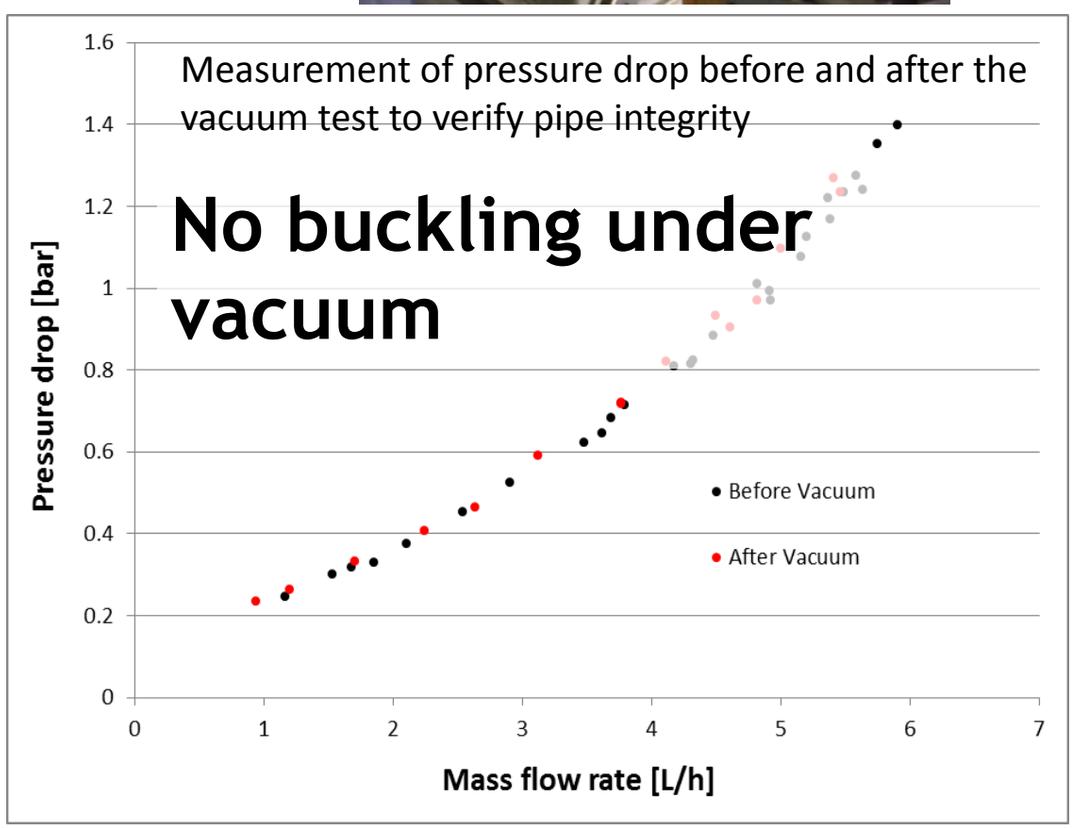
Pipe Burst @ 51bar



- **Vacuum** IB

Objective: Verify stave and plastic tube stability under vacuum

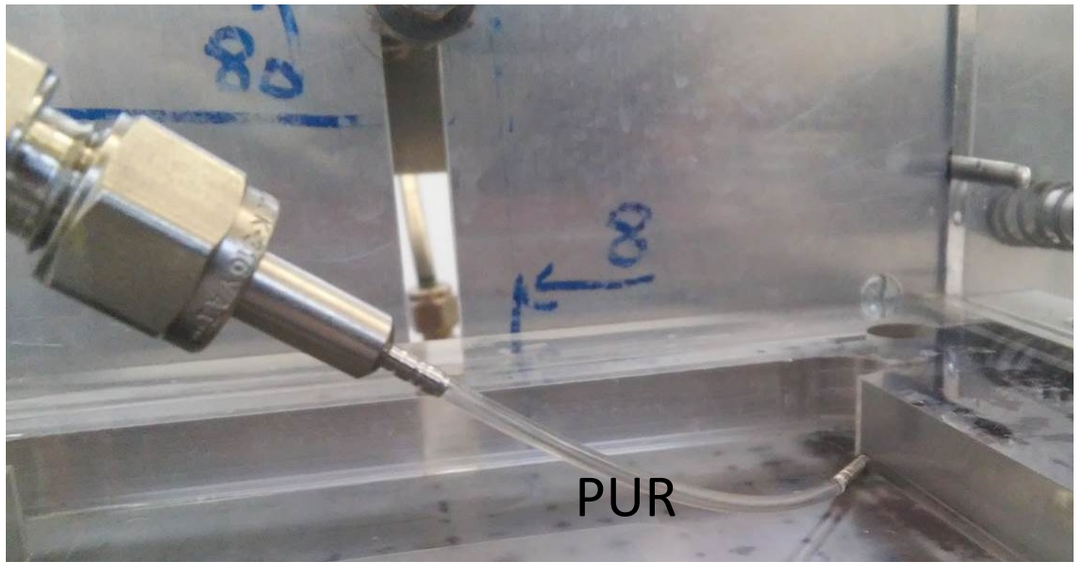


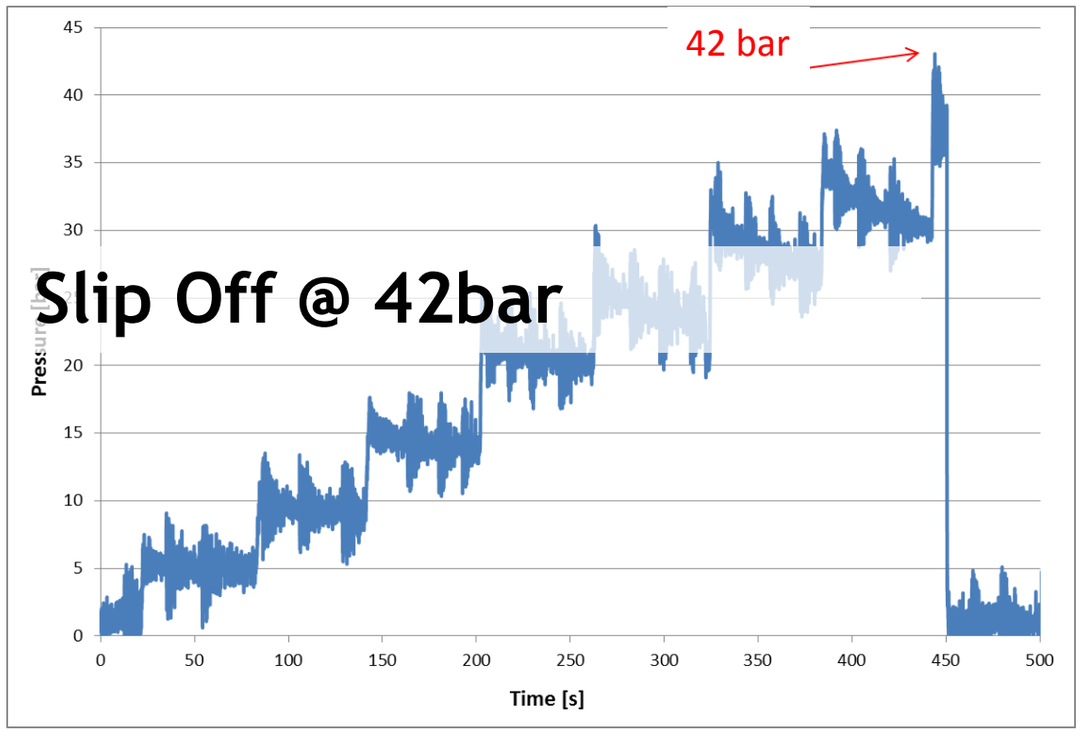


IB Stave — cooling lines test

Slip Off pressure

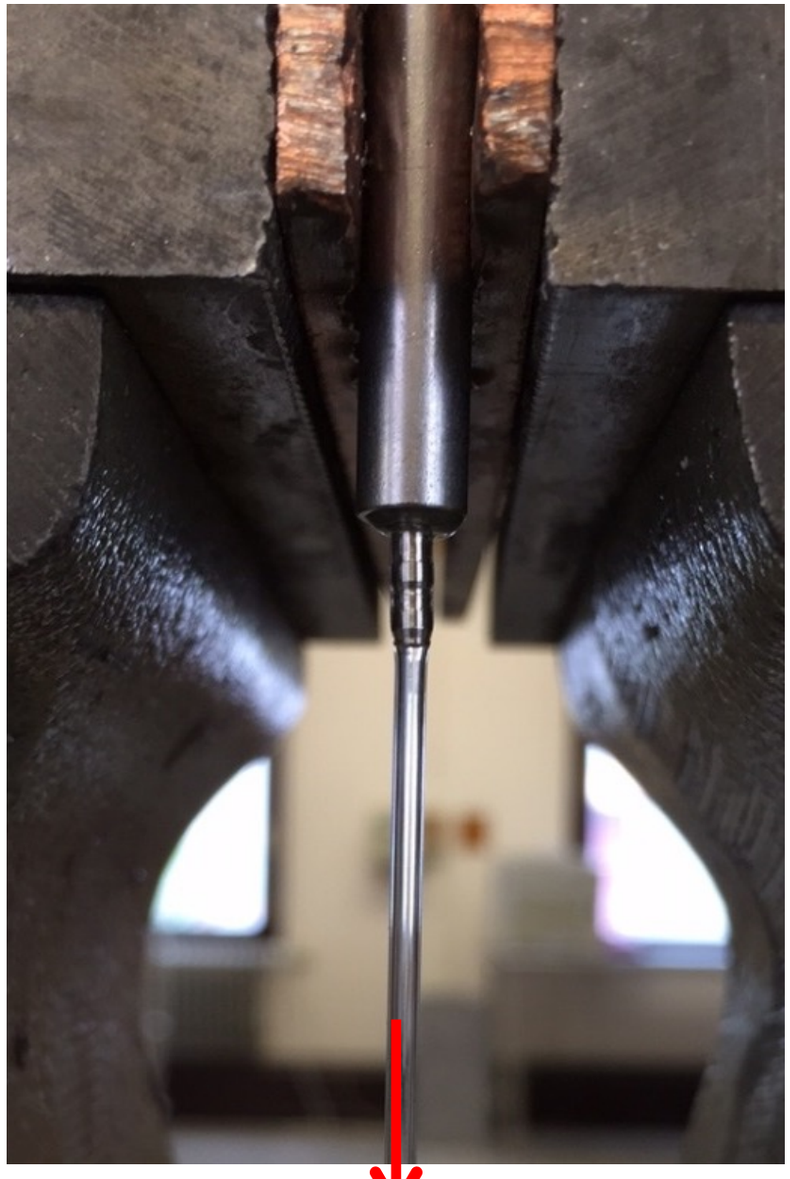
The maximum pressure required to slip off a plastic flexible tube from the SS fitting





Pull out FORCE

The maximum required force to pull a plastic flexible tube out of a SS fitting

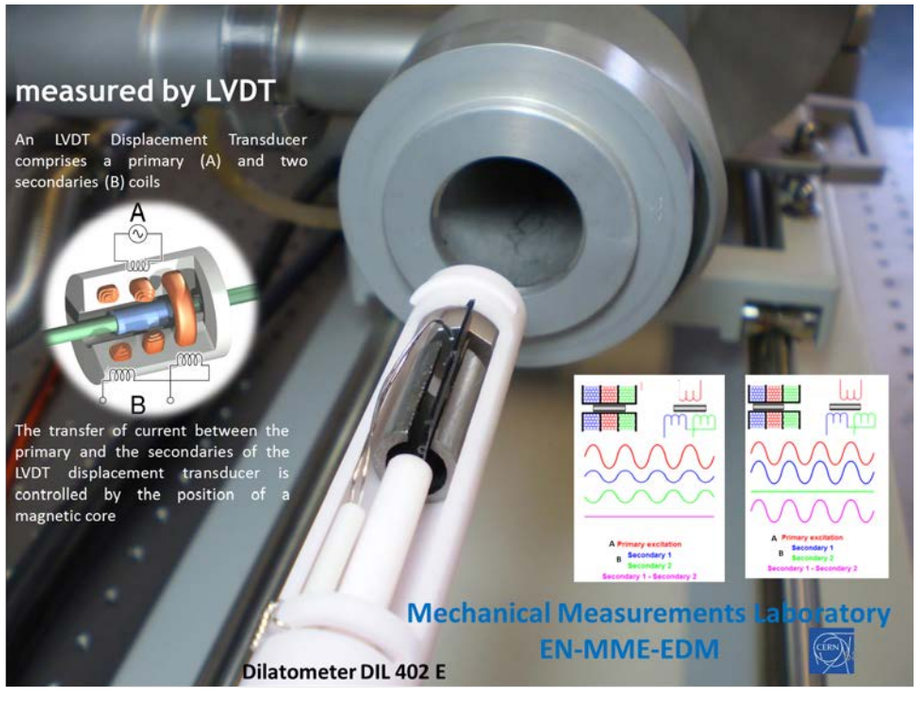


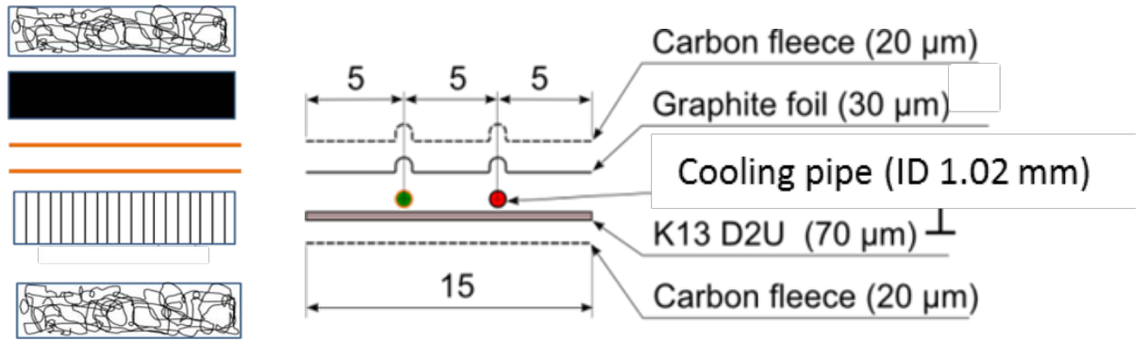
IB Stave — thermo-elastics test

Objective: Determine stave stability respect to thermal variation.

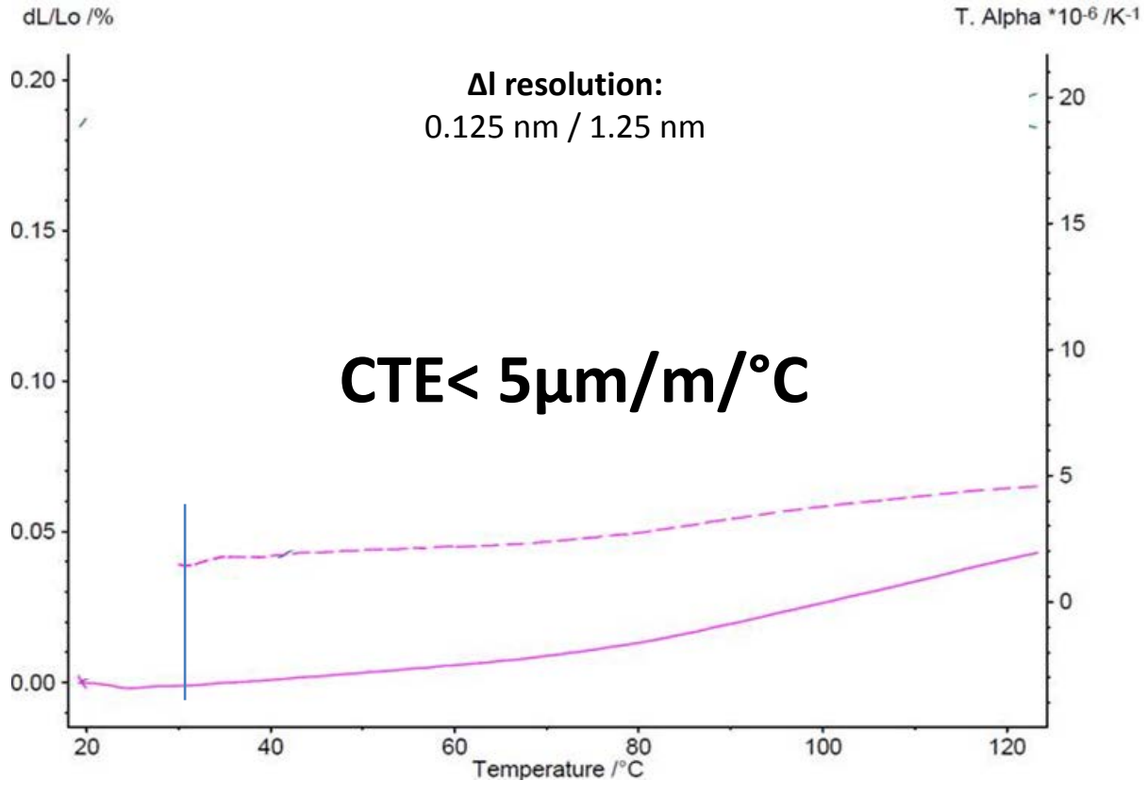
Mechanical Measurements Laboratory

EN-MME-EDM





DIL 402	
Atmosphere	Helium at 150 ml/min
Calibration standard	Graphite
temperature program	RT to 150ºC at 1ºC/min
Sample length	approx. 25 mm



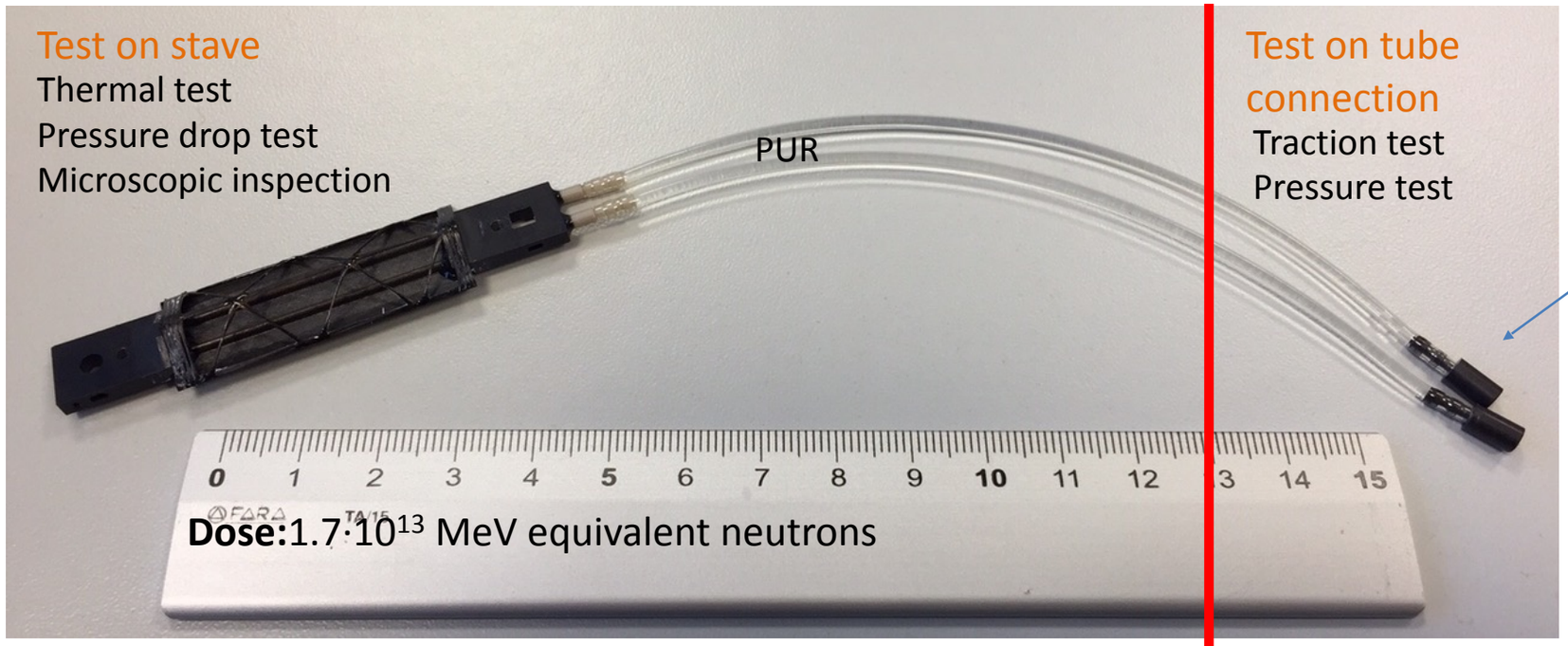
Δl resolution:
0.125 nm / 1.25 nm

CTE< 5µm/m/°C

IB Stave — cooling pipes/water compatibility test

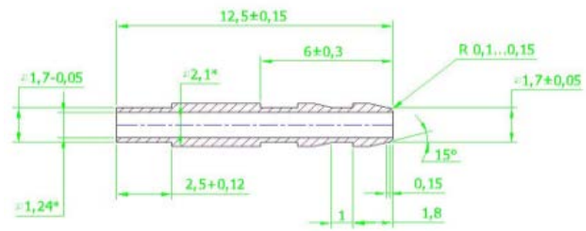
Objective: investigate the interaction of irradiated water with polyimide tubes
investigate the effect of radiation on the connection of PUR tubes to stave fittings

✓ **Test campaign before and after irradiation**

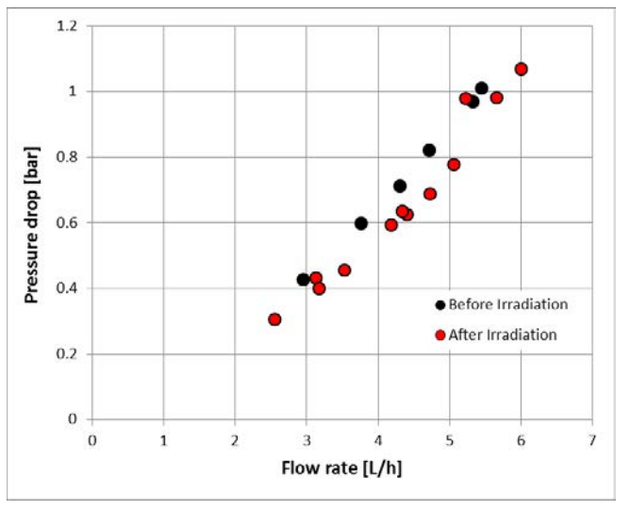


Dose: $1.7 \cdot 10^{13}$ MeV equivalent neutrons

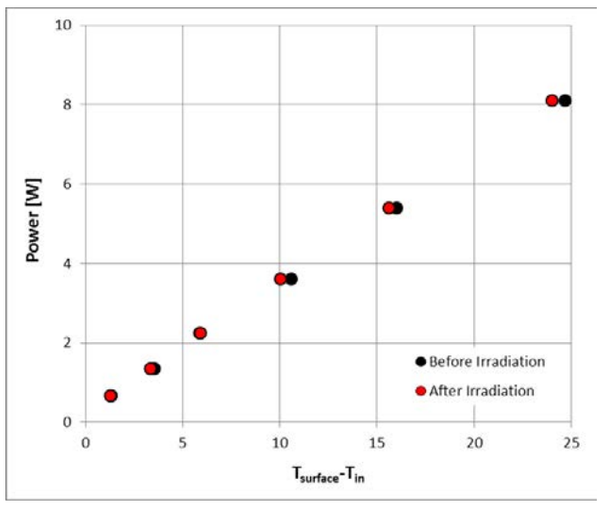
the caps have the same geometry of the stave fittings



stave fittings

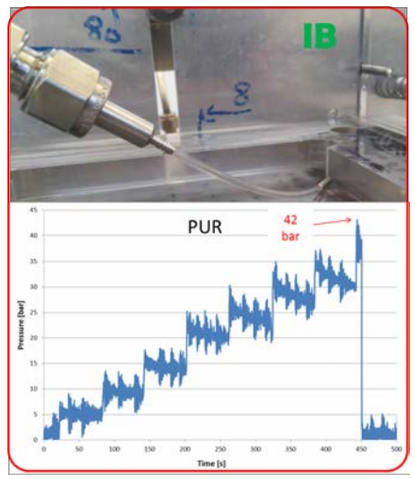


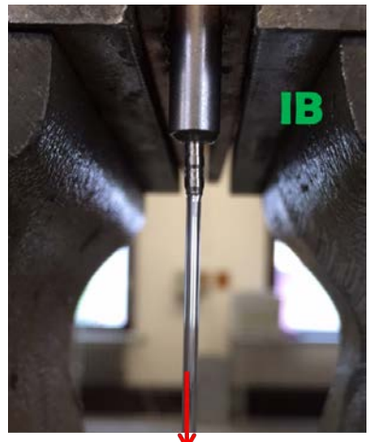
Pressure drop



Heat transfer

No effects on stave cooling performance





IB PUR max weight 4 kg

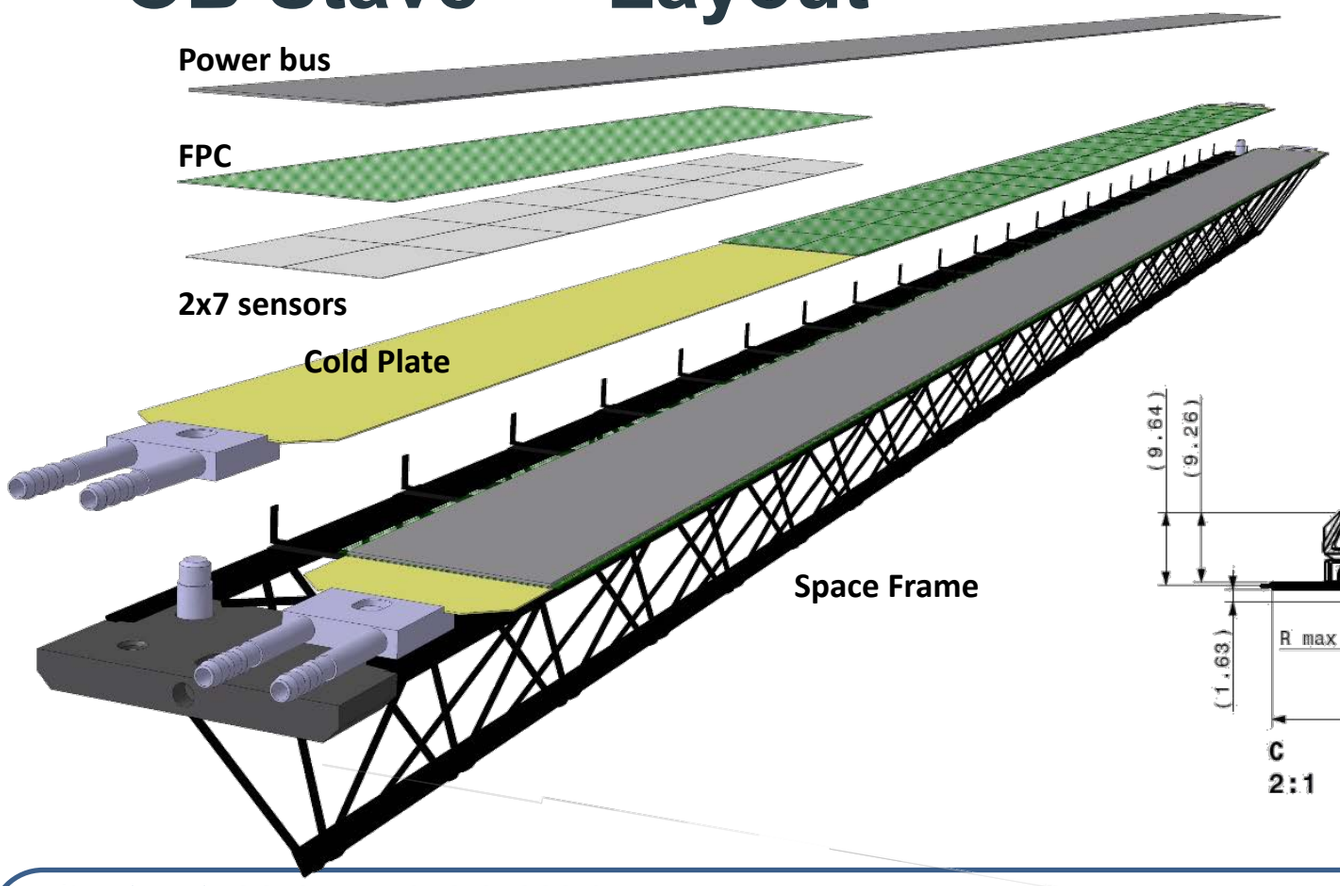
42 bar, 4 kg before and after

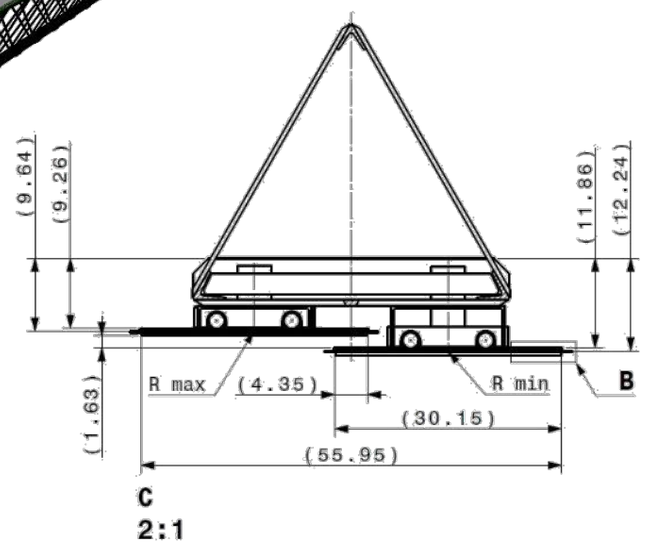
No effects on the pipe connection

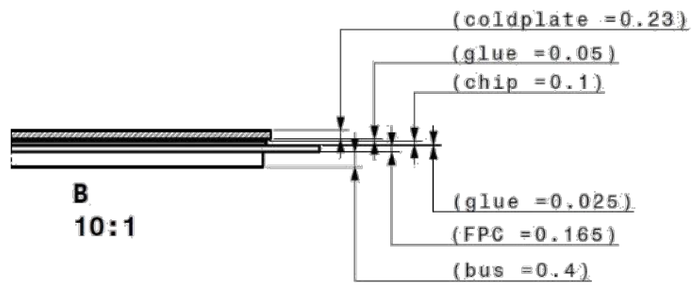
ALICE

OB Stave

OB Stave — Layout







Radius (mm)196, 245.4, 343.8, 393.3

Nr. staves: 24,30,42,48

Nr. Chips/ module:2x7

Length in z (mm): 844.2 (ML), 1477.5 mm (OL)

Nr. module/ stave: 4 (ML), 7(OL)

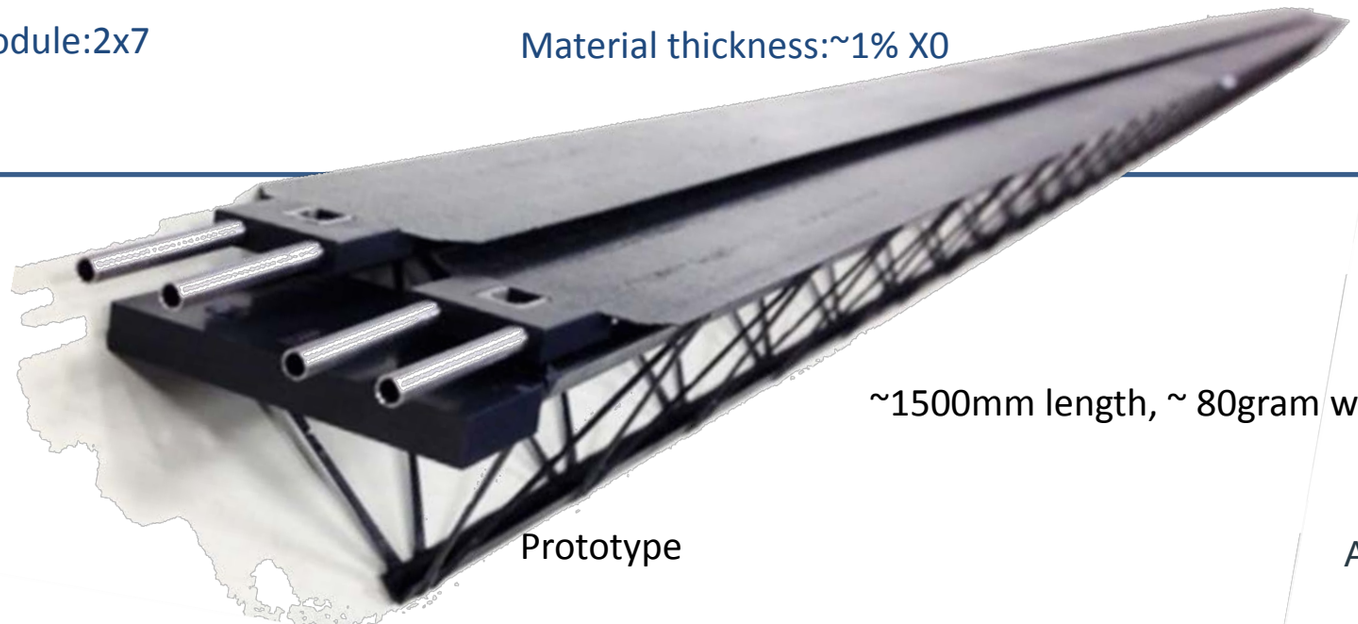
Material thickness:~1% X0

Coolant Single-phase H_2O leak-less

Pixel operational temperature < 30°C

Pixel max temperature non-uniformity < 5°C

Chip Power dissipation< 100mW/cm^2

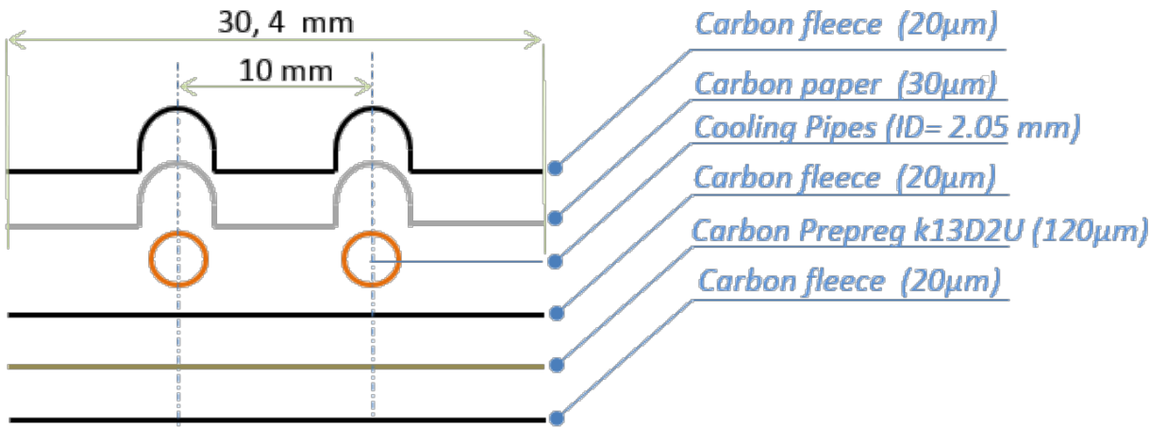


~1500mm length, ~ 80gram weight

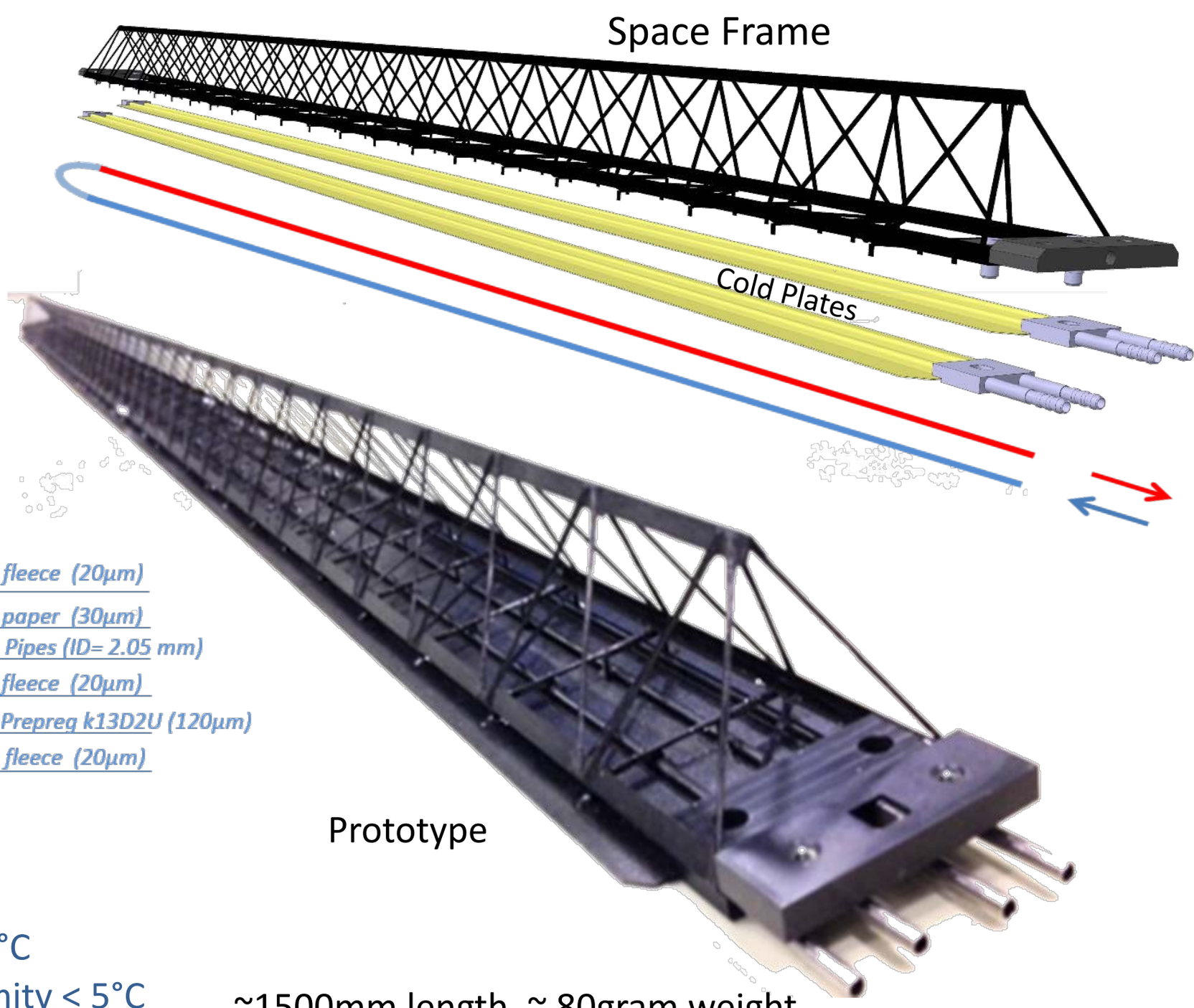
Prototype

OB Stave — Layout

Cold Plate



Space Frame



Prototype

Coolant Single-phase H_2O leak-less

Pixel operational temperature < 30°C

Pixel max temperature non-uniformity < 5°C

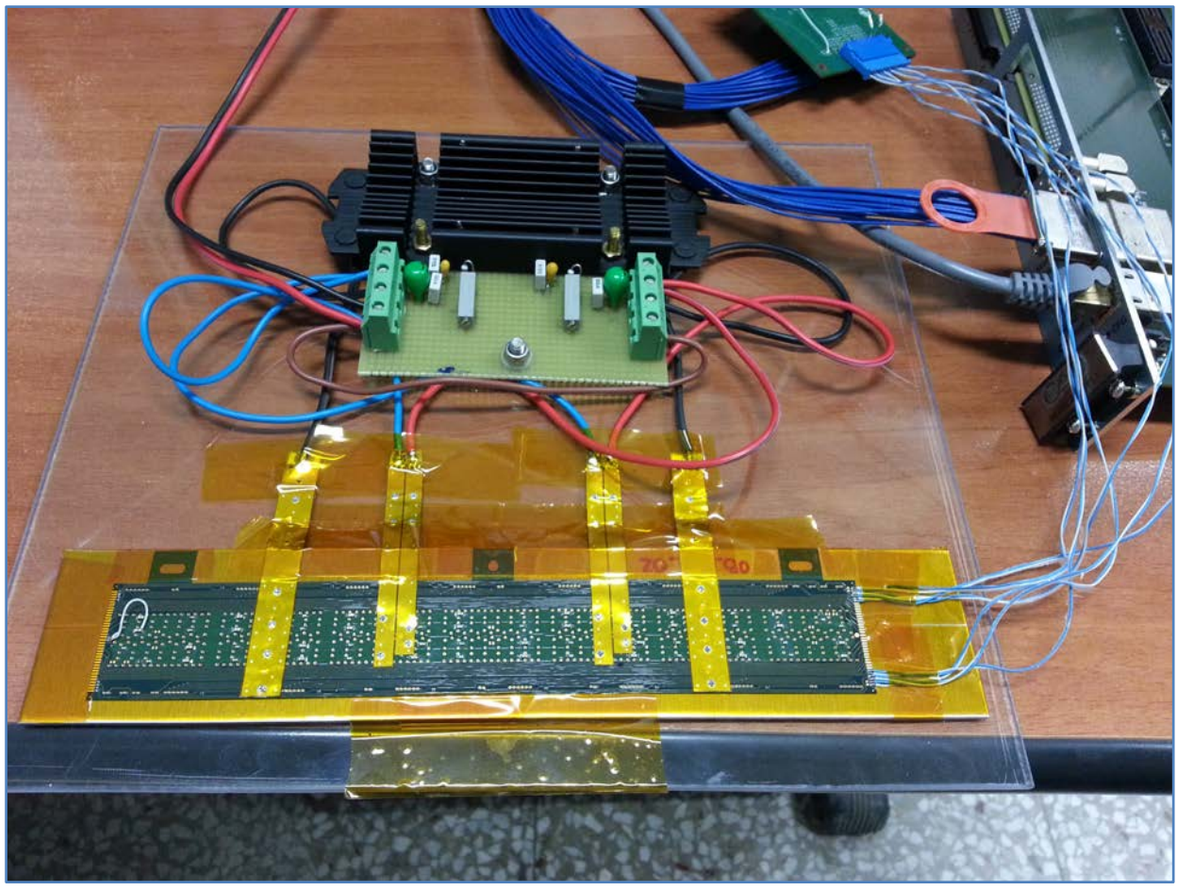
Chip Power dissipation< 100mW/cm^2

~1500mm length, ~ 80gram weight

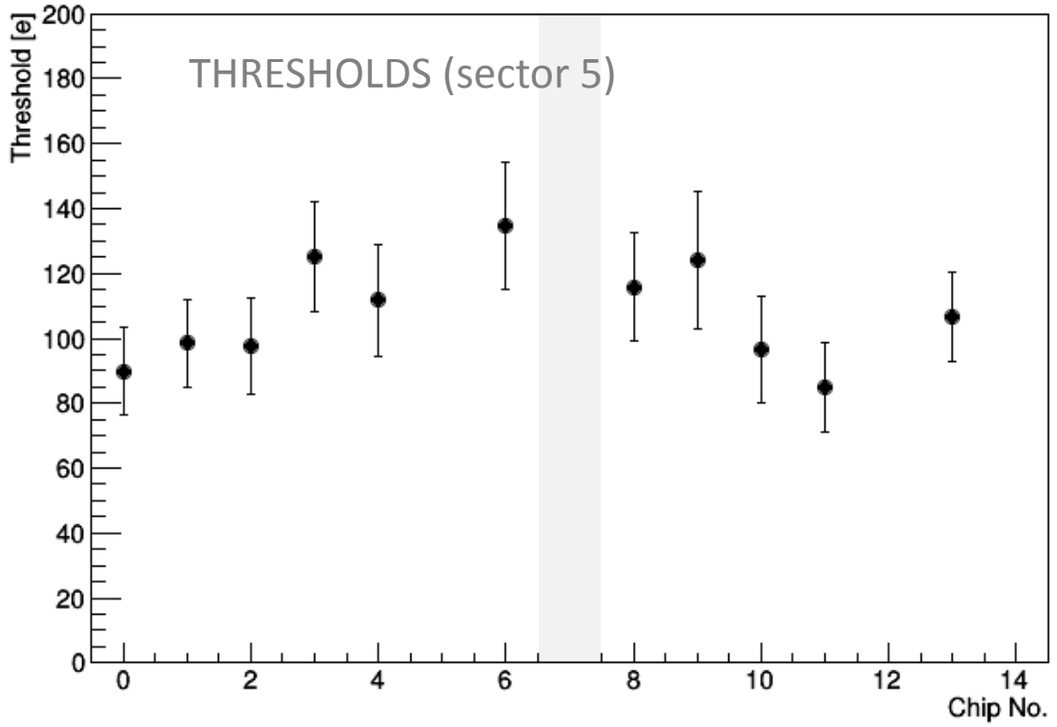
OB HIC Test Setup and Results

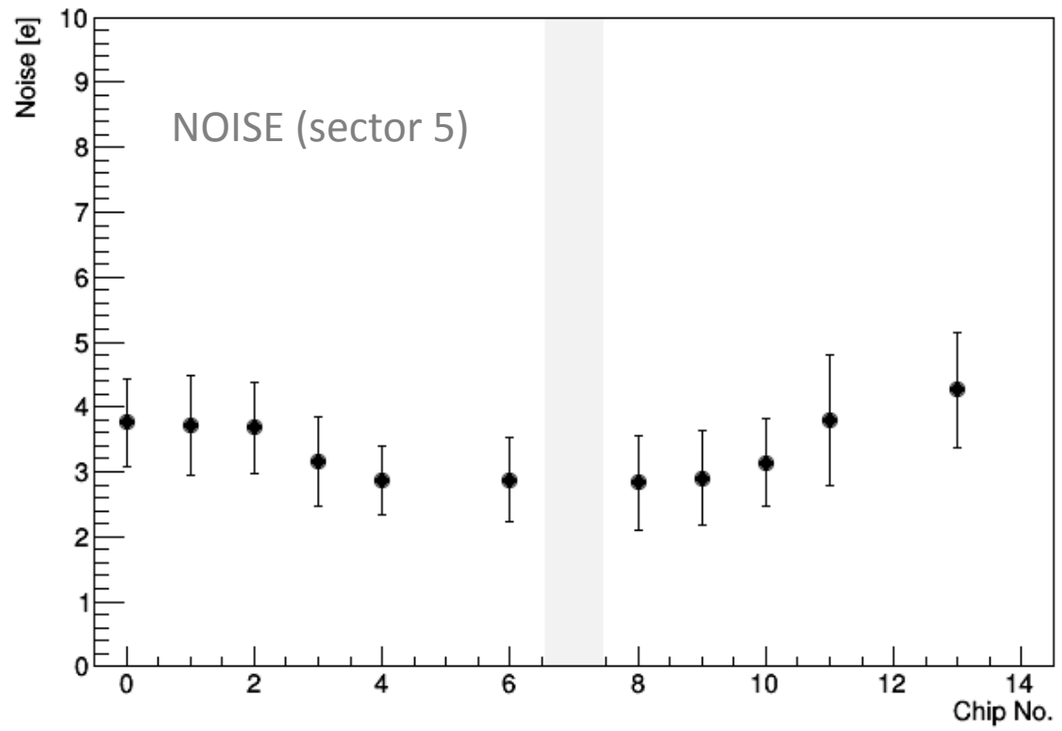
8 OB HIC have being built and characterized

Results similar to IB HIC

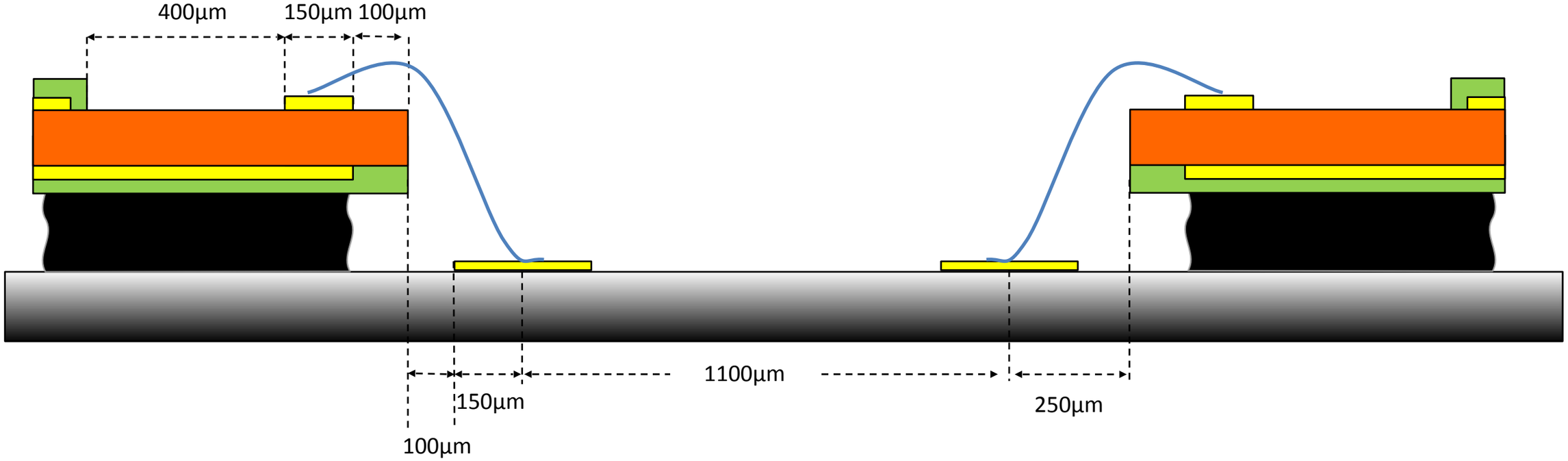


Test of an OB HIC. Power is supplied from external voltage regulators through the cross cables, soldered to the FPC



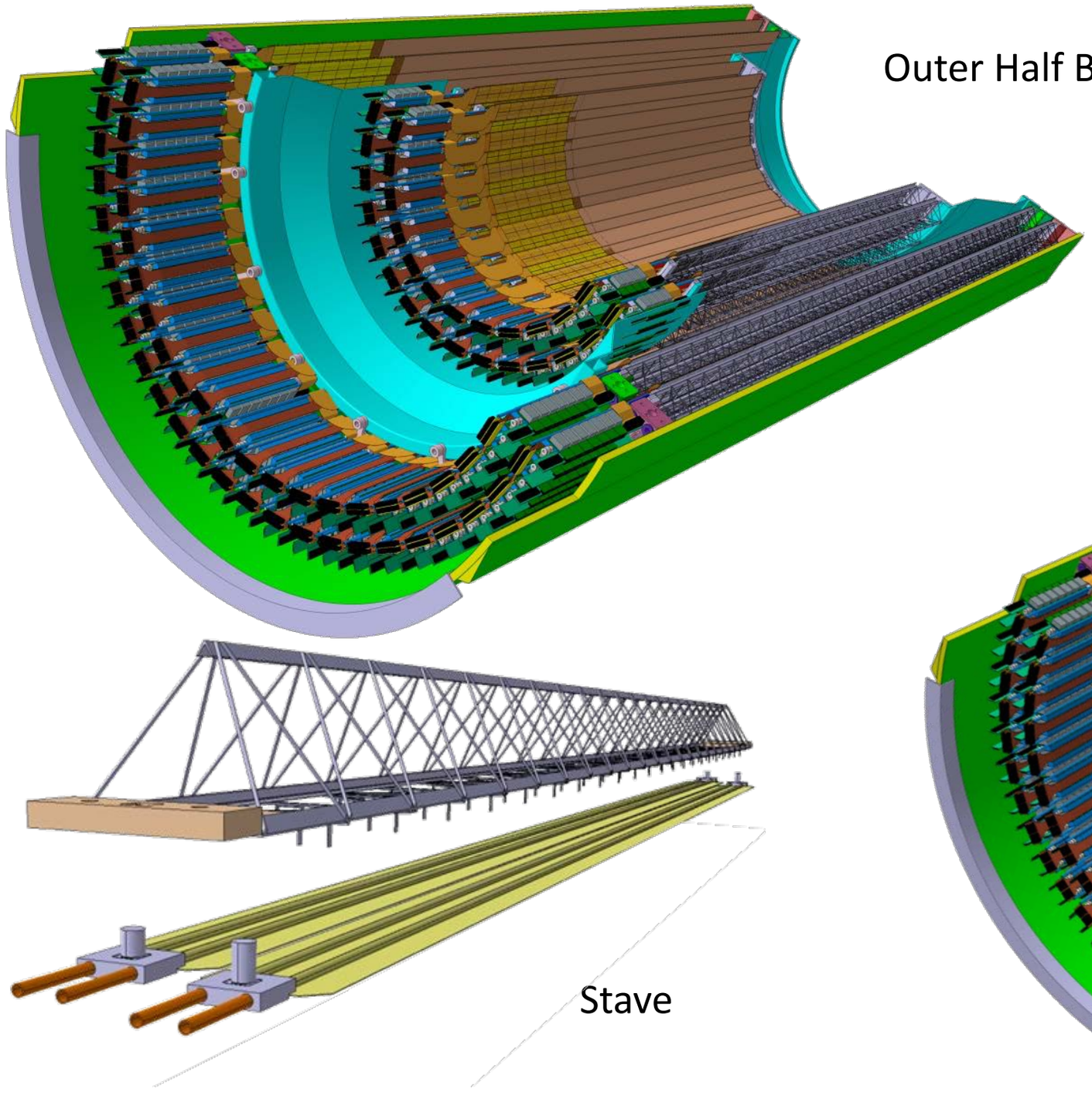


Schematic view of the FPC-chip interconnection



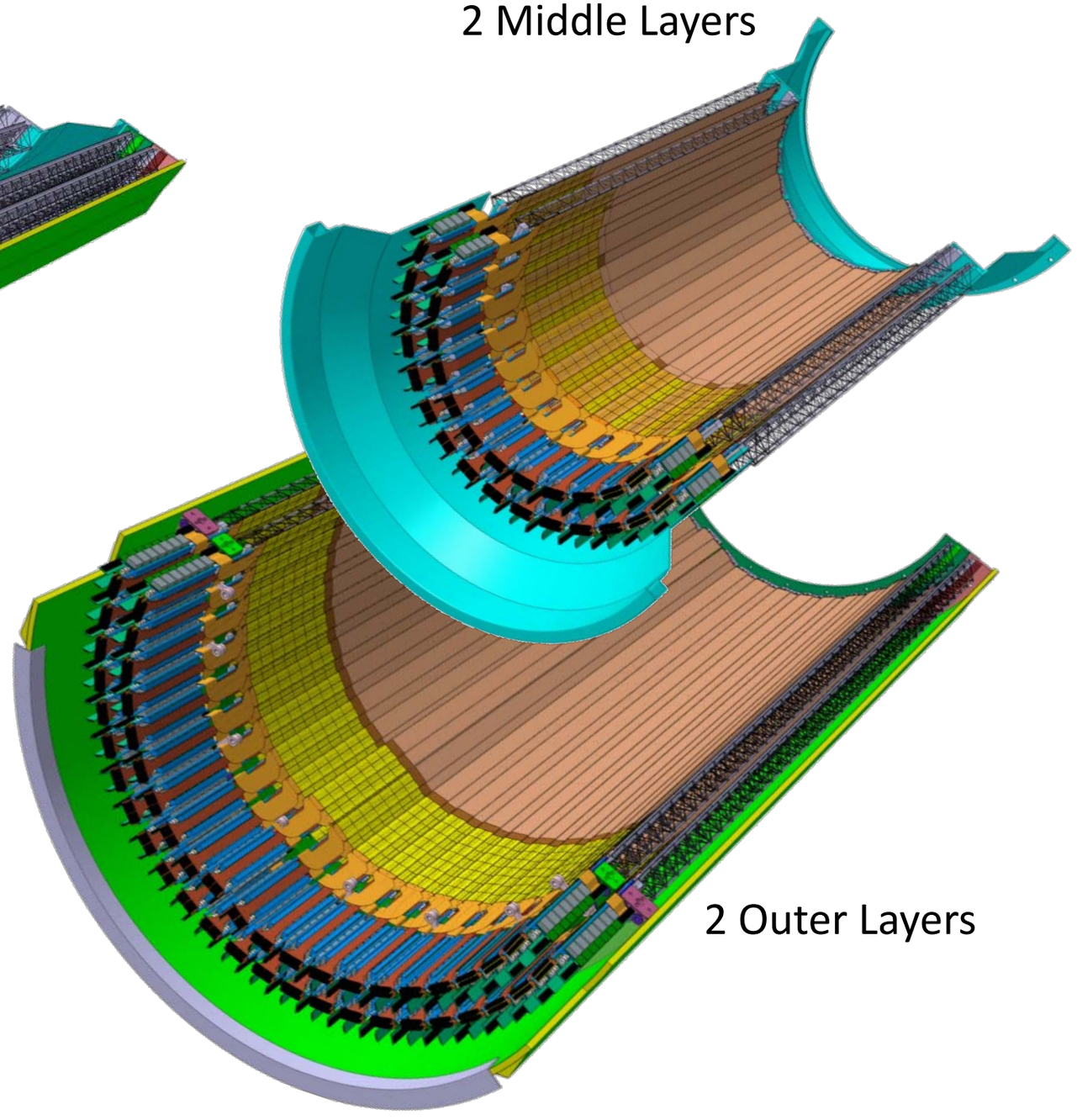
Detector Layout

ITS Outer Detector Barrel



Outer Half Barrel

Stave



2 Middle Layers

2 Outer Layers

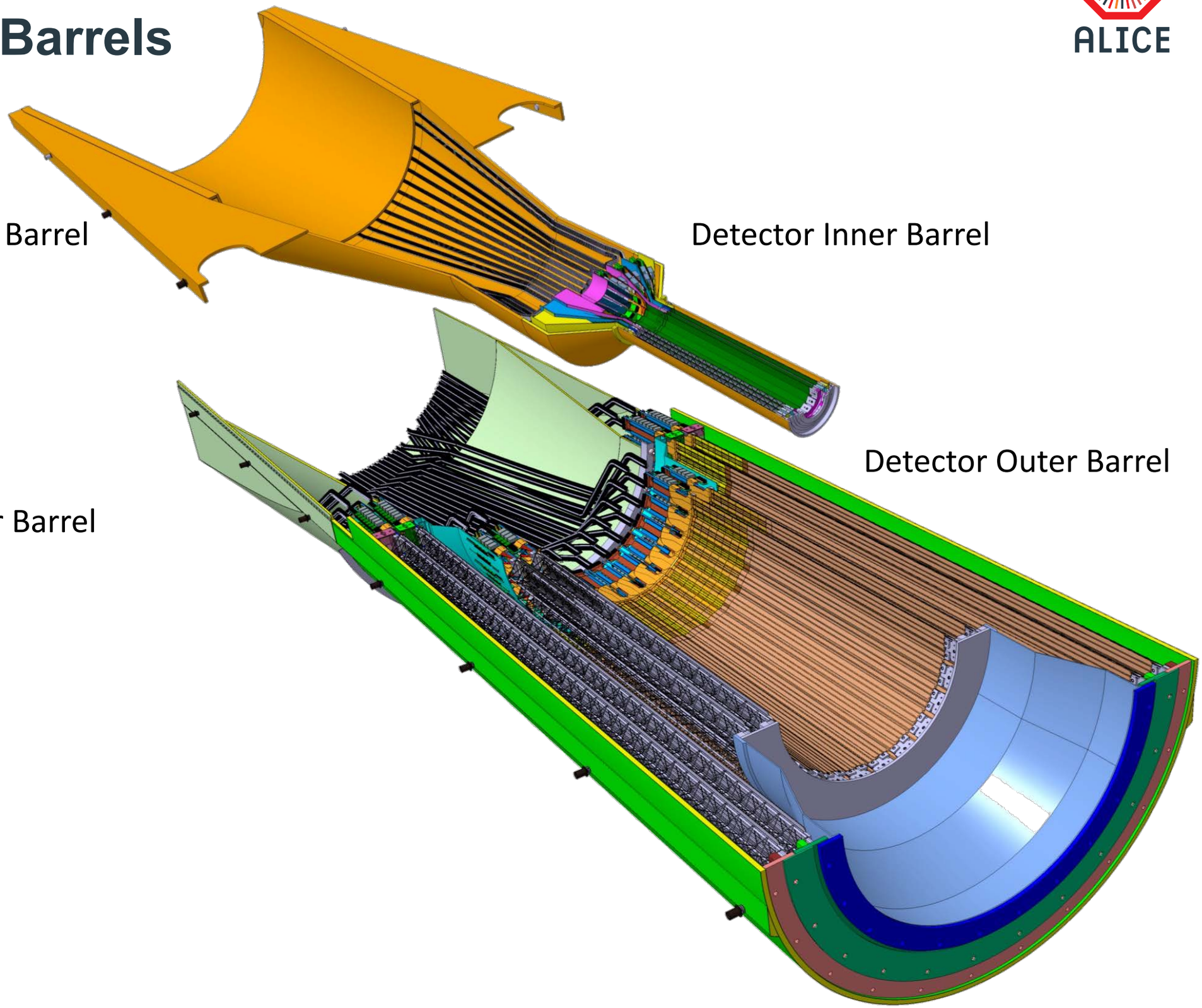
Detector Barrels

Service Inner Barrel

Detector Inner Barrel

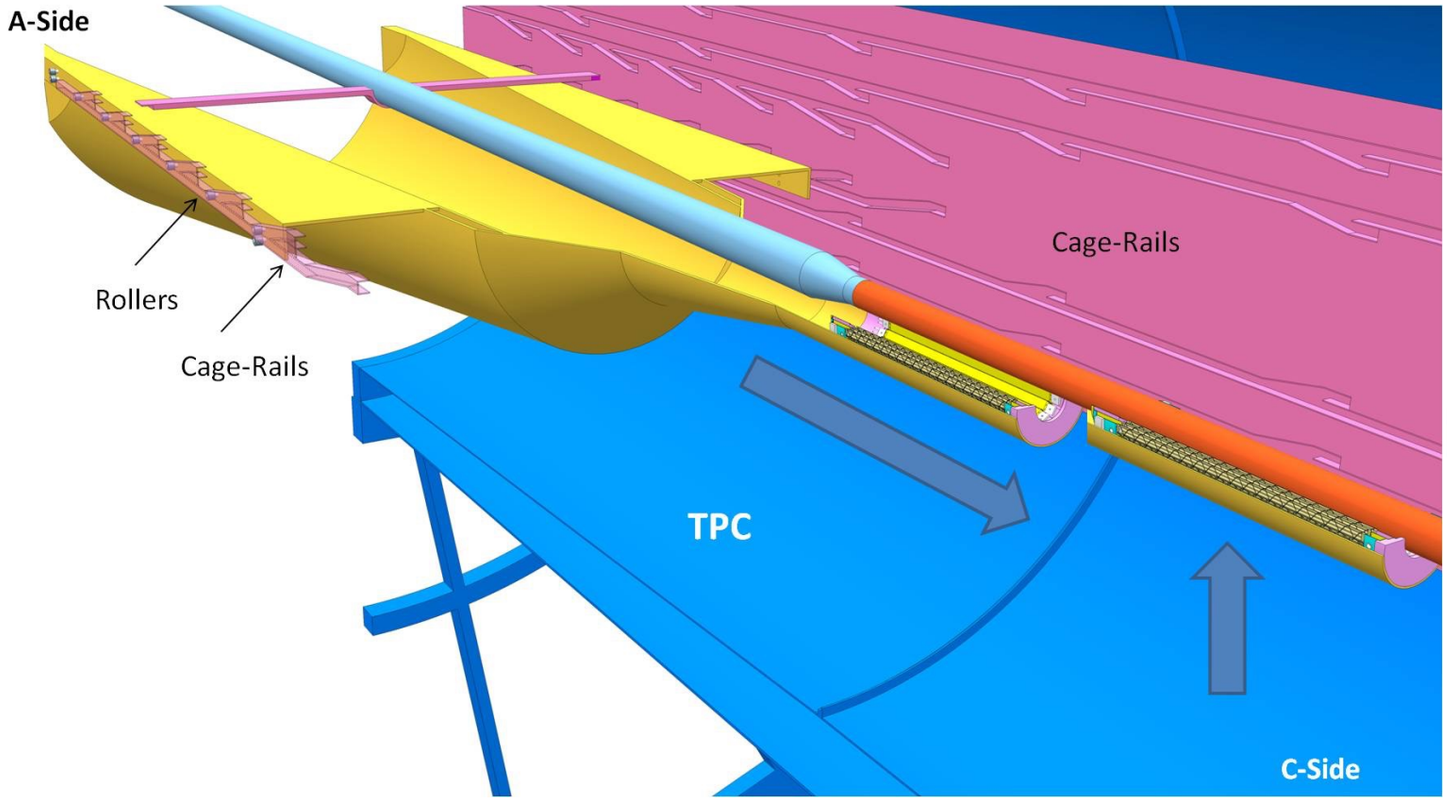
Service Outer Barrel

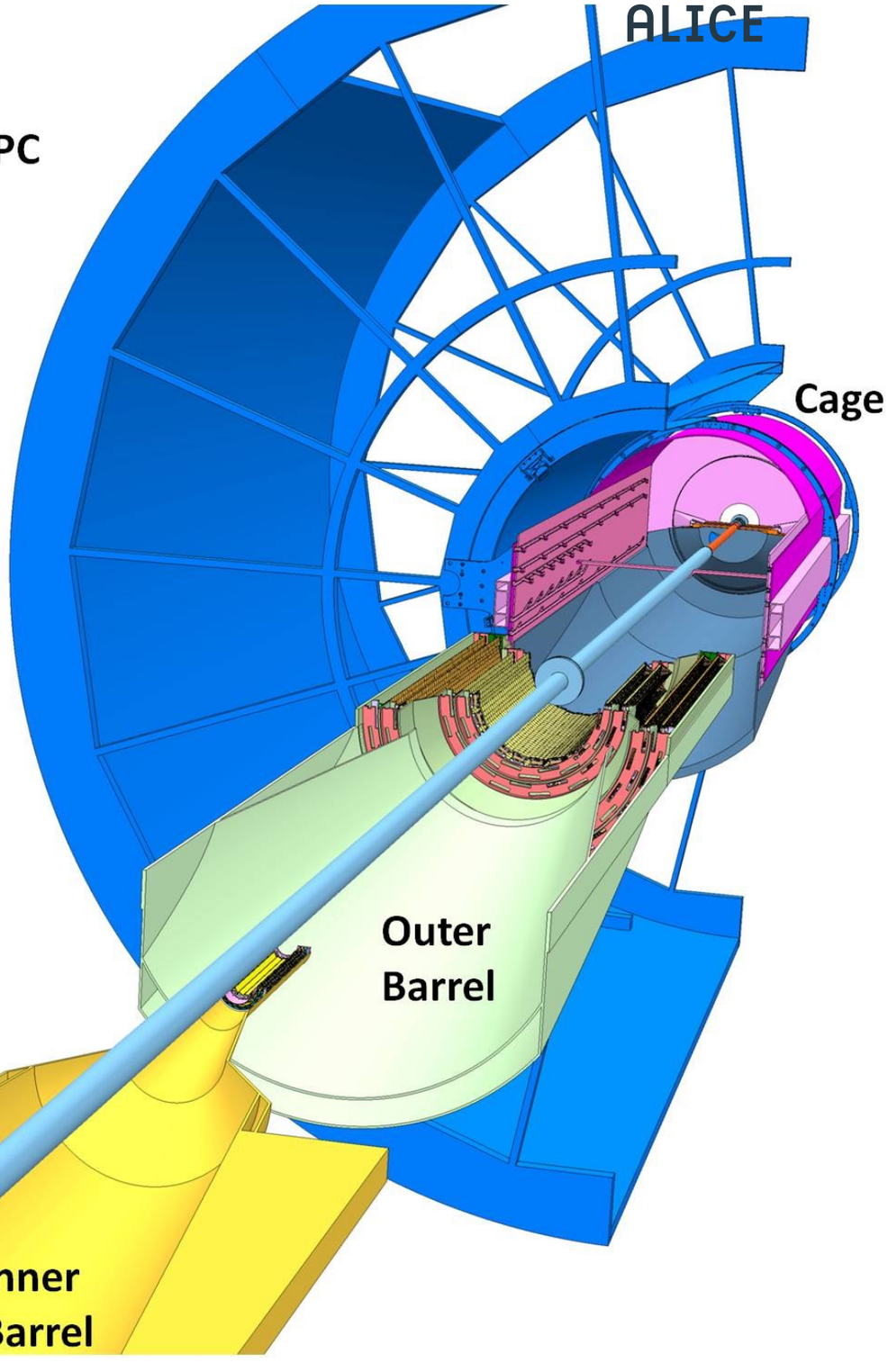
Detector Outer Barrel



Mechanical Integration

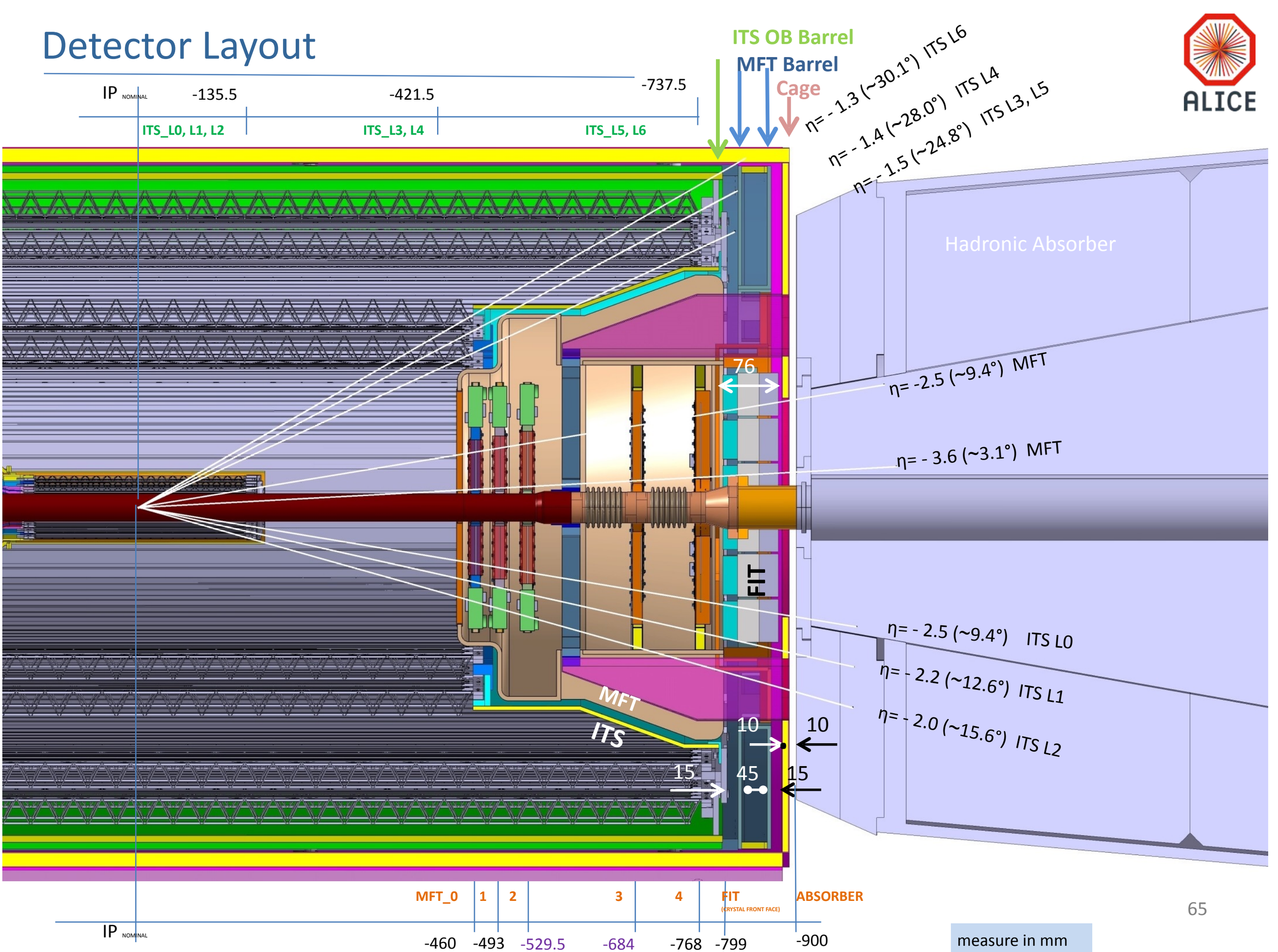
Installation of IB half-barrel





Half-barrel utilises rollers fixed to the Cylindrical Structural Shell to slide along a rail system supported by the cage

Detector Layout



Detector Layout

A Large Ion Collider Experiment

ALICE

η= - 1.5 (~24.8°) ITS L3, L5

η= - 1.4 (~28.0°) ITS L4

η= - 1.3 (~30.1°) ITS L6

-737.5 -421.5 -135.5 IP NOMINAL

ITS_L5, L6 ITS_L3, L4 ITS_L0, L1, L2

(12,65°) V0A+ ext

(11,45°) PMD

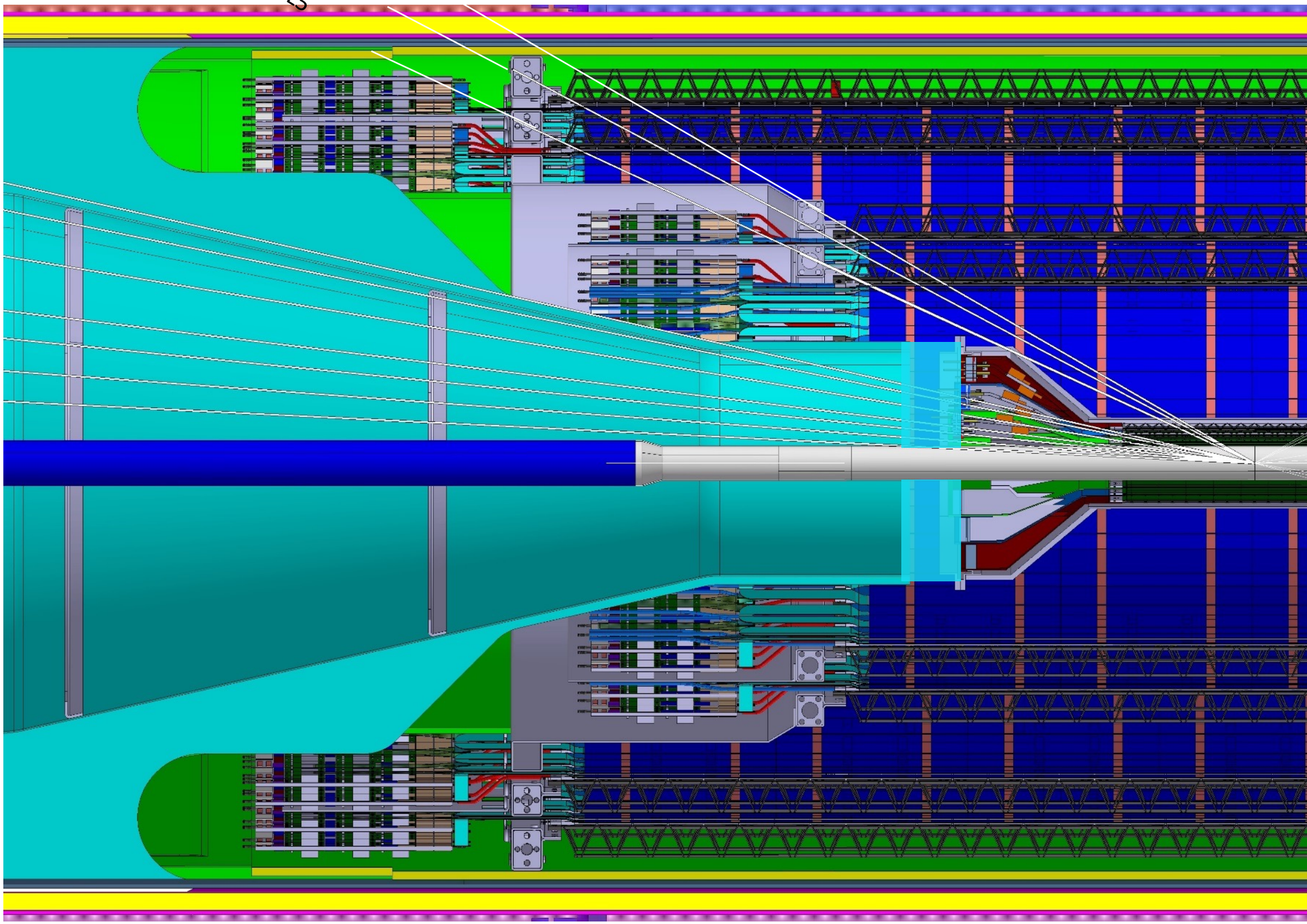
(9,4°) ITS L0

(6,96°) V0A+

(5,7°) FOCAL EFCA 2014

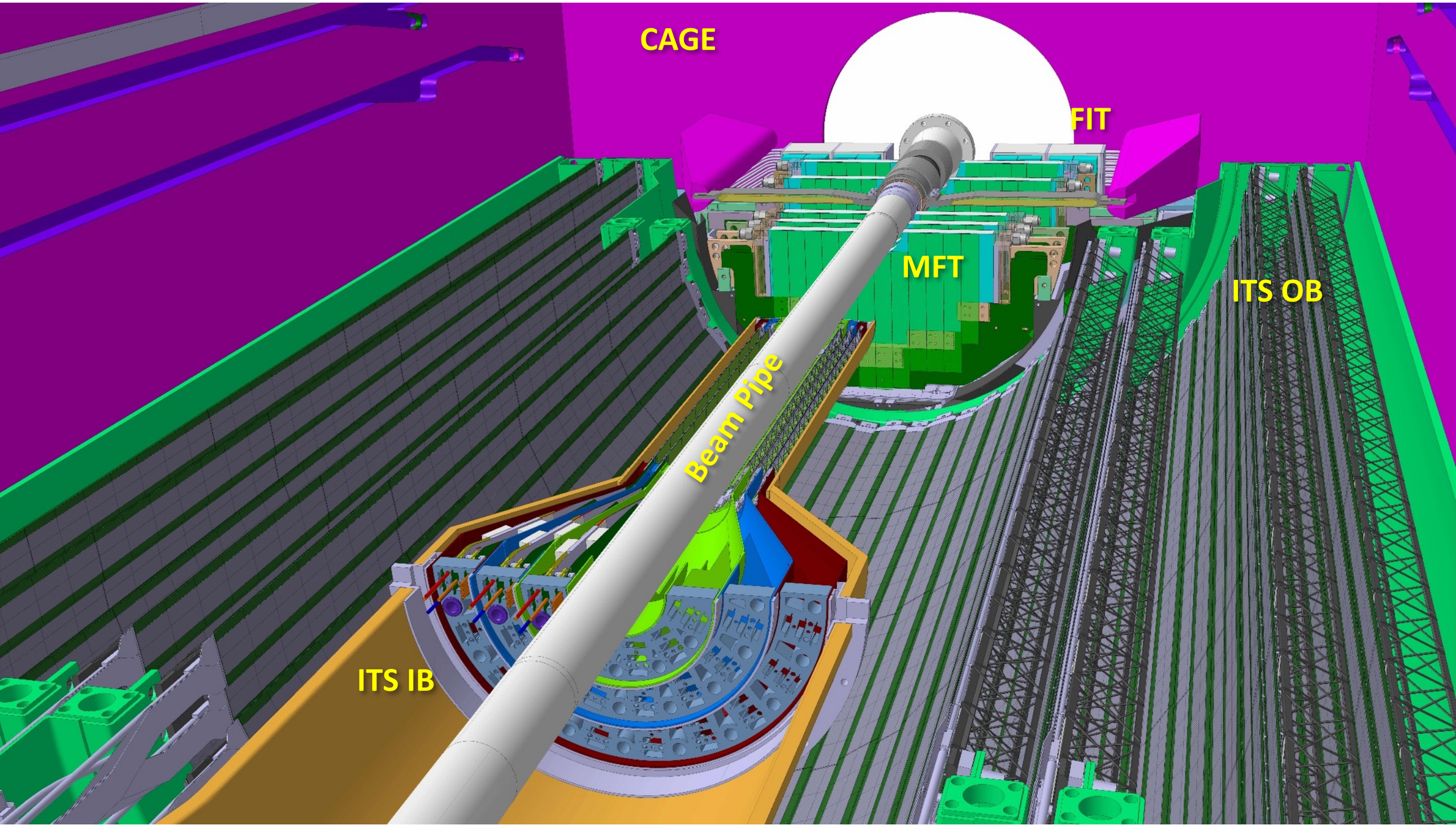
(4,22°) FOCAL MB 2015

(2,83°) T0A+



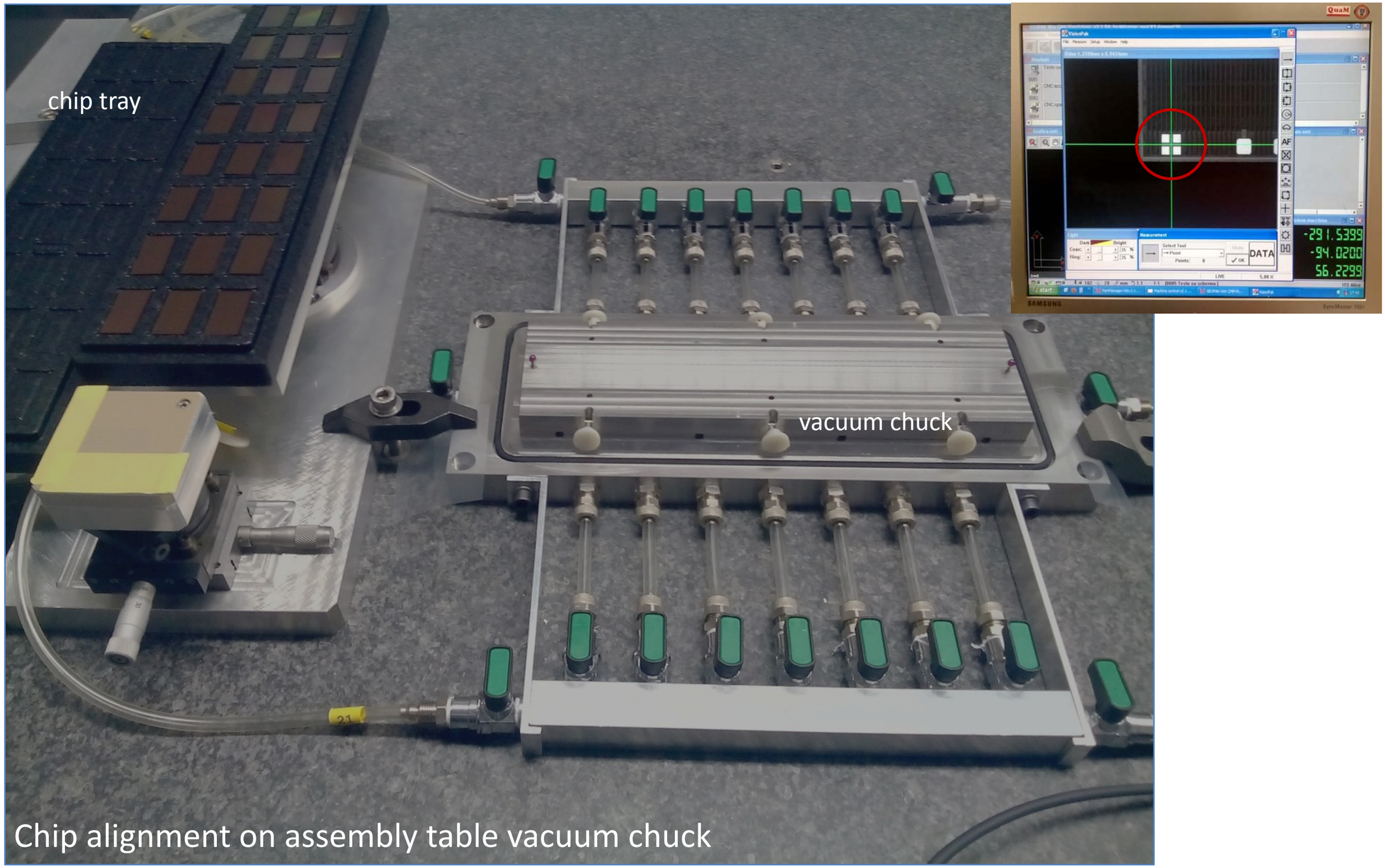
measure in mm

Detector Layout



HIC Assembly

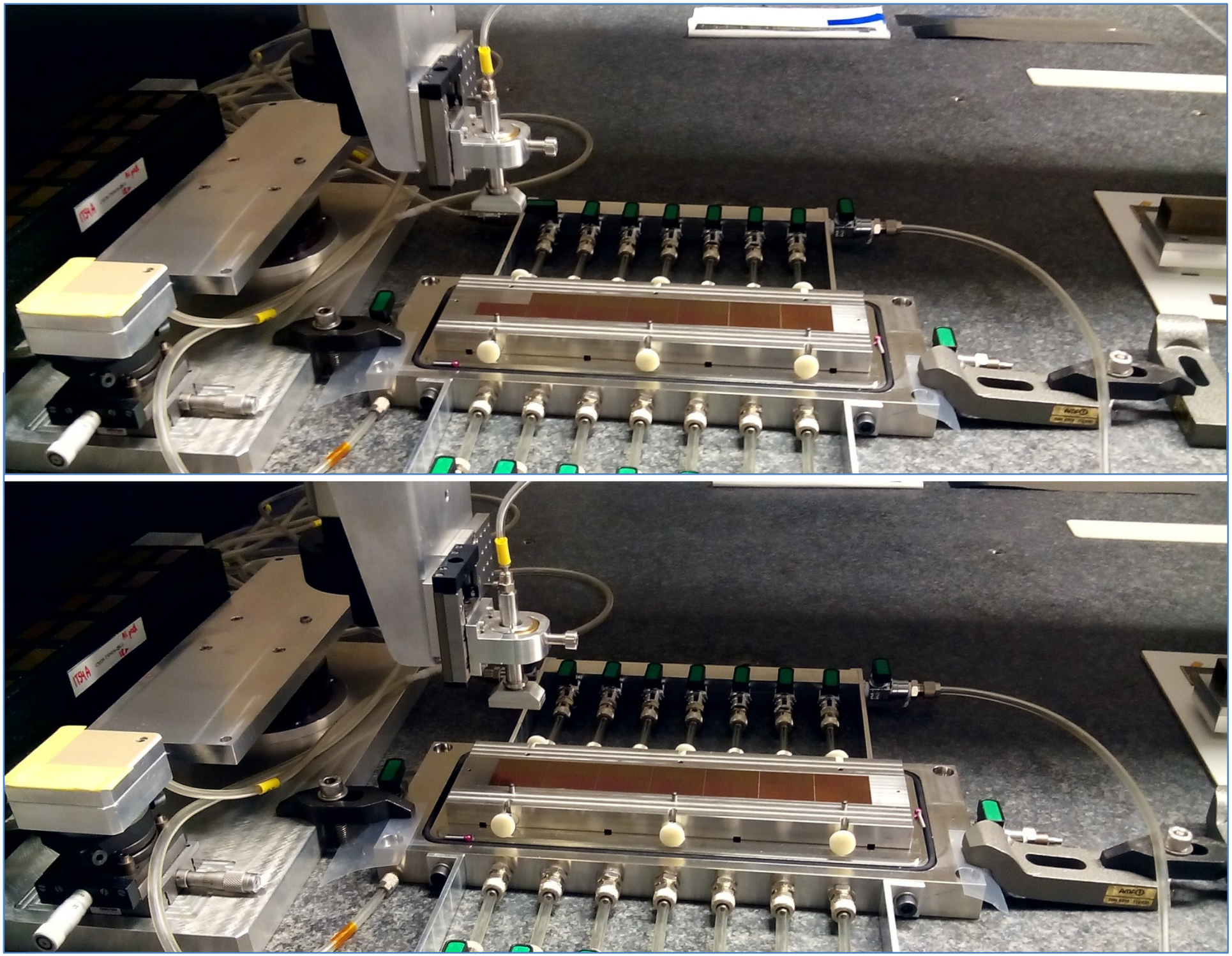
HIC Assembly



HIC Assembly

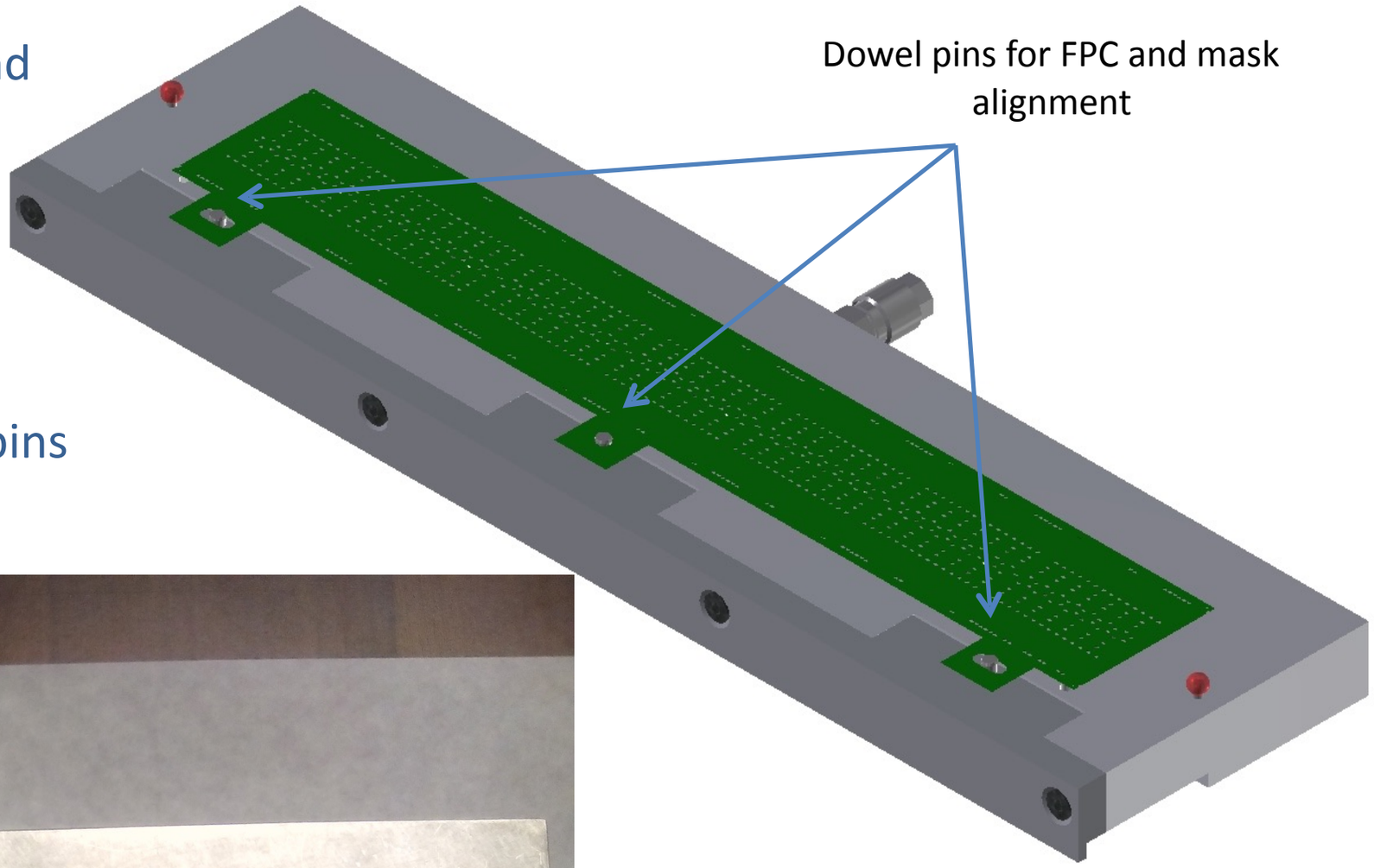
Chip alignment on assembly table vacuum chuck

HIC Assembly

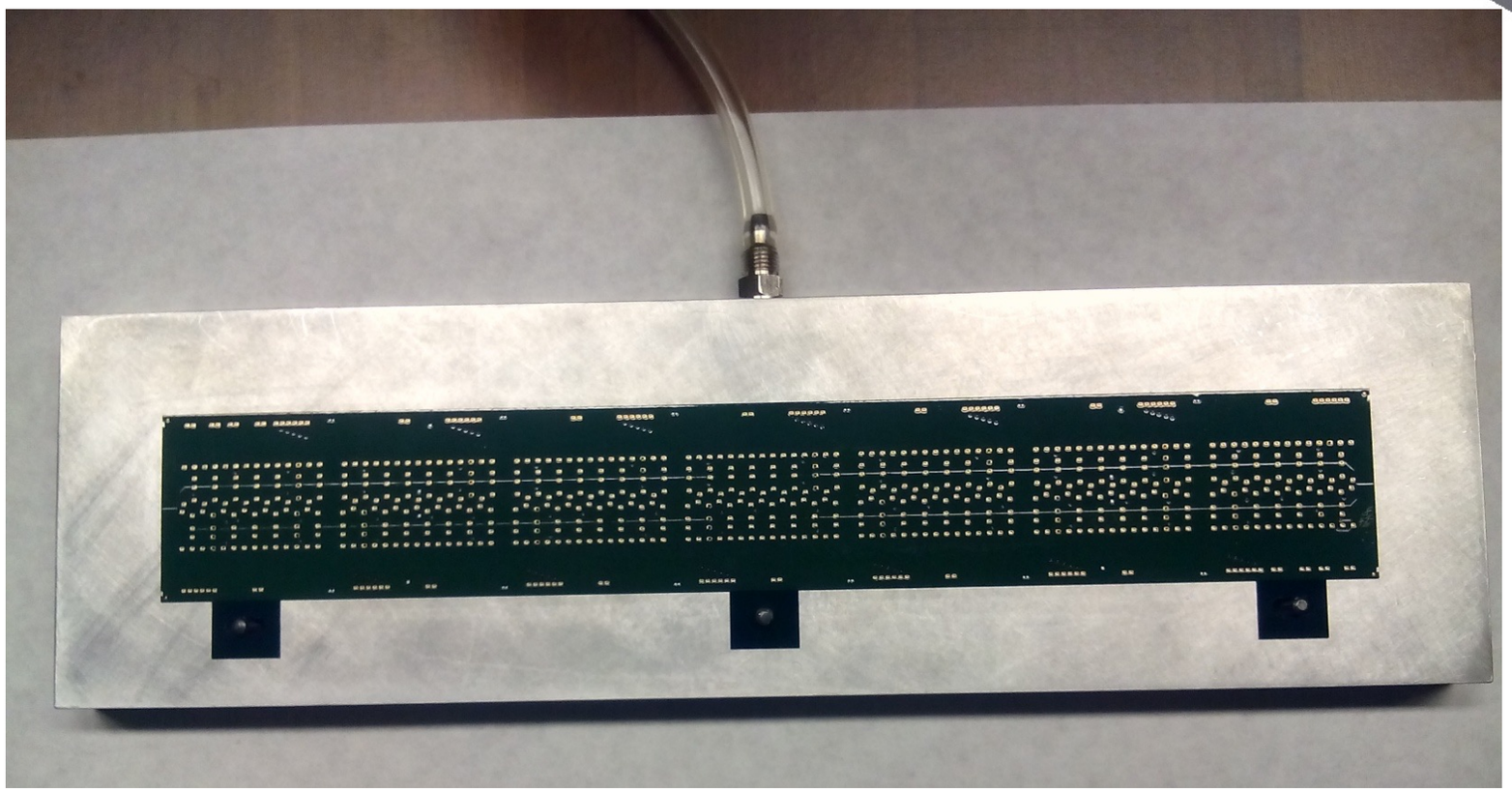


HIC Assembly

FPC is placed on pick-up tool and vacuum is applied to flatten it



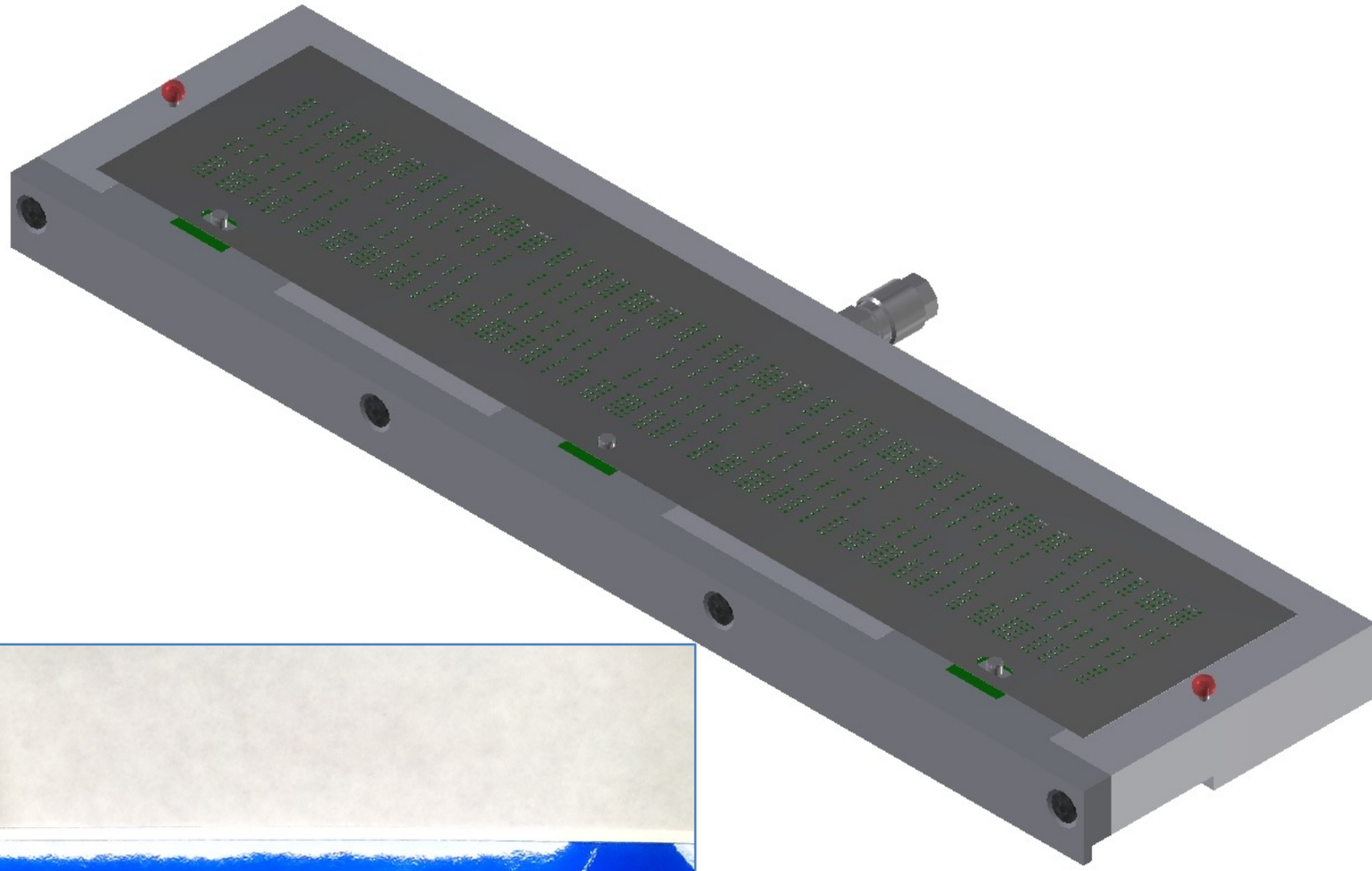
FPC alignment based on dowel pins

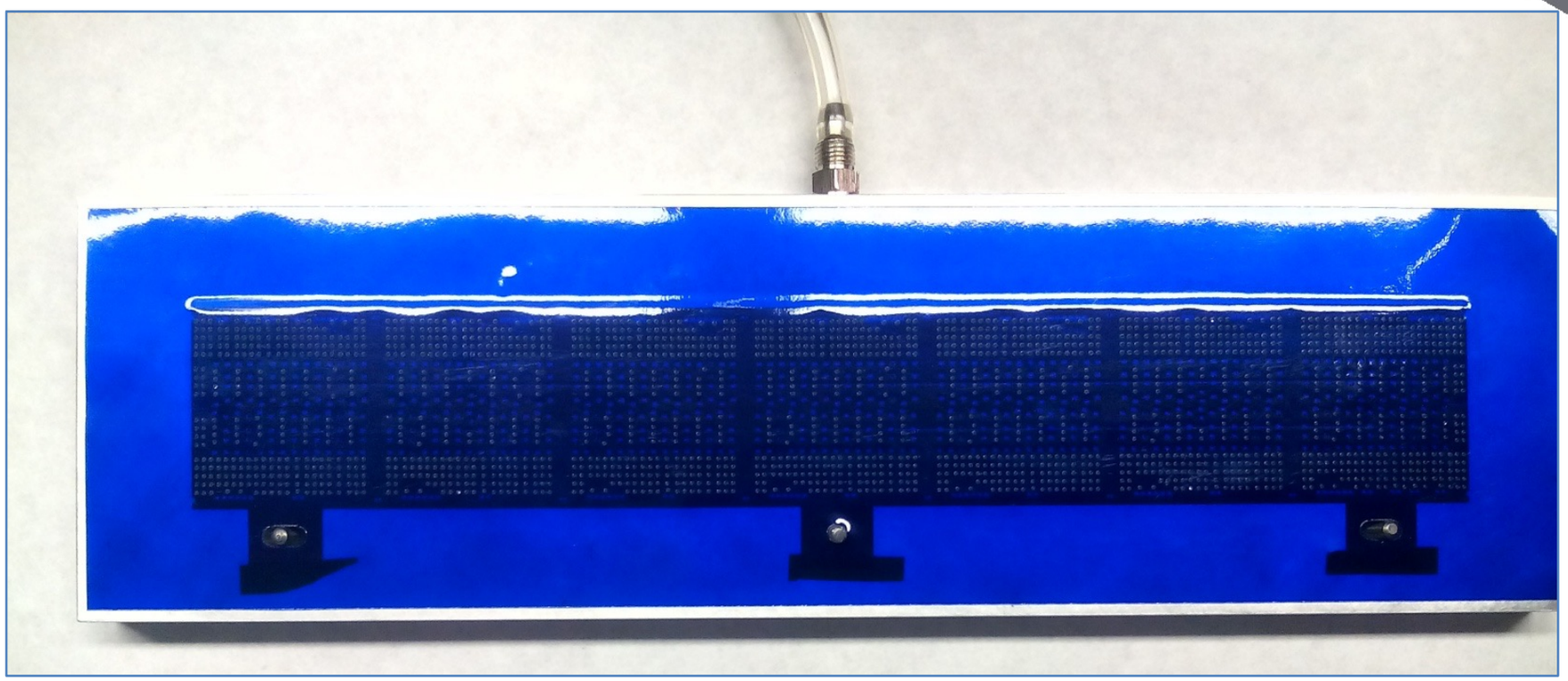


HIC Assembly

An adhesive mask is placed above the FPC to dispense a precise pattern of glue droplets

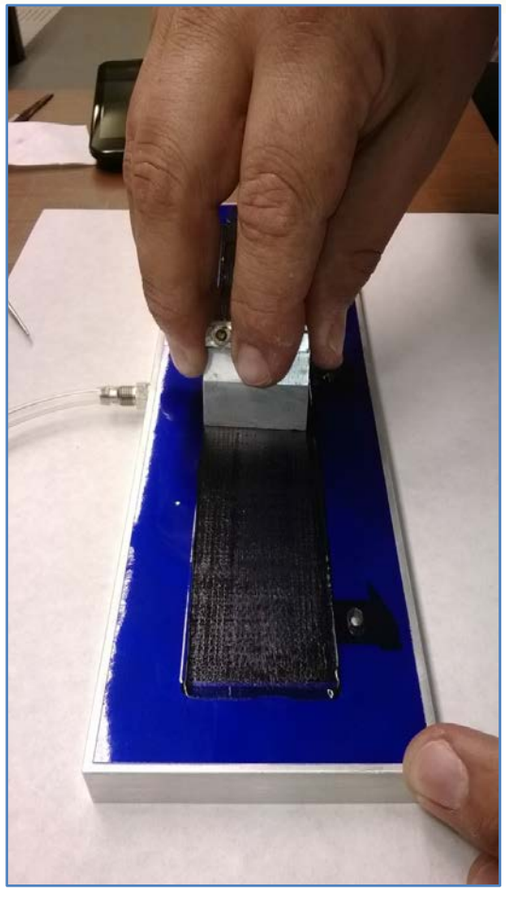
Optimisation for mechanical strength and to prevent chip pads contamination and spilling through the vias.

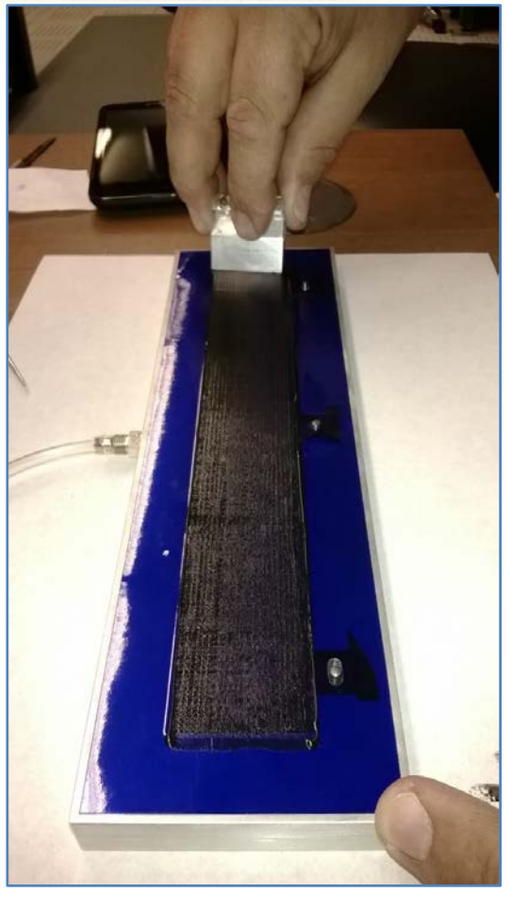




HIC Assembly

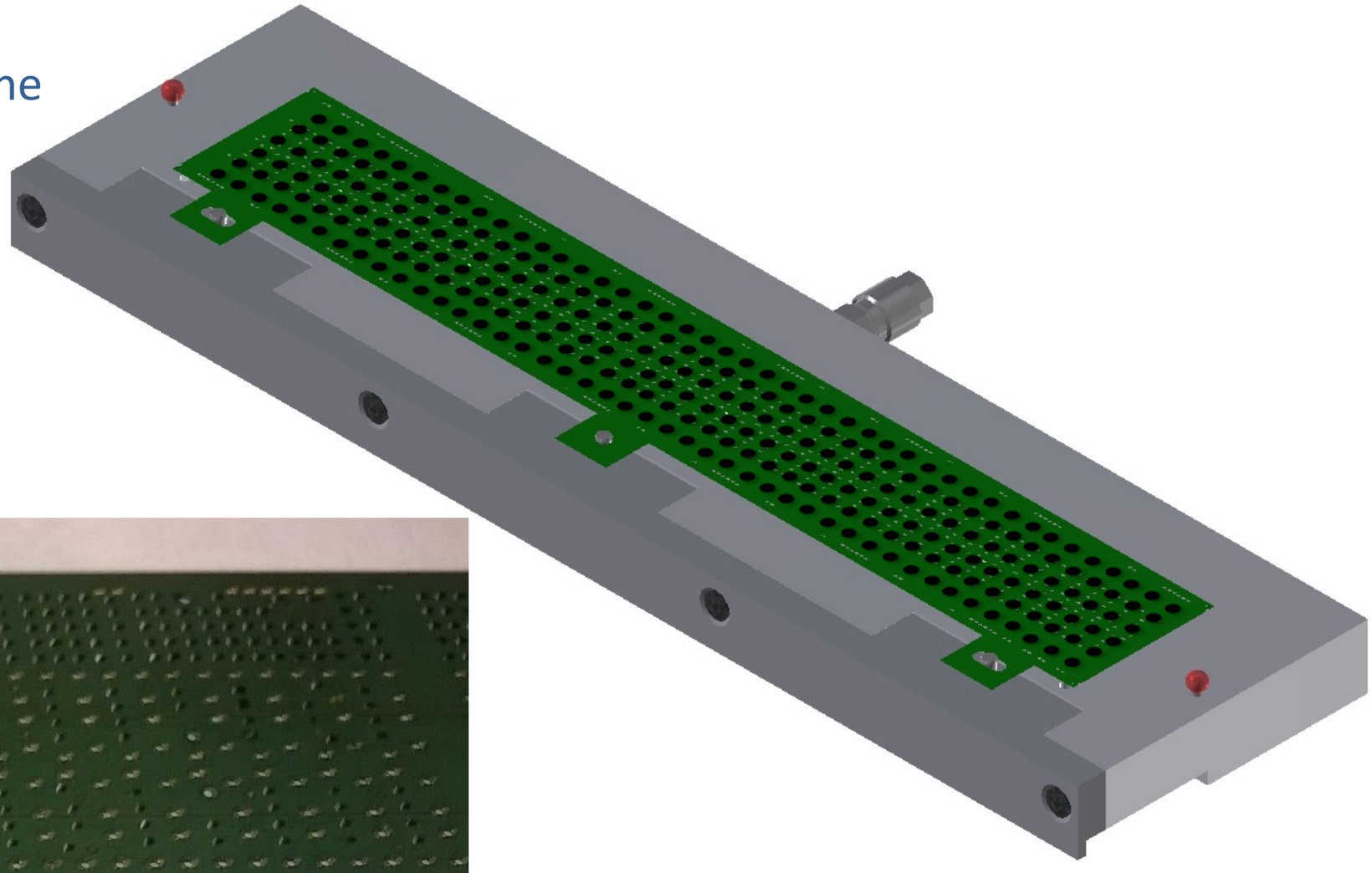
The glue is dispensed and sputtered above the mask

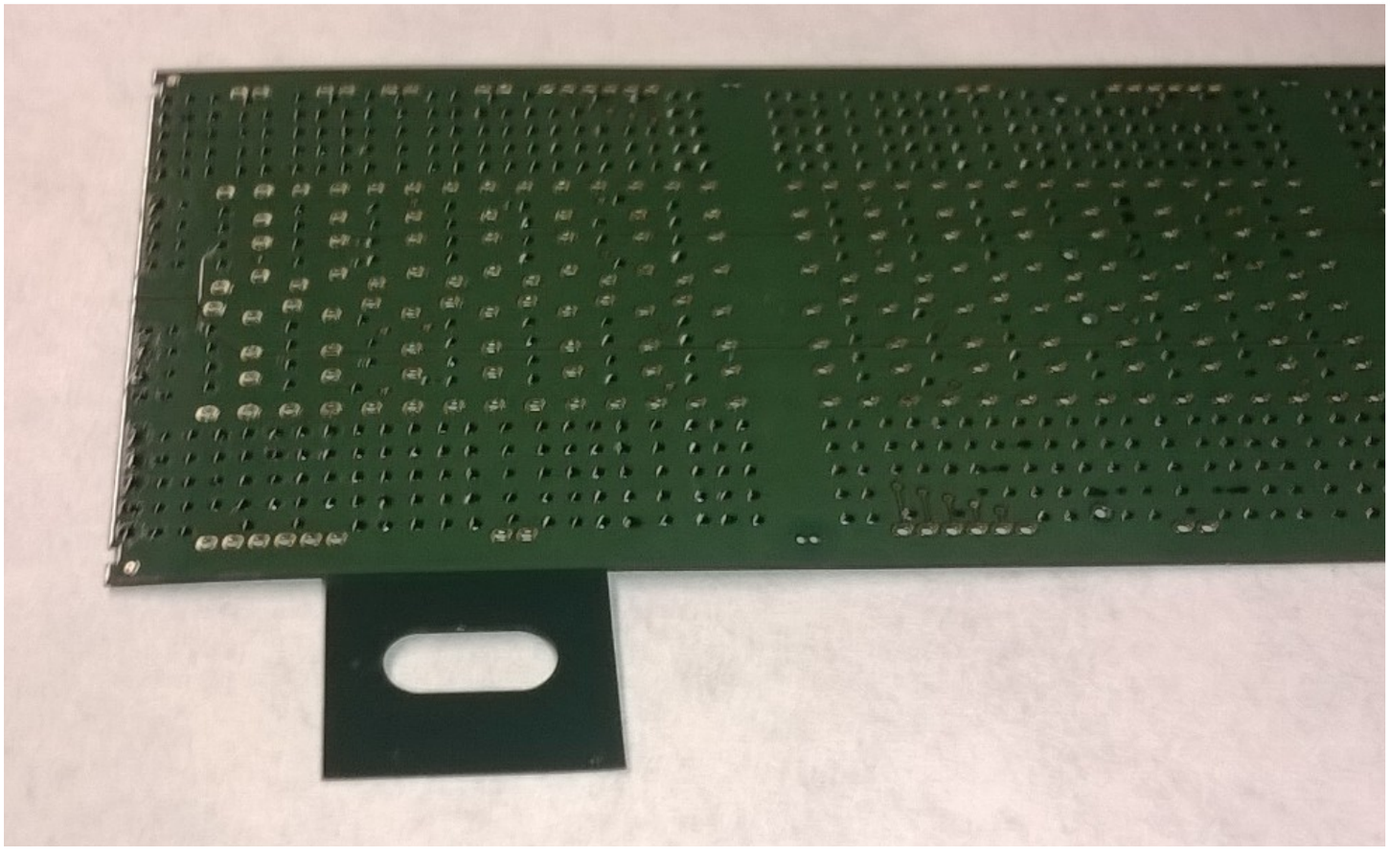




HIC Assembly

The mask/stencil is removed and the pattern of glue is checked

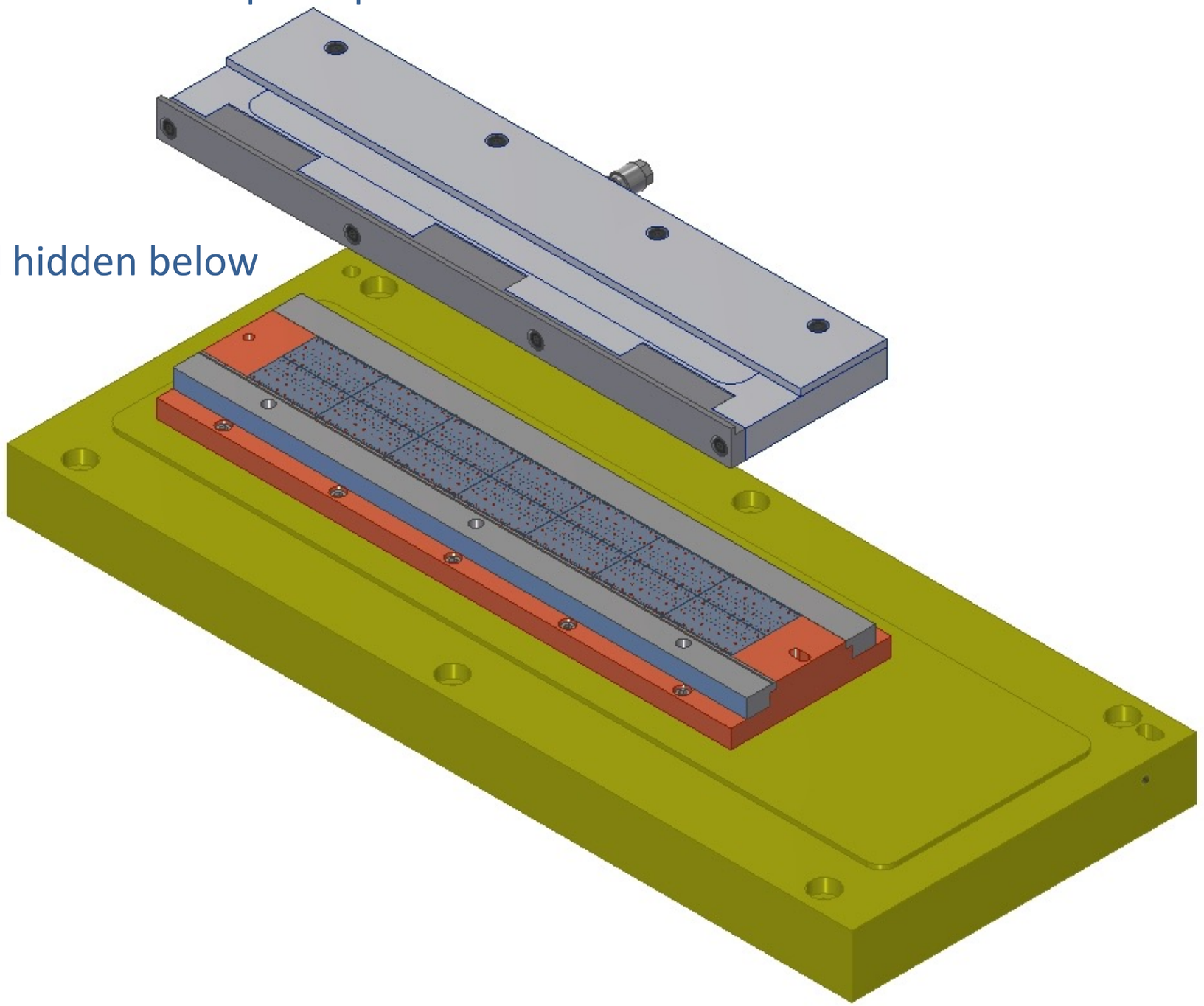




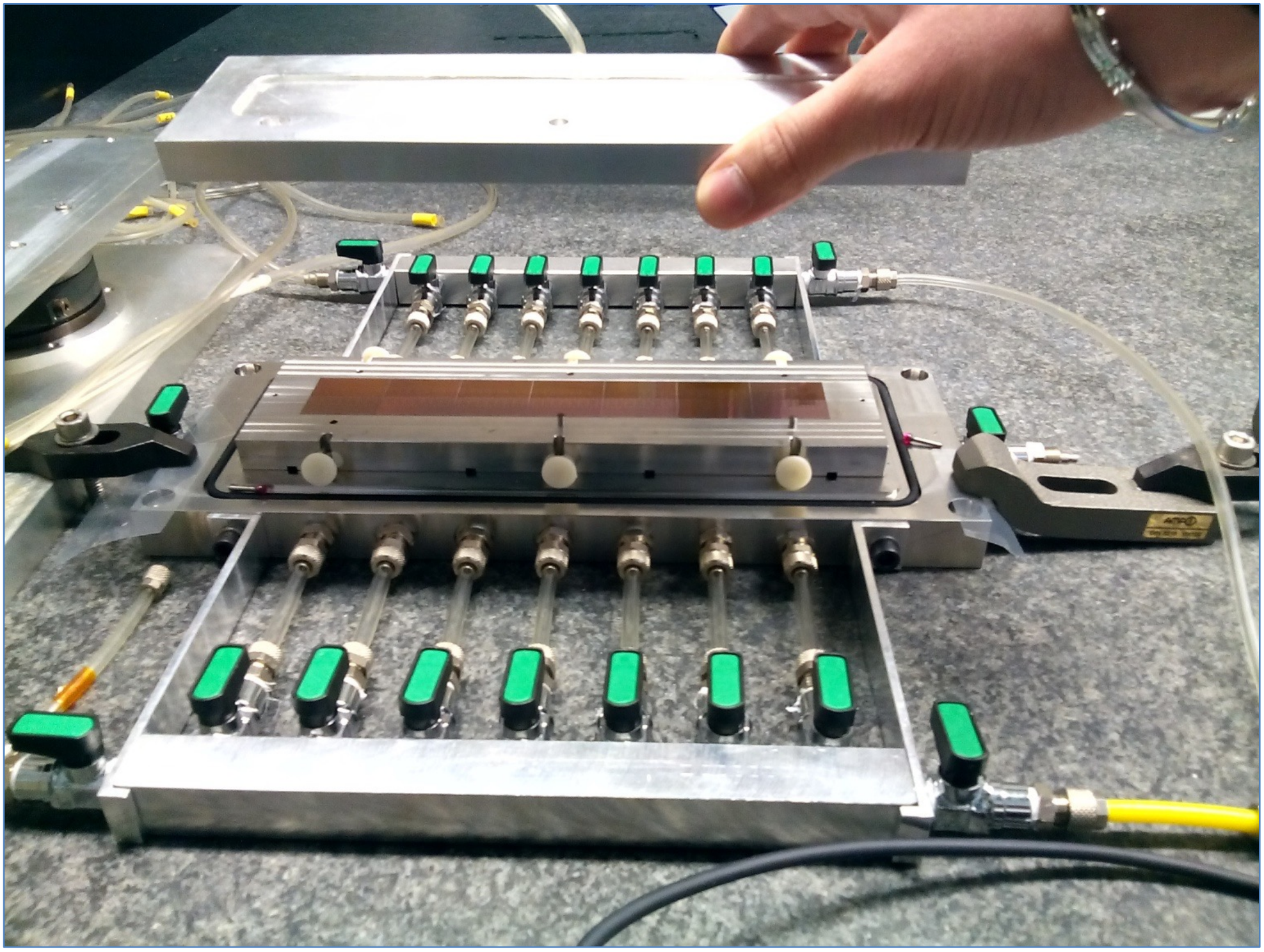
HIC Assembly

Placement of the FPC attached to the pick-up tool onto the chip array

FPC held by vacuum and hidden below the FPC pick-up tool



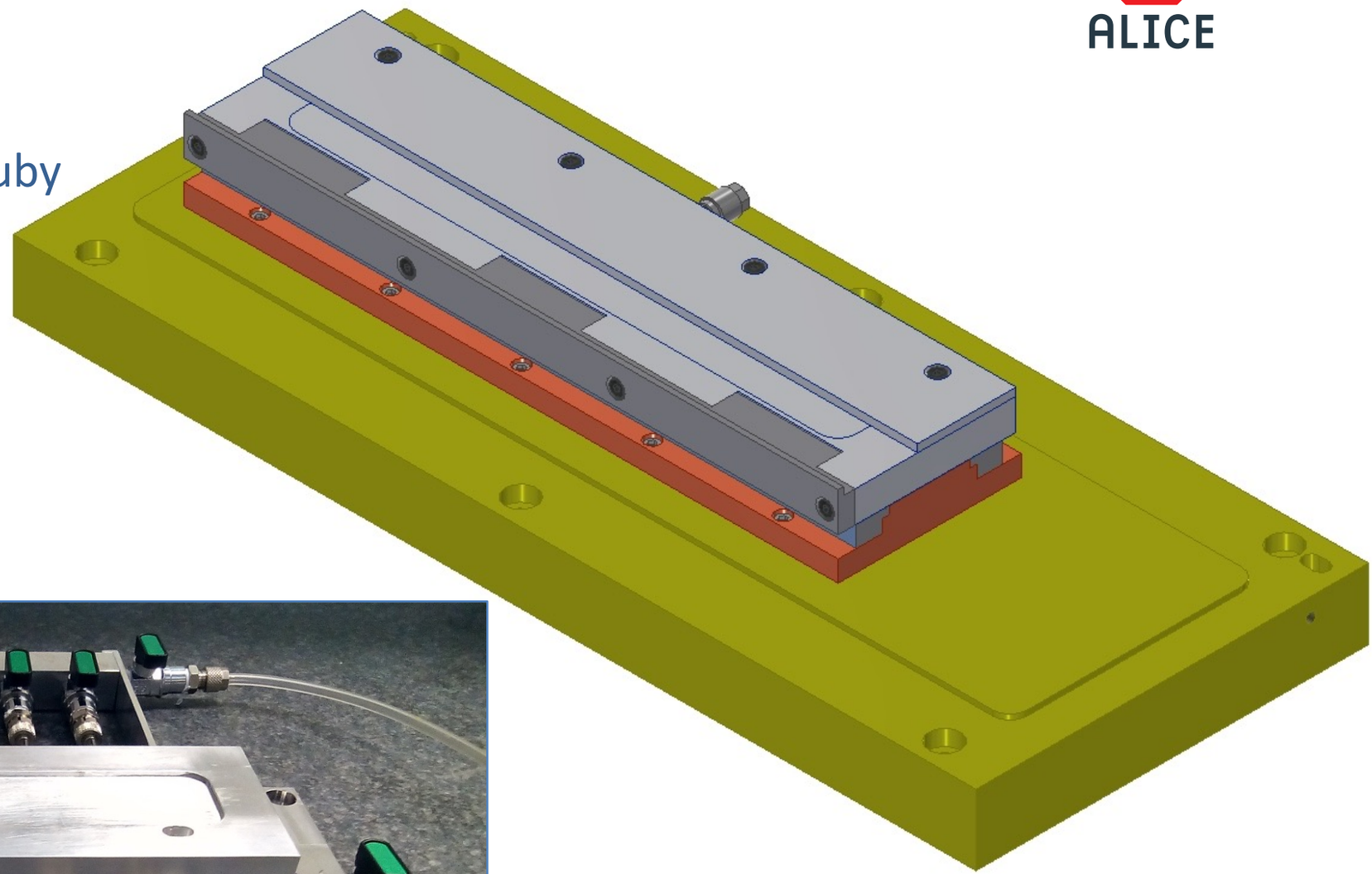
HIC Assembly

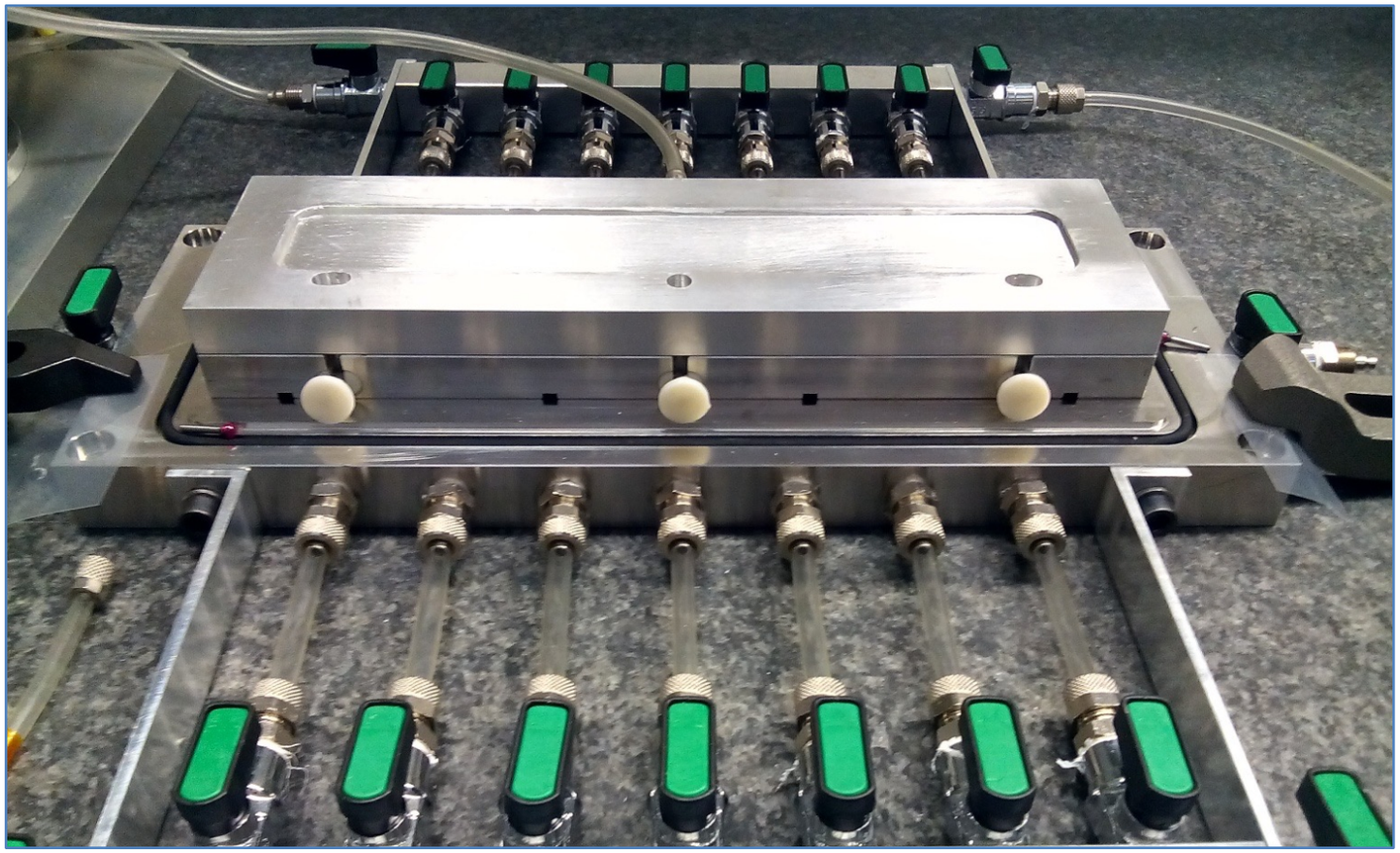


HIC Assembly

Relative alignment ensured by ruby spheres

Release vacuum from the FPC pick-up tool, which is kept in place till complete glue curing



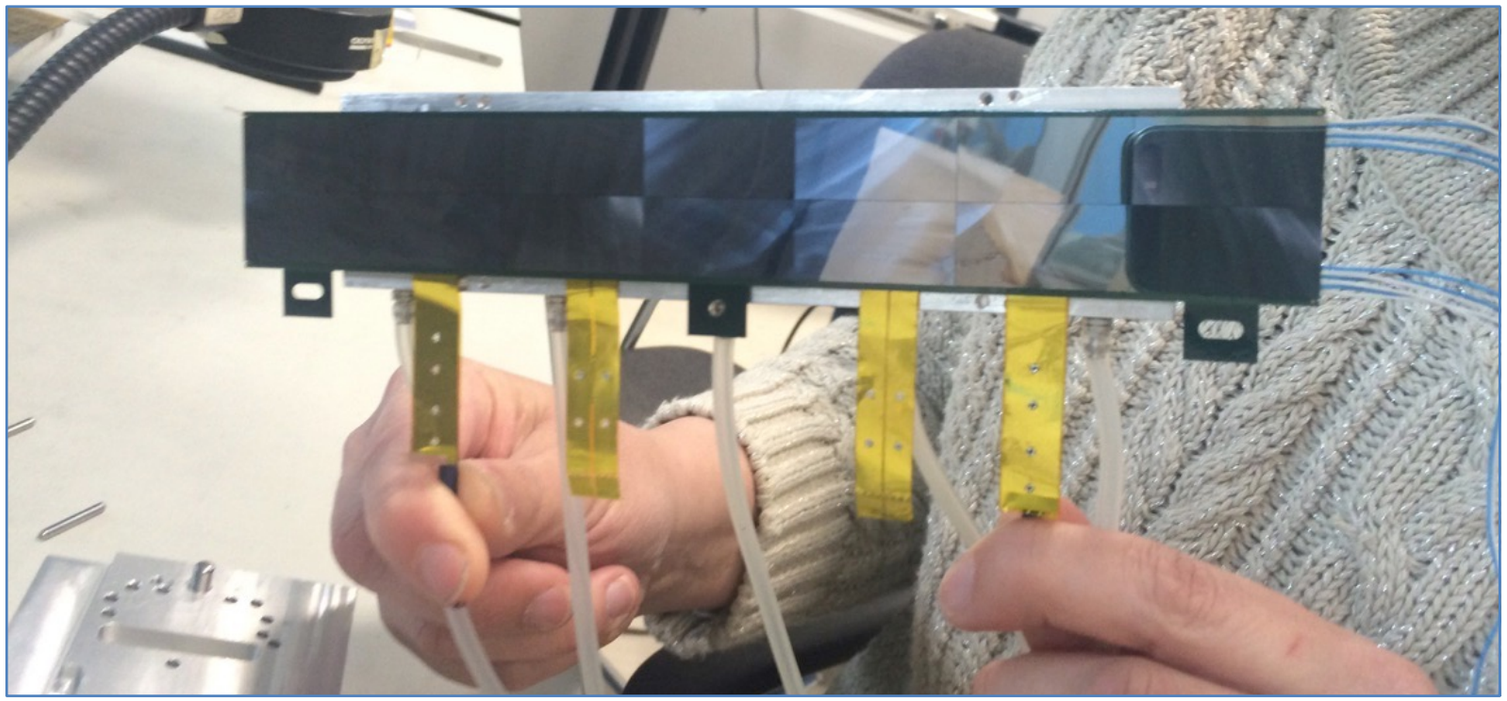


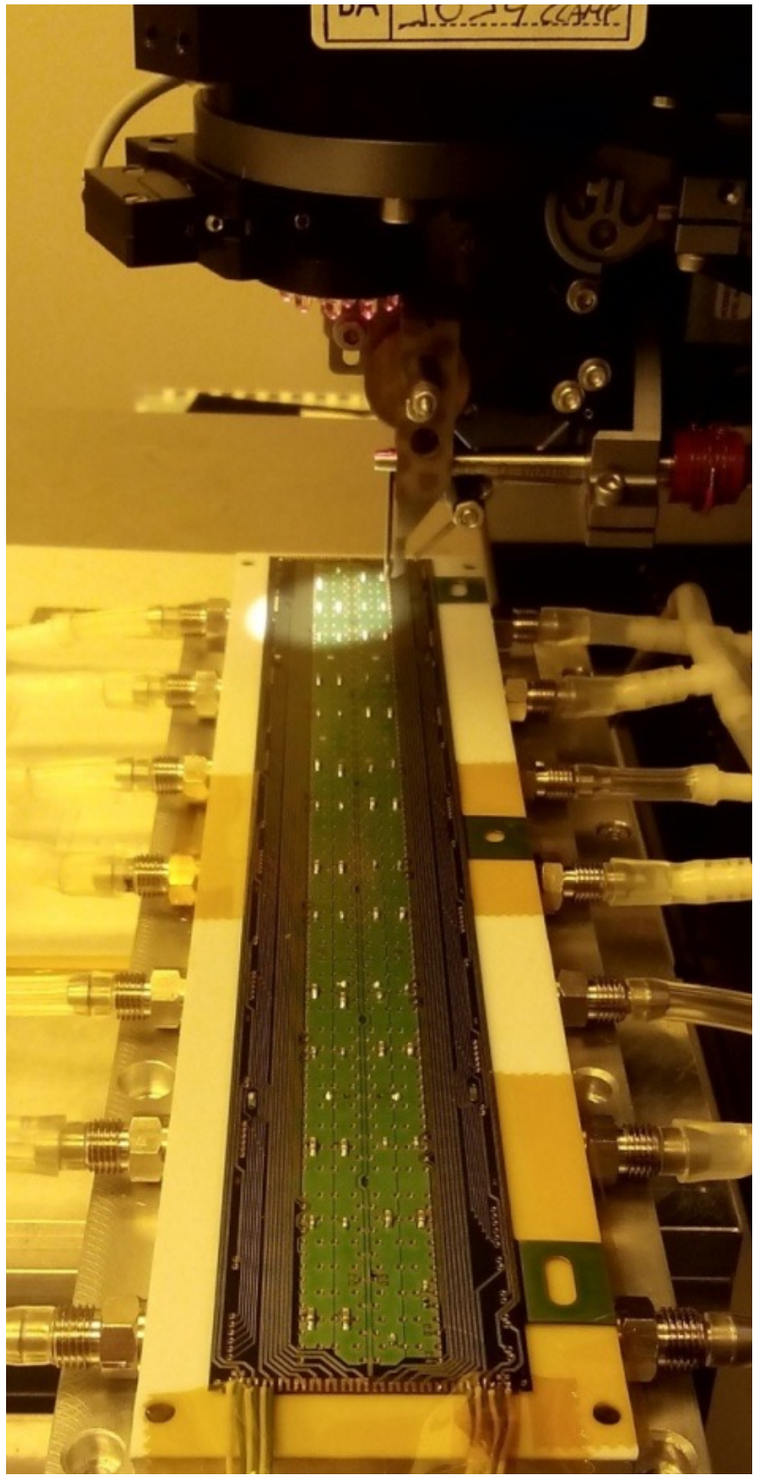
HIC Assembly

The flip-chip bonding is achieved by ultrasonic wedge bonding using a 25 µm aluminum wire through the vias of the FPC.

The connection is established between the pad over the chip and the metalized crown surrounding the vias

Improved hole layout for redundant bonds (≥2) and eventually re-working



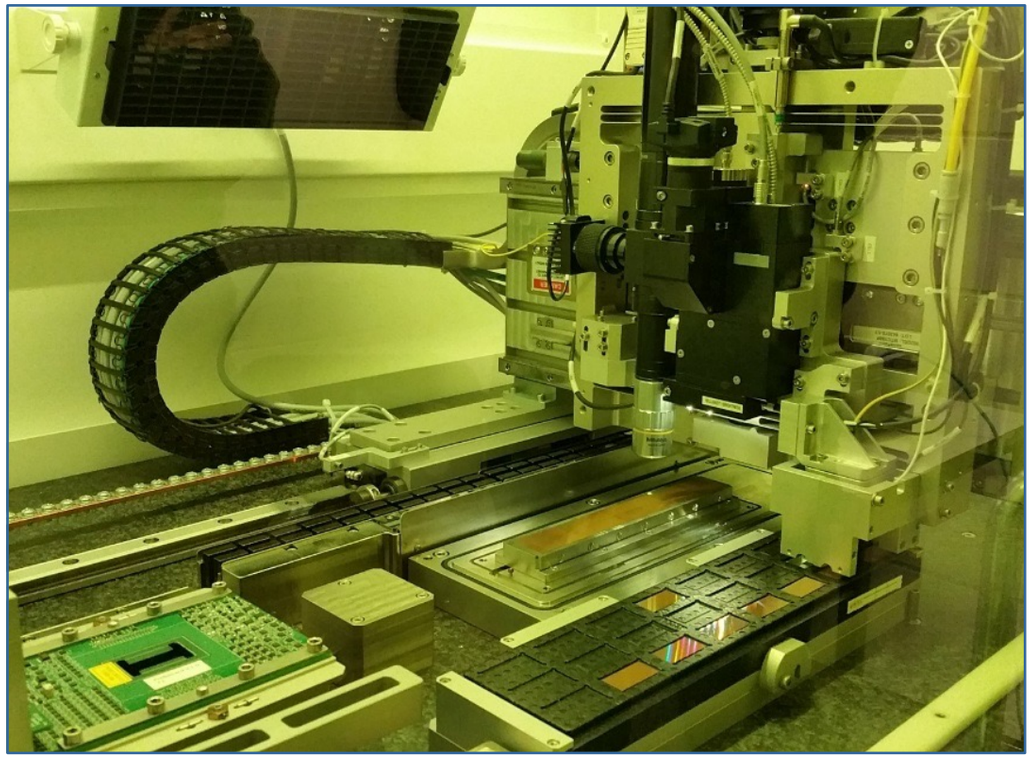


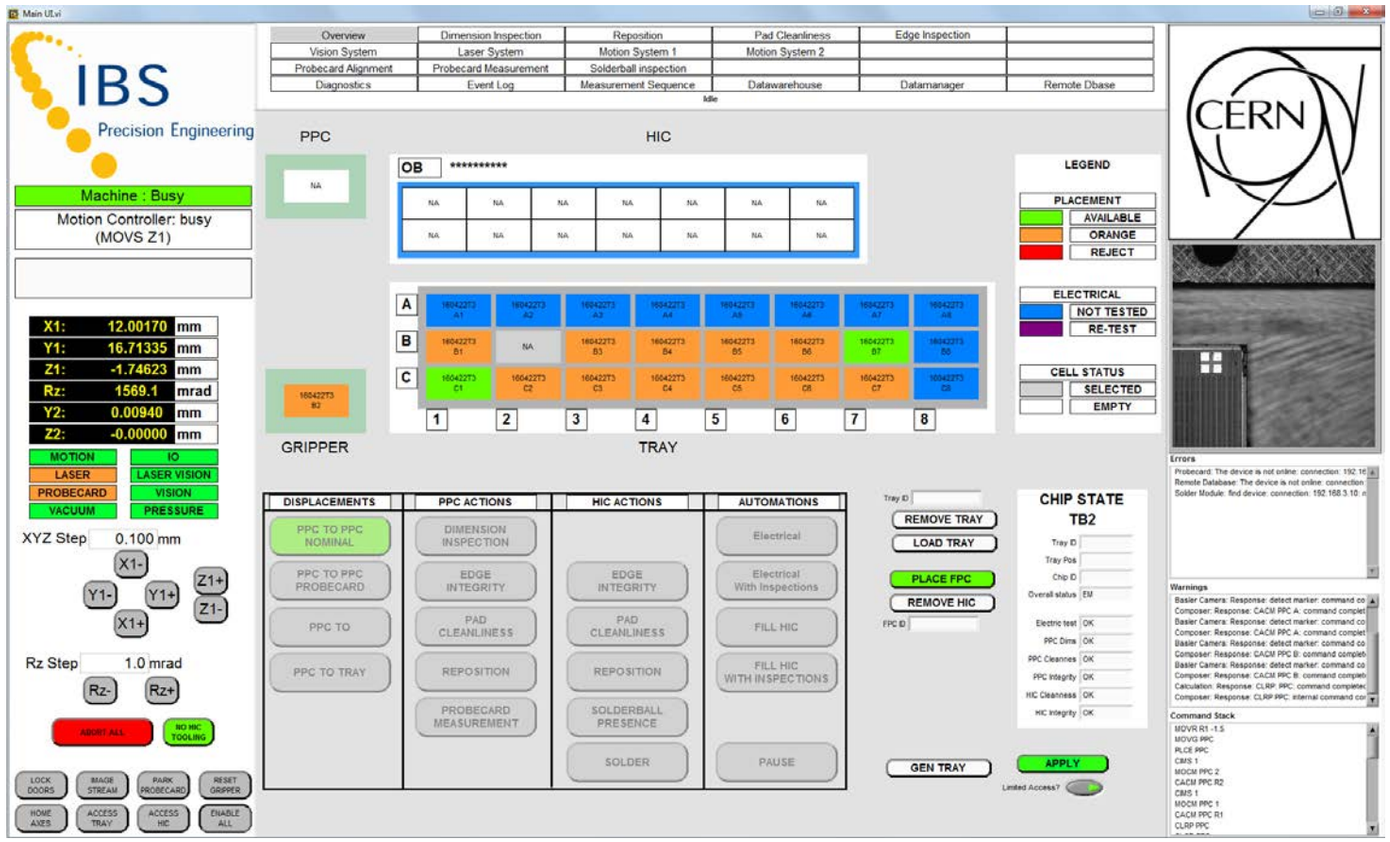
Module Assembly Machine

Module Assembly Machine

Timing (time per chip):

- Chip placement on pre-position chuck and probe card alignment : ~ 1.4’
- Chip AOI (edge integrity + pad cleanliness) : ~ 4’
- Chip pick-up from tray and alignment on assembly table: ~ 2.5’





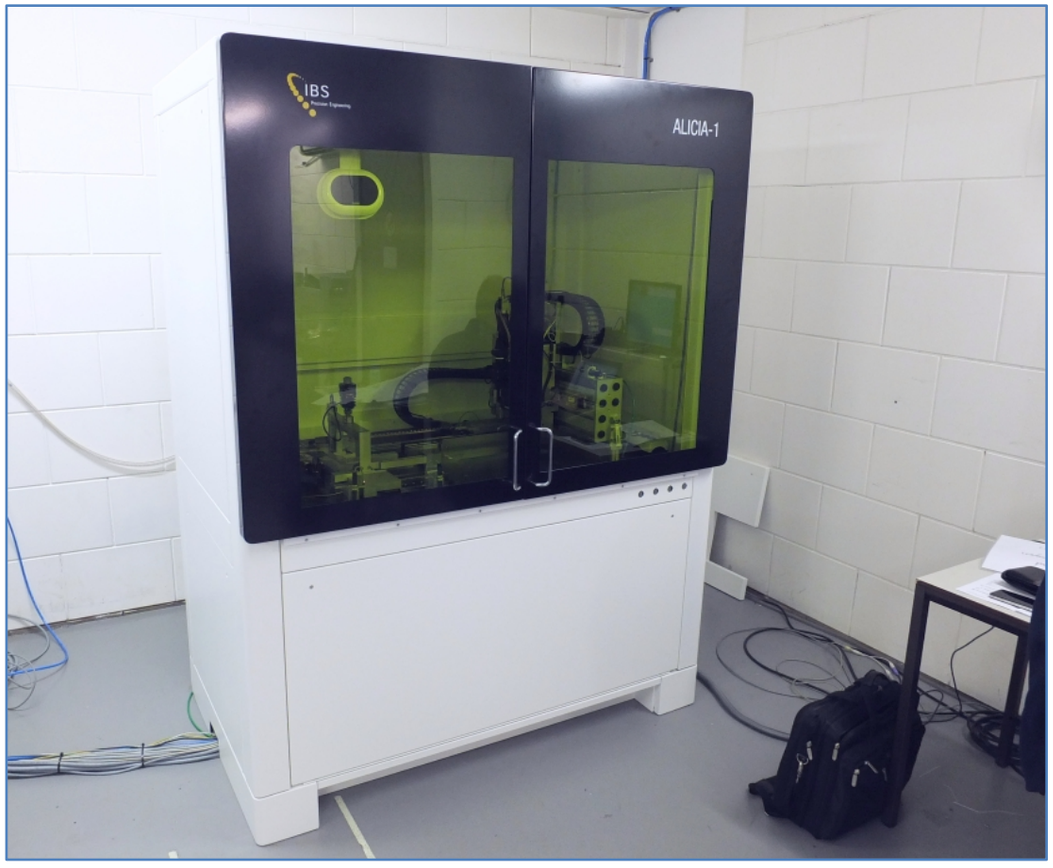
Prototype SAT date Wk 21

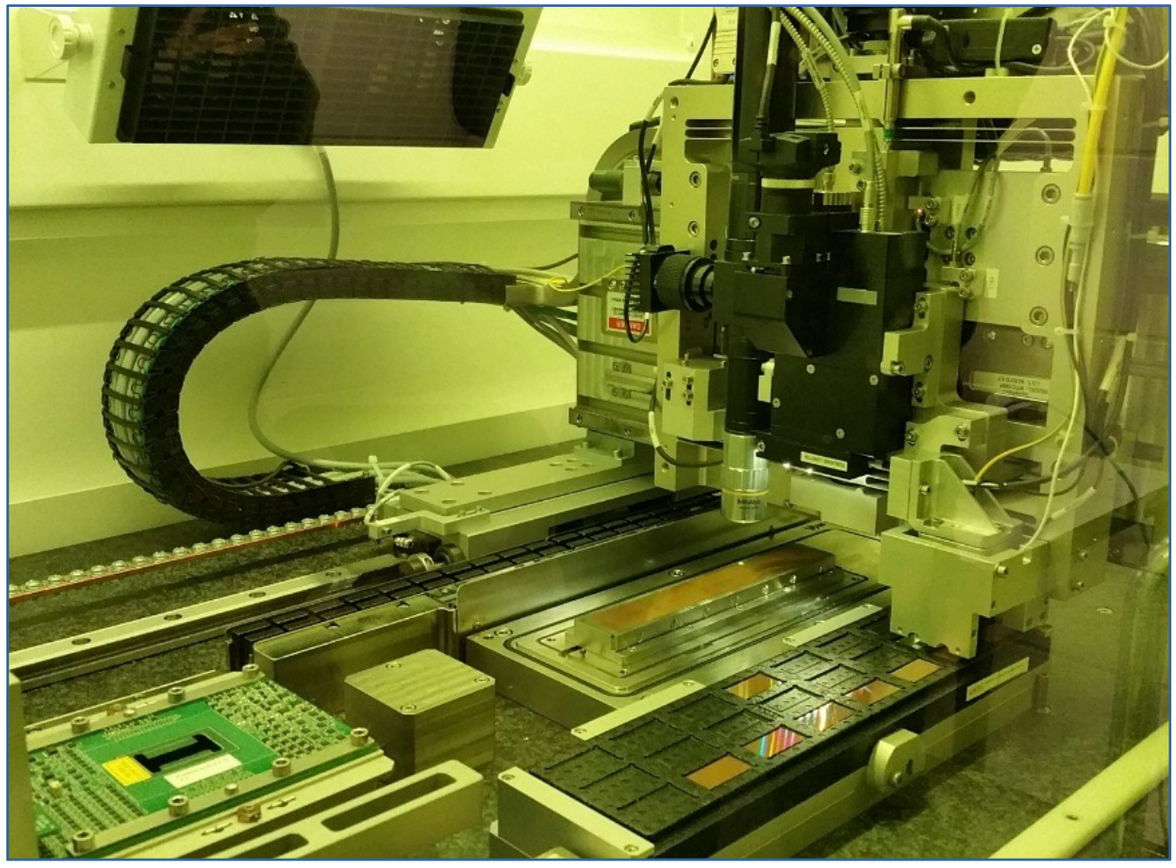
- delivery on Tue 24/05
- SAT on 26-27/05

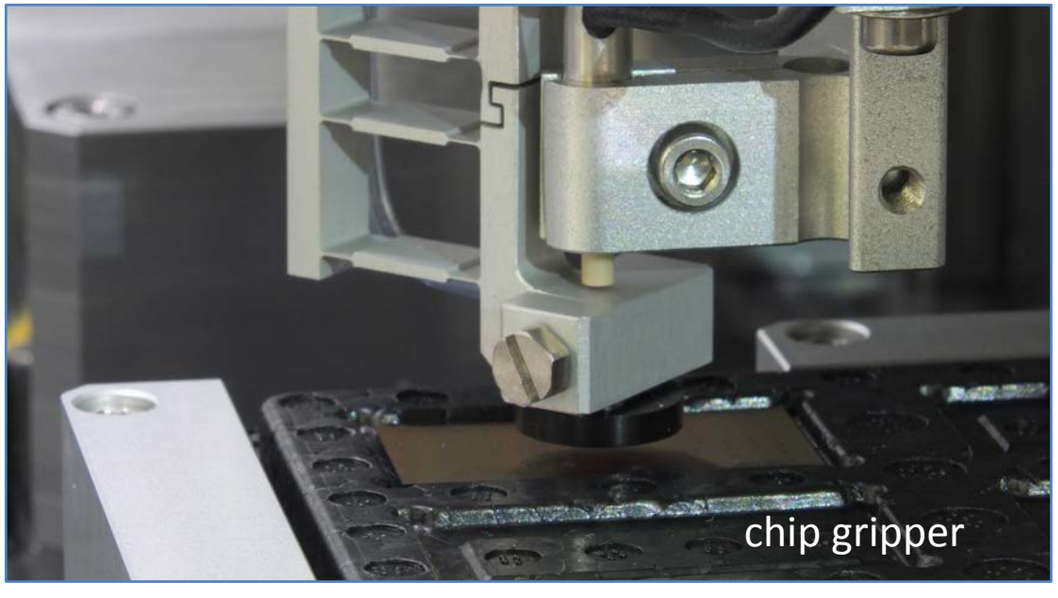
Delivery of series machine

1) Pusan Wk 46
2) Bari Wk 48
3) Liverpool Wk 50
4) Strasbourg Wk 2
5) Wuhan Wk 4

Module Assembly Machine



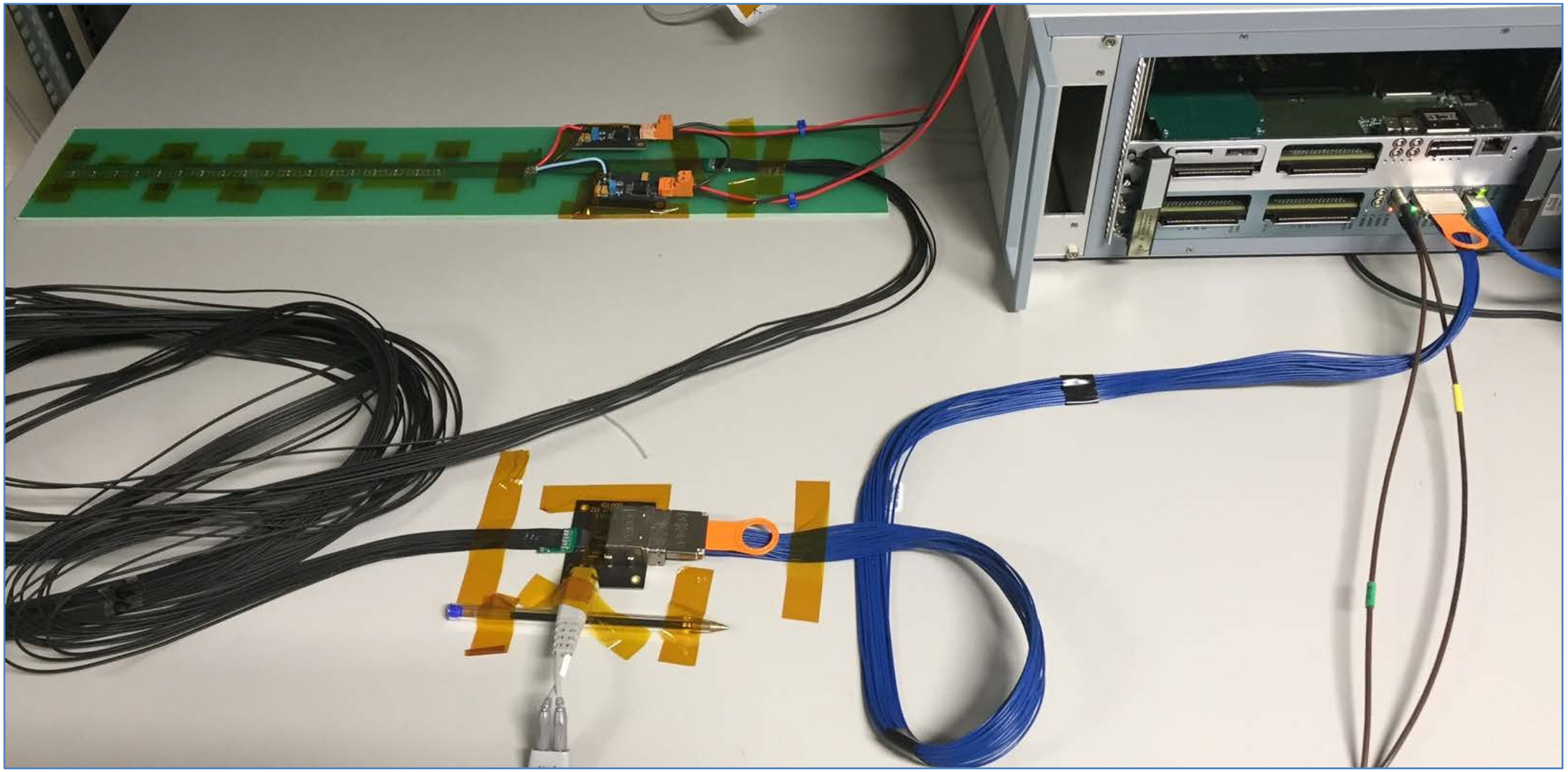




ALICE

HIC Testing

IB HIC Test Setup

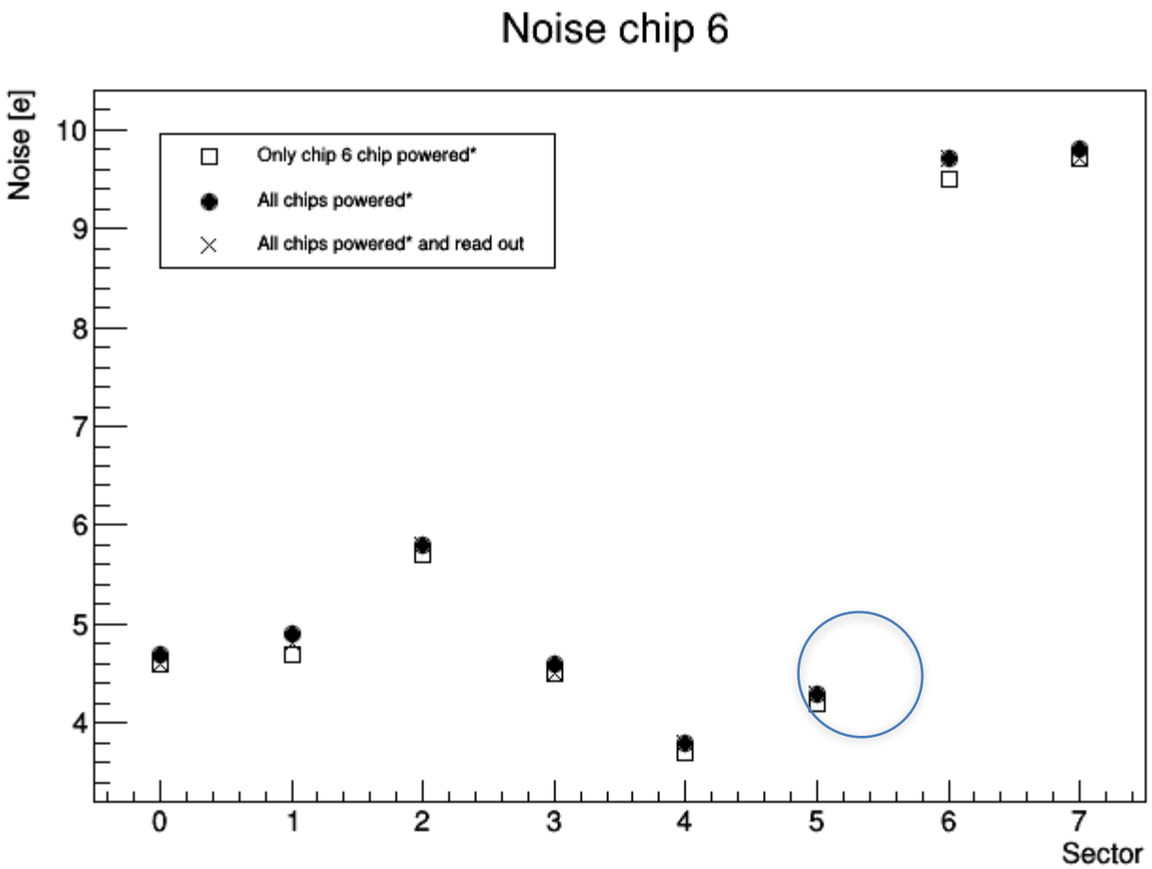


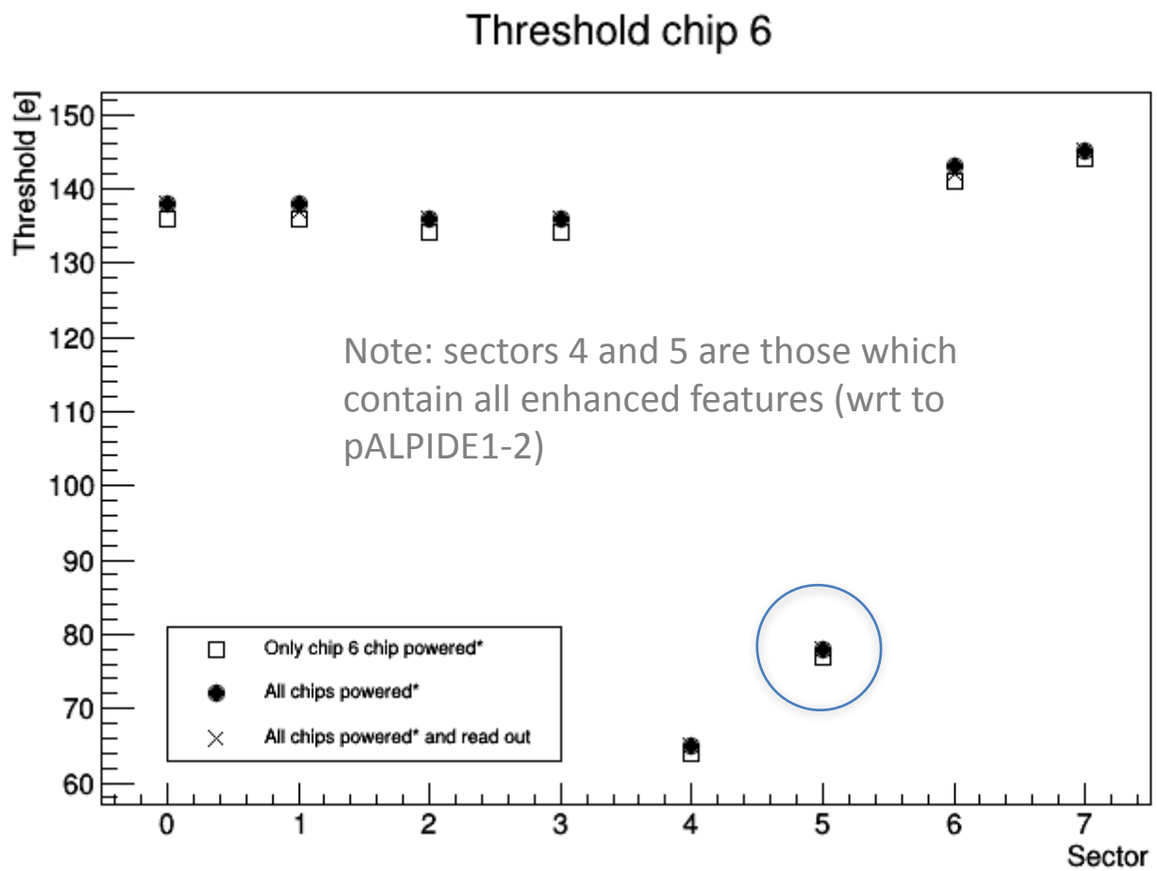
- HIC connected to MOSAIC test / readout card via 5m firefly cable + adapter card + 1 m Eyespeed cables
- Analogue and digital supply voltages provided by regulators close to the HIC
- Connection of regulators to supply planes by cables, significantly worse than in final layout.

IB HIC Test Results — Thresholds and Noise

Threshold scan results for one chip under three different conditions:

- All chips read out concurrently
- All chips powered, but only one chip read out
- Only one chip read out and analogue bias of other chips switched off, reducing analogue current consumption from 80 – 90 mA to 12 mA

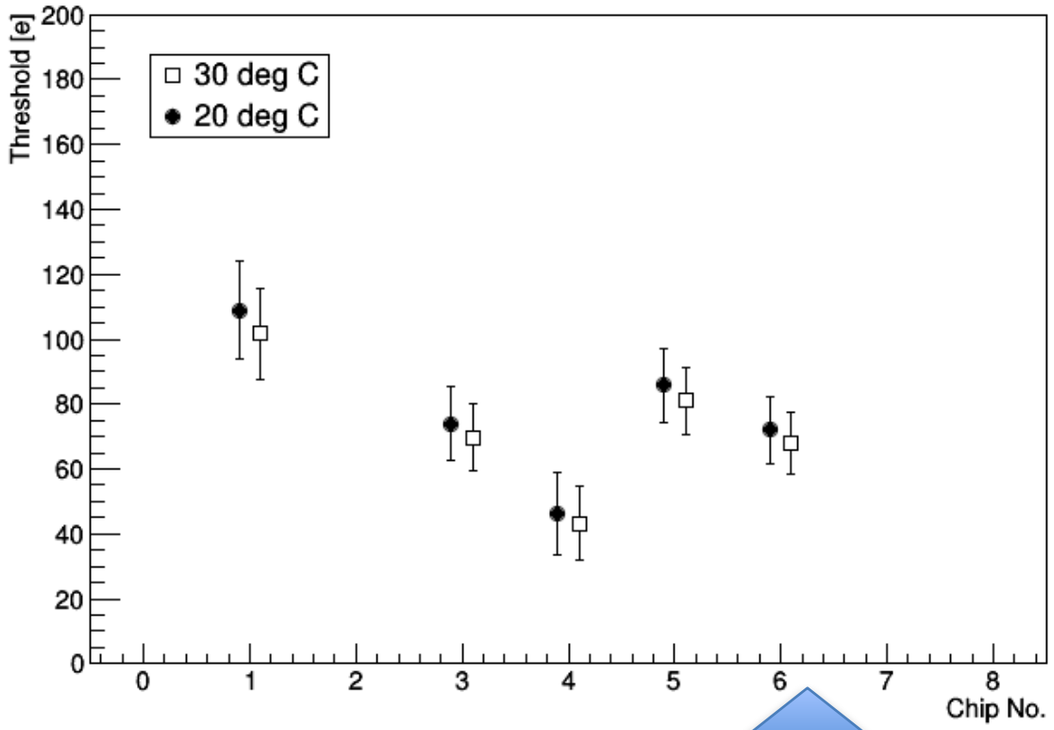


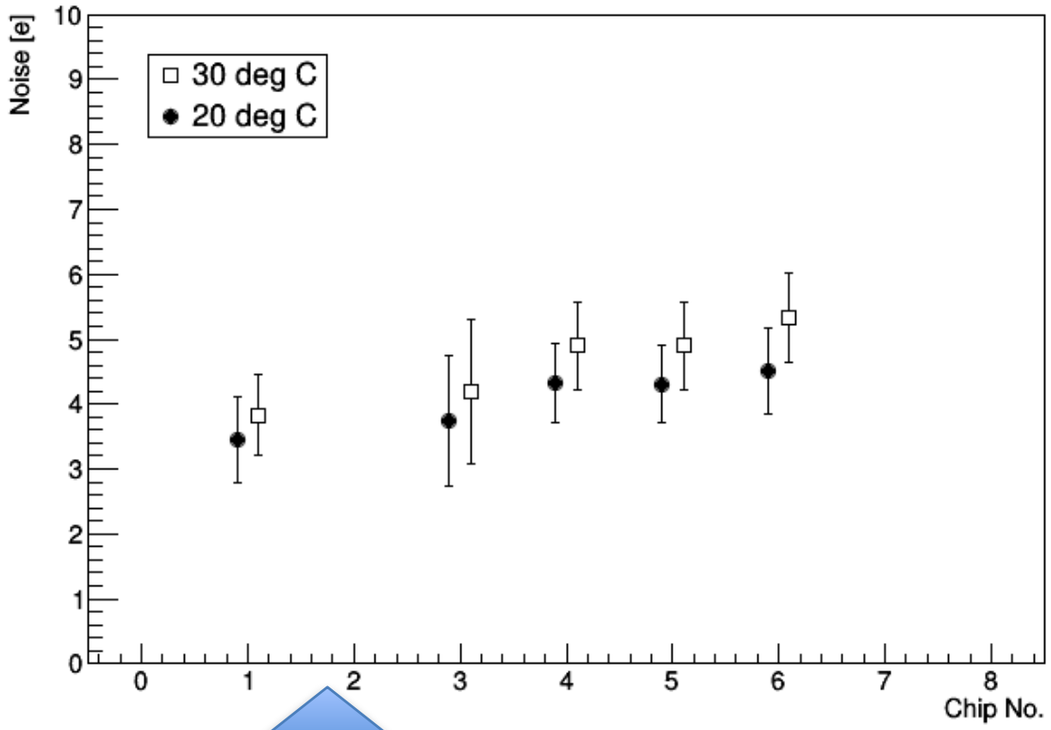


Both threshold and noise show now measurable difference between the three conditions

IB Stave - Characterisation

Threshold and Noise extracted from S-curve scan for two different coolant temperatures





Slight decrease of threshold with increasing temperature, and slight increase of noise (< 1e), as observed on single chips