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The prototype of 6-bit SAR ADC for SOI pixel detector readout

Silicon-On-Insulator (SOI) technology uses an insulator layer in a standard silicon substrate CMOS structure. The reduction of parasitic capacitances to substrate increases the speed of a circuits and decreases theirs power consumption. Moreover, there is a possibility to design monolithic detectors with sensor matrix and electronic integrated on a single wafer. These features make the SOI technology a good candidate for particles detector readout systems. In this work the design and preliminary measurements of 6- bit SAR ADC is presented. The ADC was designed in 200 nm Lapis SOI and is dedicated for column readout of SOI pixel detectors developed in this technology. The first measurements show that correct operation and the ADC achieves ENOB of about 5 bits at 7~MHz of sampling frequency. The measured power consumption is about 300μW.

Summary

The SOI technology is a promising candidate for future high energy physic detector systems because of the possibility for monolithic pixel detector design. Moreover, the Burried-Oxide (BOX) layer in the SOI structure helps to reduce the power consumption of the electronic circuits and increase their speed. The additional advantages is latch-up effects elimination and significant reduction of Single Event Upsets (SEU). The proposed Analog-to-Digital Converter (ADC) is a sub-part of a complex pixel detector matrix with dedicated readout electronics, being developed by the authors of this work in 200nm Lapis Fully-Depleted, Low-Leakage SOI technology.

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The Successive Approximation Register (SAR) architecture provides a good conversion speed in relation to c

In order to test the behavior of different transistors available in 200nm Lapis SOI, three different varia

First measurements show that all prototypes are fully functional and there is no meaningful difference in
The presented ADC has been implemented as column ADC and fabricated in a prototype monolithic pixel detect
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