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Readout electronics for LGAD sensors

Low Gain Avalanche Detectors (LGAD) represent a remarkable advance in high energy particle detection, since they provide a moderate increase (gain ~10) of the collected charge, thus leading to a notable improvement of the signal-to-noise ratio, which largely extends the possible application of Silicon detectors beyond their present working field. The optimum detection performance requires a careful implementation of the multiplication junction, in order to obtain the desired gain on the read out signal, but also a proper design of the edge termination and the peripheral region, which prevents the LGAD detectors from premature breakdown and large leakage current.

The Low Gain Avalanche Detector (LGAD) is based on the standard Avalanche Photo Diodes (APD) concept, commonly used in optical and X-ray detection applications, including an internal multiplication of the charge generated by radiation. The multiplication is inherent to the basic n++-p+-p structure, where the doping profile of the p+ layer is optimized to achieve high field and high impact ionization at the junction.

All avalanche diode detectors have a region with a high electrical field leading to multiplication of signal charges (electron and/or holes) flowing through this region. The gain mechanism is achieved within the semiconductor material by raising the electric field as high as necessary to enable the drifting electrons to create secondary ionization during the collection process. Normally, the junction consists of a thin and highly doped n-type layer on top of a moderately doped p-layer in which the multiplication (of electrons) takes place. A high resistivity p-type silicon substrate is typically used to produce detectors with a bulk that can be fully depleted.

Compared to standard APD detectors, LGAD (Low Gain Avalanche Detectors) structure exhibit moderate gain values. This is mandatory to obtain fine segmentation pitches in the fabrication of microstrip and pixel detectors, free from the limitations commonly found in avalanche detectors. In addition, a moderate multiplication allows the fabrication of thinner sensors, with an output signal amplitude that is as large as that from thicker sensors without internal gain. The design of LGAD structure exploits the charge multiplication effect to obtain a silicon detector that can simultaneously measure precisely the position and time of arrival of incident particles.

The LGAD structures are optimized for applications such as tracking or timing detectors for high energy physics experiments or medical applications where time resolution lower than 30 ps is required.

In this paper, an ASIC fabricated in 180 nm CMOS technology from AMS with the very front-end electronics used to readout LGAD sensors is presented as well as its experimental results. The front-end has the typical architecture for Si-strip readout, i.e., preamplification stage with a Charge Sensitive Amplifier (CSA) followed by a CR-RC shaper. Both amplifiers are based on a folded cascade structure with a PMOS input transistor and the shaper only uses passive elements for the feedback stage and the shaping time is fixed at 1 us. The CSA has programmable gain and a configurable input stage in order to adapt to the LGAD sensors. The fabricated prototype is 0.865 mm x 0.965 mm and includes the biasing circuit for the CSA and the shaper, 4 analog channels (CSA+shaper) and programmable charge injection circuits included for testing purposes. The power consumption is 150 uW per channel.

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