Operational Experience with the ATLAS Pixel detector

Kerstin Lantzsch (Universität Bonn)
on behalf of the ATLAS Collaboration

Pixel 2016, Sestri Levante, 05.09.2016

Outline

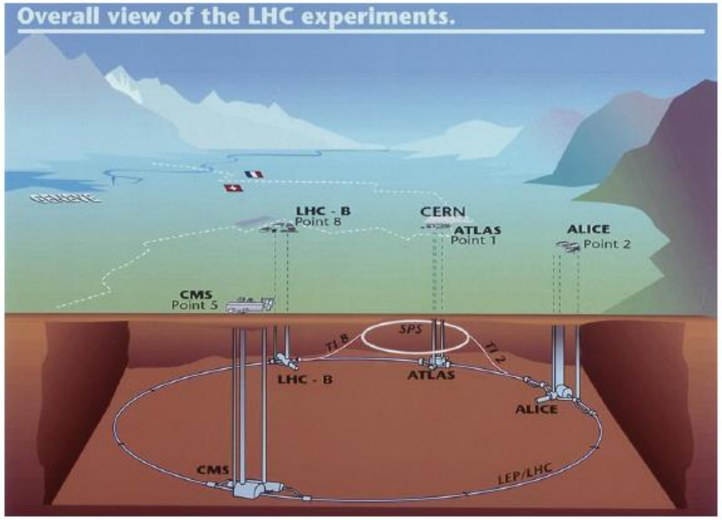
- ATLAS Pixel Detector
  - LHC performance and roadmap
  - Detector parameters and upgrades
- Operations
  - Intrinsic limitations
  - Operational challenges
- Performance
- Outlook

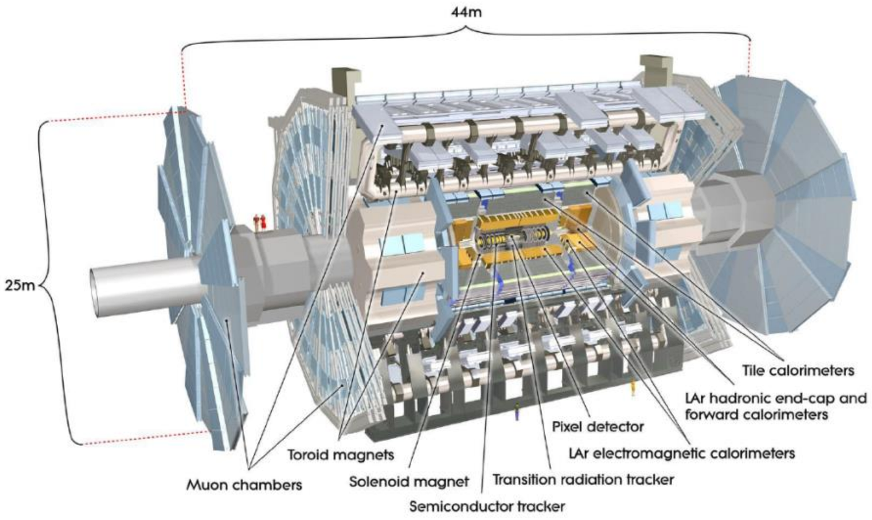
LHC – Large Hadron Collider

design vs. 2016 conditions

- 7 TeV nominal beam energy (6.5 TeV)
- $1x10^{34}$ cm^{-2} s^{-1} nominal luminosity ($1.2x10^{34}$ cm^{-2} s^{-1})
- 2808 proton bunches per beam (2220b)
- 25 ns bunch spacing/40 Mhz

- First Long Shutdown (LS1) 2013/14 with repairs and upgrades to the accelerator and the experiments



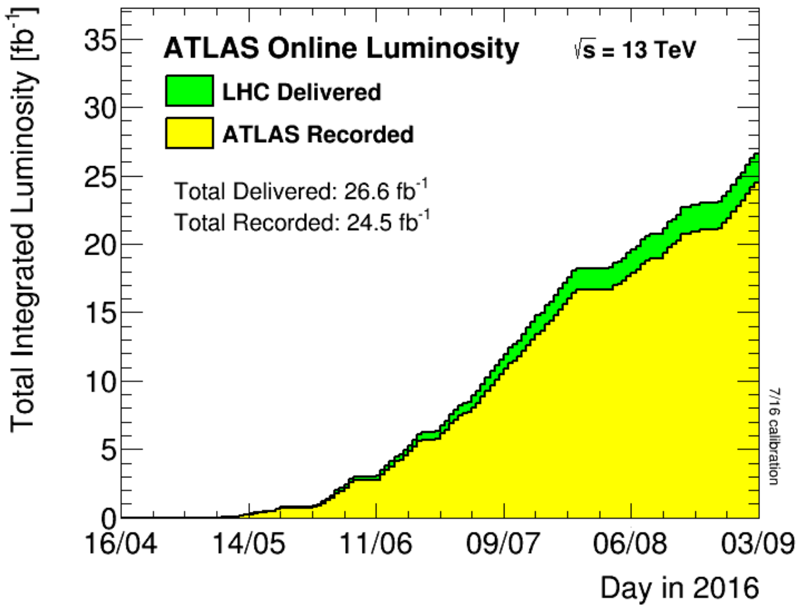


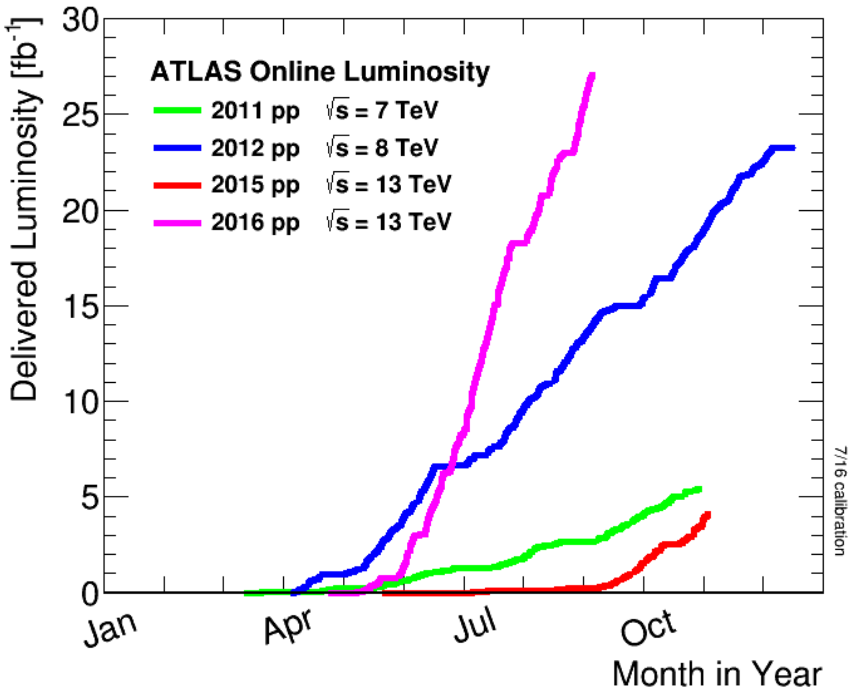
ATLAS

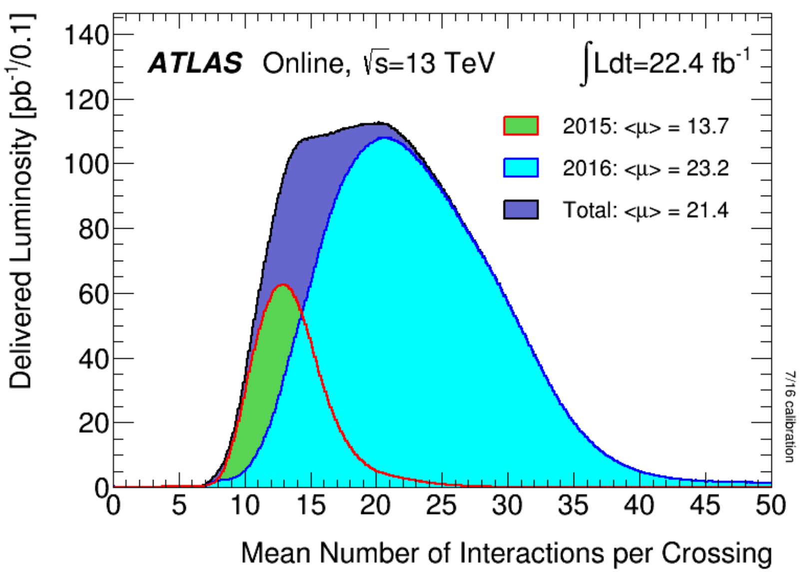
Multi-purpose detector designed to

- Investigate the TeV scale
- Search for the Higgs boson
- Search beyond the standard model
  - Supersymmetry, Mini-black holes, Leptoquarks, Extradimensions
- Make precision measurements of SM

LHC & ATLAS performance 2016

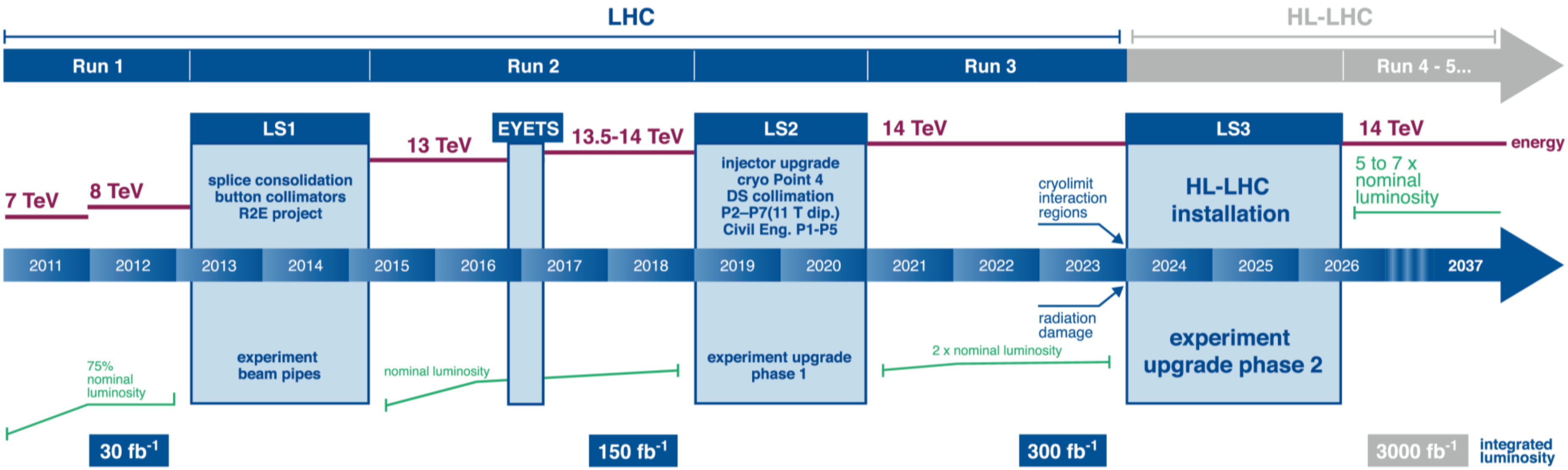




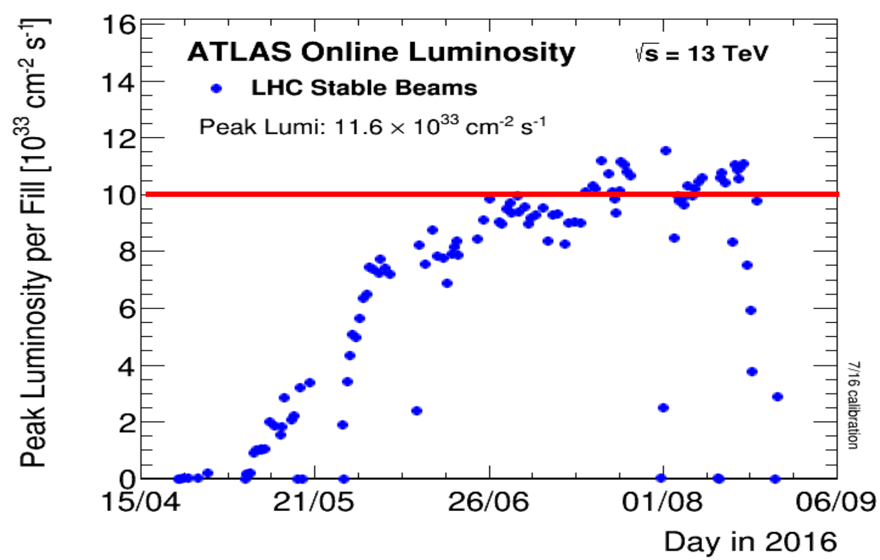


ATLAS pp 25ns run: April-July 2016										
Inner Tracker			Calorimeters		Muon Spectrometer				Magnets	
Pixel	SCT	TRT	LAr	Tile	MDT	RPC	CSC	TGC	Solenoid	Toroid
98.9	99.9	100	99.8	100	99.6	99.8	99.8	99.8	99.7	93.5
Good for physics: 91-98% (10.1-10.7 fb^{-1})										

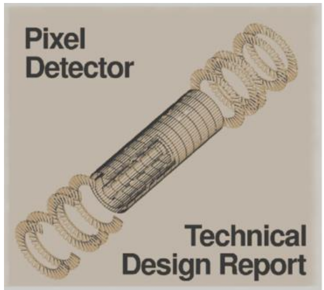
LHC roadmap

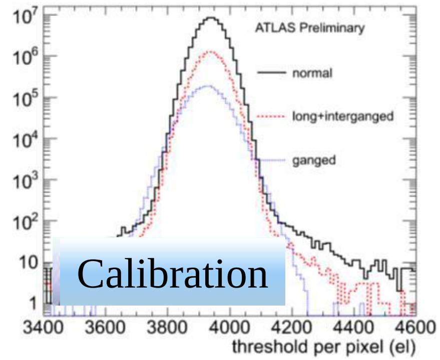


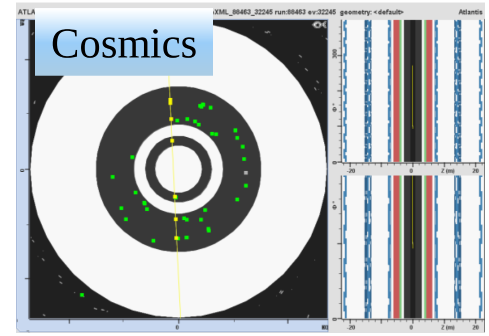
- Surpassed $1\text{x}10^{34}\text{cm}^{-2}\text{s}^{-1}$ in July 2016
- Expect to see $2\text{x}10^{34}\text{cm}^{-2}\text{s}^{-1}$ (and beyond?) during the lifetime of the Pixel Detector



Pixel Timeline

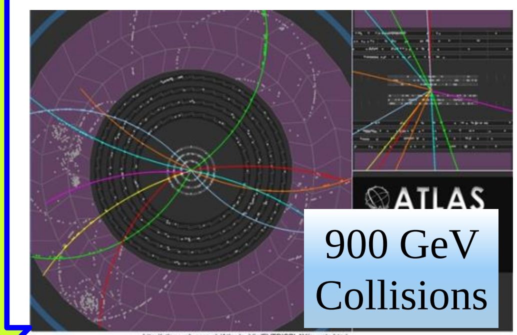




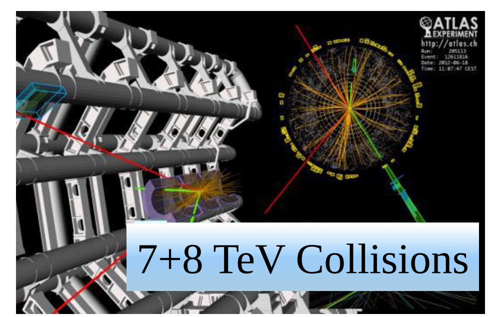


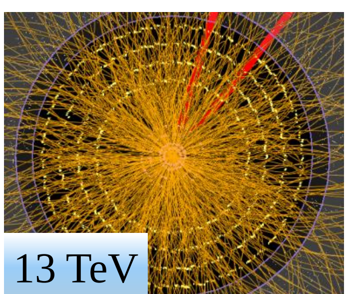
1998 → 2007 → 2008 → 2009 → 2010 → 2012 → 2013 → 2014 → 2015

RUN 1



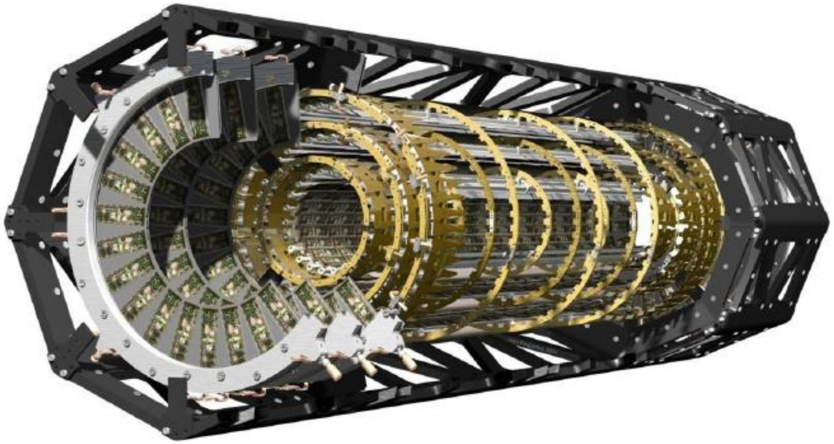
RUN 2

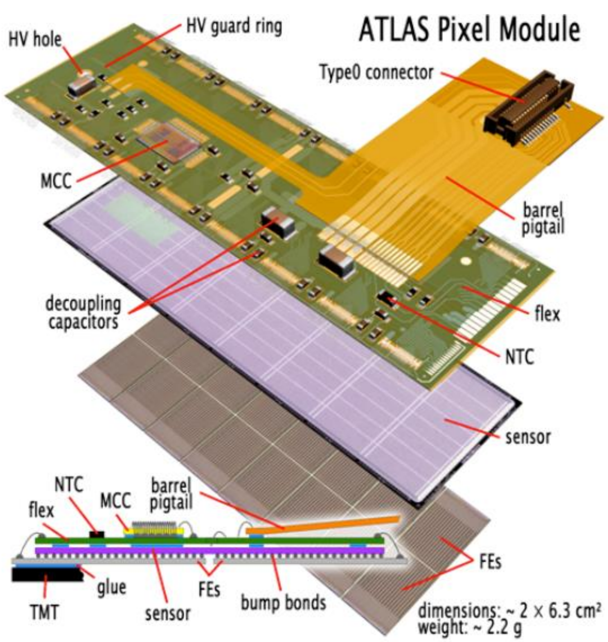




The ATLAS Pixel Detector – before LS1

- 3 hit-system for $|\eta| < 2.5$
  - 3 barrel layers
  - 3 disks per end-cap
- Resolution in r-ϕ < 15 µm
- 1744 modules, 80M readout channels
- Innermost barrel layer at 50.5 mm
- Radiation tolerance 500 kGy / 10^{15} 1MeV neq cm^{-2}
- Evaporative C_3F_8 cooling





Sensor

- 250 µm thick n-on-n sensor
- 47232 (328 x 144) pixels
- Typical pixel size 50 x 400 $µm^2$

Readout

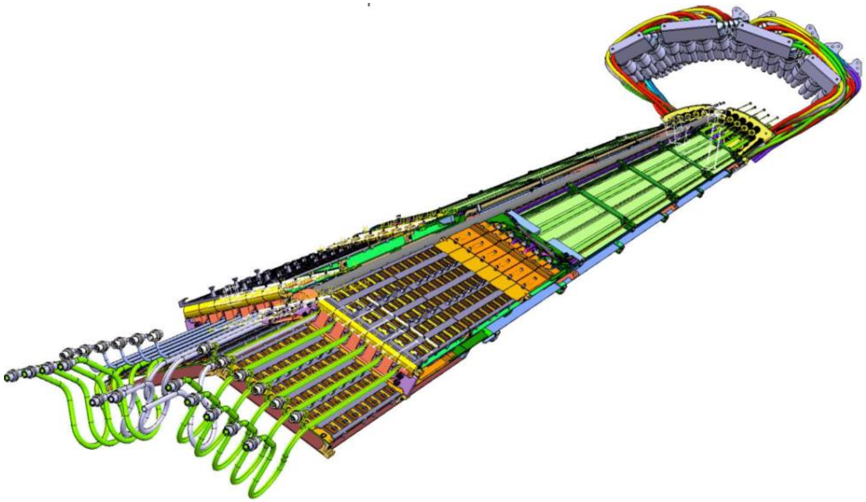
- 16 FE chips, 2880 pixels each
- Zero suppression in the FE chip, MCC builds module event
- Data transfer 40 – 160 MHz depending on layer

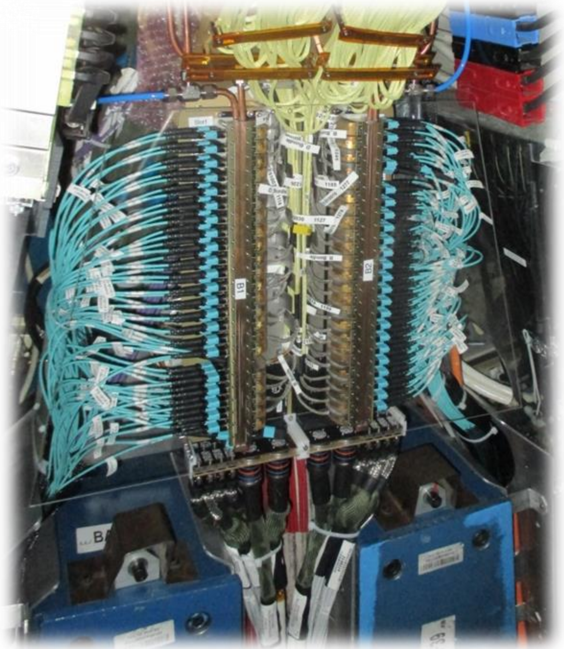
LS1 upgrades: nSQP

Pixel Detector extracted during LS1

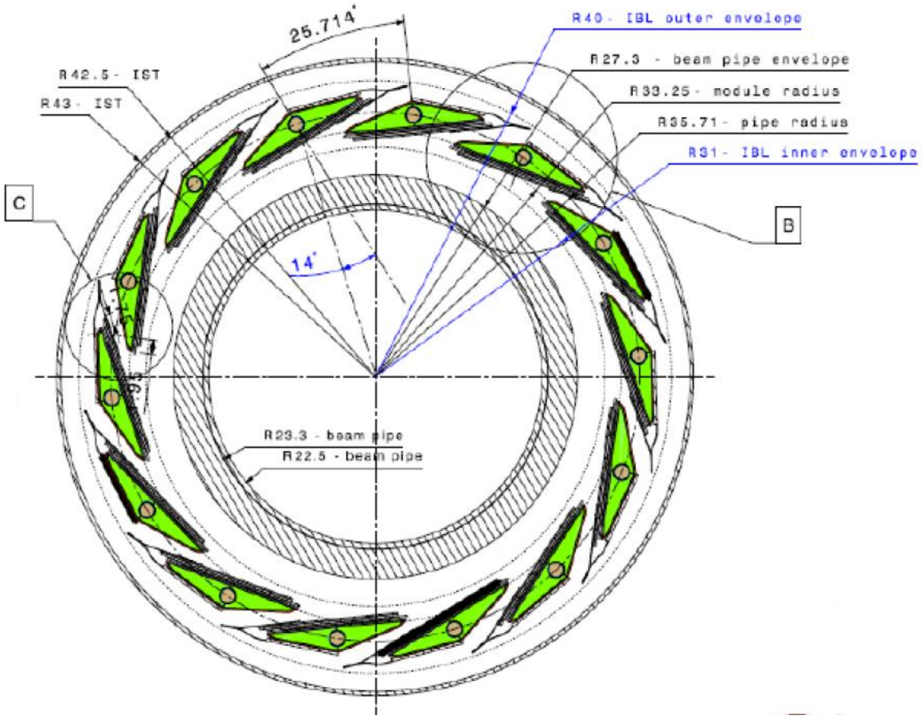
Motivation for new Service Quarter Panels (LS1):

- Move on-detector opto-electrical transceivers (optoboards) to a serviceable location
- Allow later Layer 1 readout speed upgrade to 160 Mbit/s (add second line for Layer 1 modules data lines)
- While detector is on the surface: repair all accessible failures

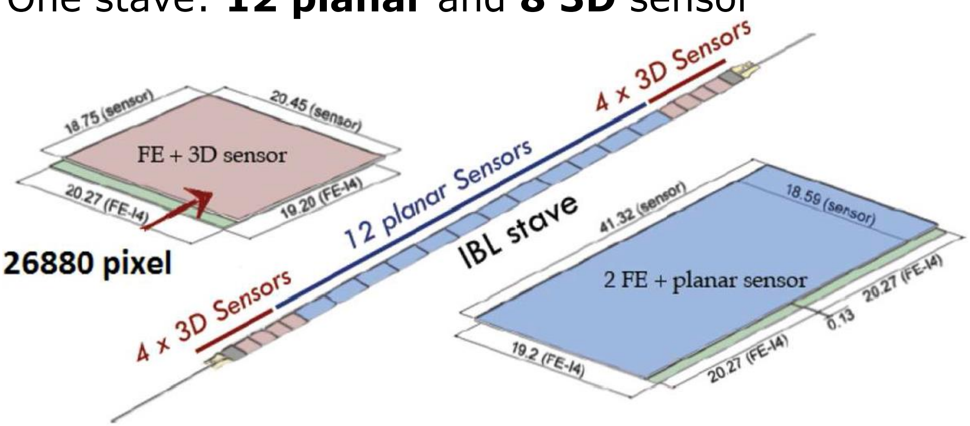




LS1 upgrades: IBL



One stave: **12 planar** and **8 3D** sensor

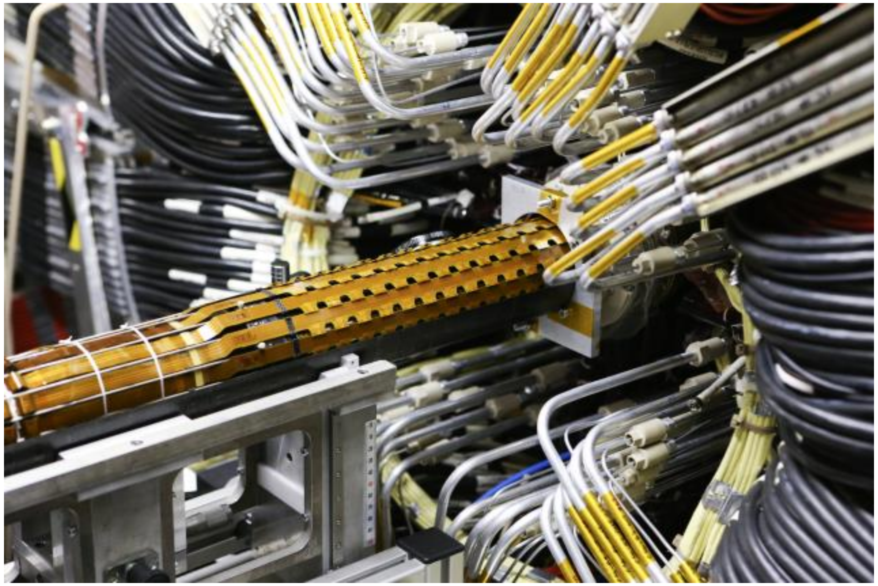


IBL a new inner most layer:

- With a new reduced beam pipe radius
- 14 staves inside a 10mm radius envelope
- New detector: sensor, FE, readout, cooling

Why?

- B-layer aging was anticipated
- Improvement of the tracking performance



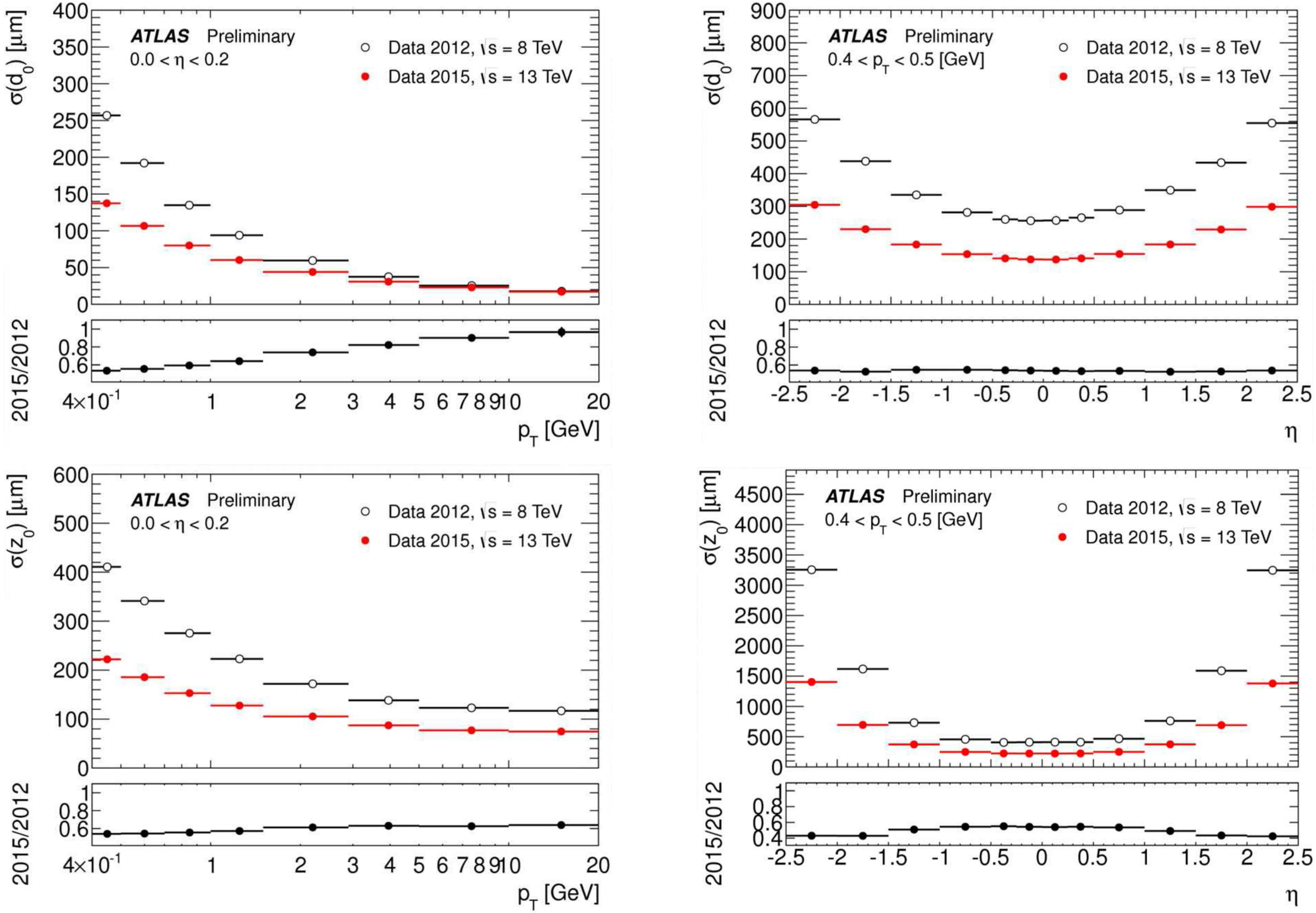
→ Alessandro's talk

Improved performance with IBL

Comparison of Run 1 and Run 2 impact parameter resolution

Transverse impact parameter

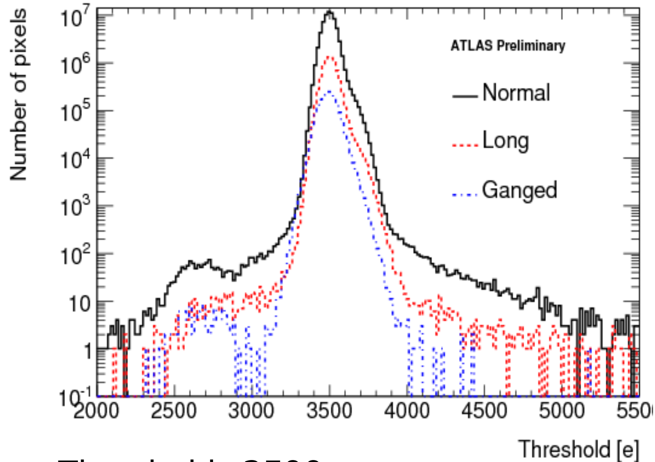
Longitudinal impact parameter



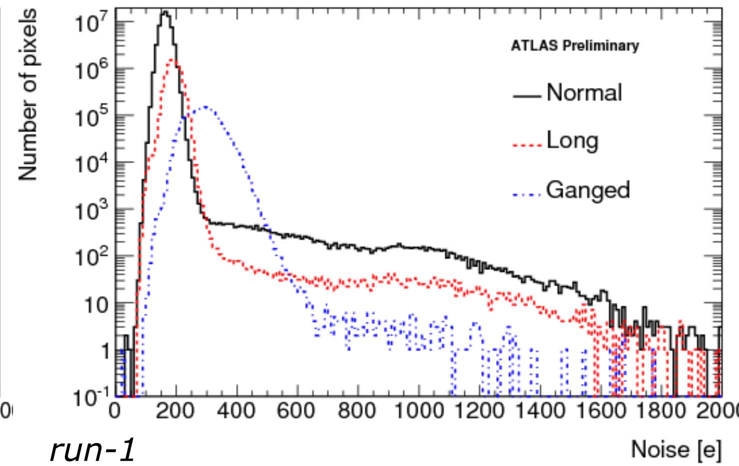
Detector Calibration

Performance is partly related to the detector calibration

Typical Threshold/Noise



Threshold: 3500 e
Dispersion ~40 e-
Module by module variation: few e^-



run-1

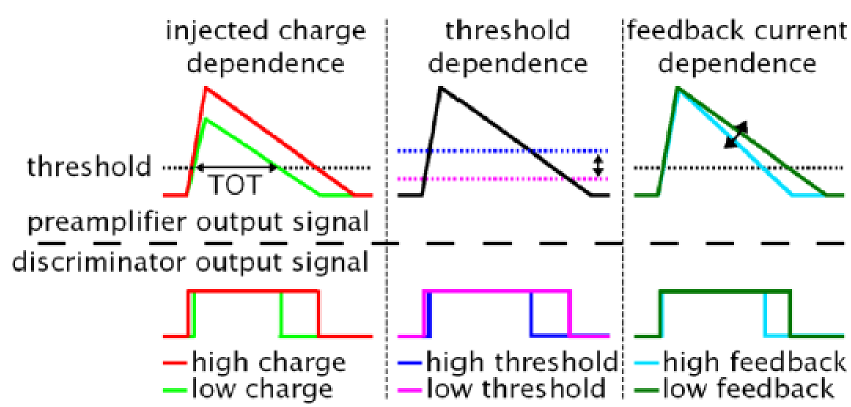
Typical Noise (normal Pixels)= 170 e^-

Time-over-threshold (ToT):

length of discriminator signal

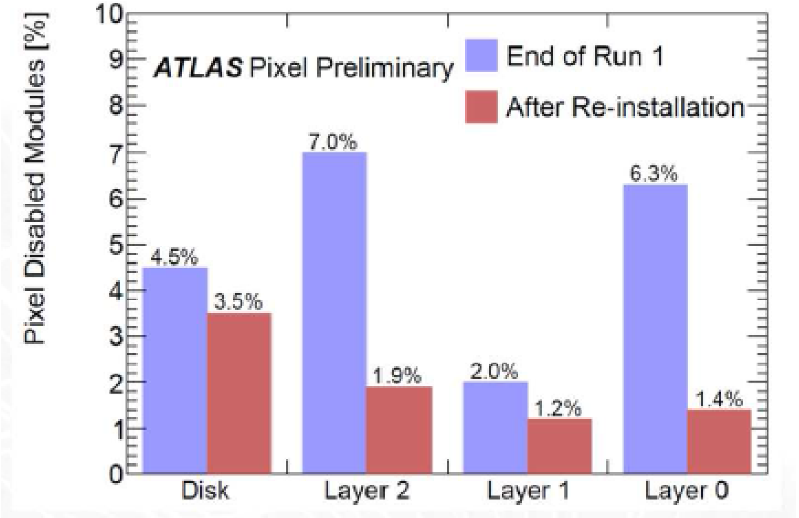
- Measurement of the *deposited charge*
- Used to extrapolate *analogue hit position*
- Preamplifier-rise time can shift low ToT hits into the next time bucket (BC) → *"Timewalk"*
- Mechanism to recover time walked hits ("ToT-doubling"): copy low ToT hits to the previous BC for readout
- ToT usually tuned pixel by pixel to 30 BC @ 20ke

ToT depends on:
charge, threshold, feedback current



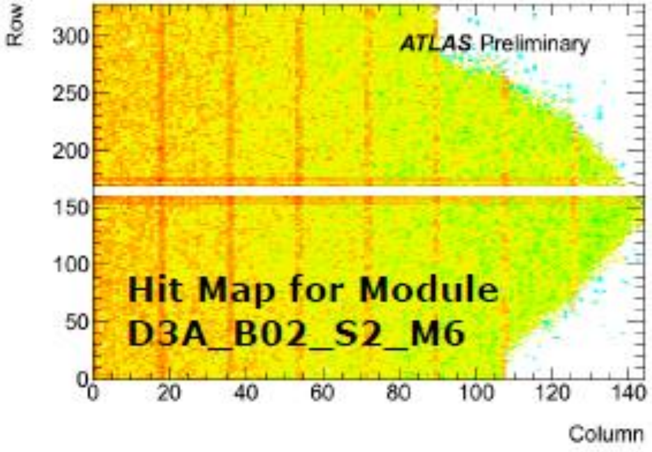
Efficiency

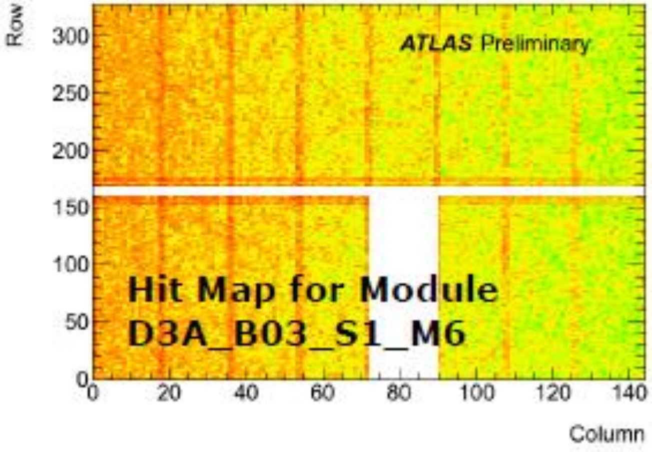
Coverage after LS1



On-Detector sources of Efficiency Loss

- Offline Calibration Loop to identify
  - Inefficiencies related to dead channels, FE, Modules, Optical links, …
  - Noise





Operational Limits

Pixel built for Luminosity of $1x10^{33}$ $cm^{-2}s^{-1}$, 100 kHz trigger rate, 50 Mrad / $1x10^{15}$ 1MeV neq cm^{-2} at LHC (B-Layer replacement was foreseen). Operation limits arise from these constraints, as well as general considerations.

Intrinsic to detector limitations:

- Bandwidth
- Buffer size limitations: FE and back-end
- Detector coverage → related to detector granularity issues
  - Tracking and reconstruction to deal with known holes
- Power and DCS limitation
  - HV Leakage Current related to radiation damage or breakdown
  - Power limitation and budget (may need to be adjusted with detector aging)
- FE and module losses in-run due to SEUs
  - Requires module reconfiguration and causes dead time

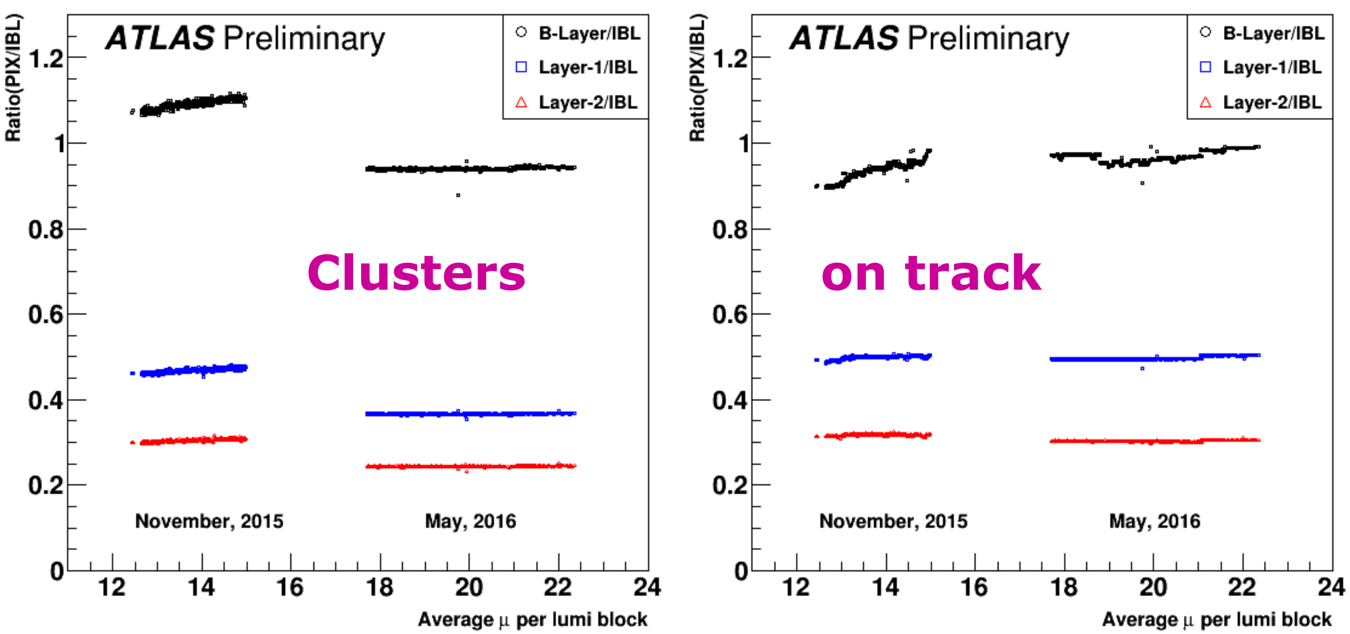
Other external factors:

- Robustness of procedures and software
- Expertise for operation and calibration

Anticipation in 2016

- Occupancy reduction given the increased luminosity in 2016
  - Disable ToT doubling in all Pixel Layers
  - Increase ToT cut to avoid reading out out-of-time hits
  - IBL was unchanged

→ Save ~20% occupancy, clusters on-track unaffected

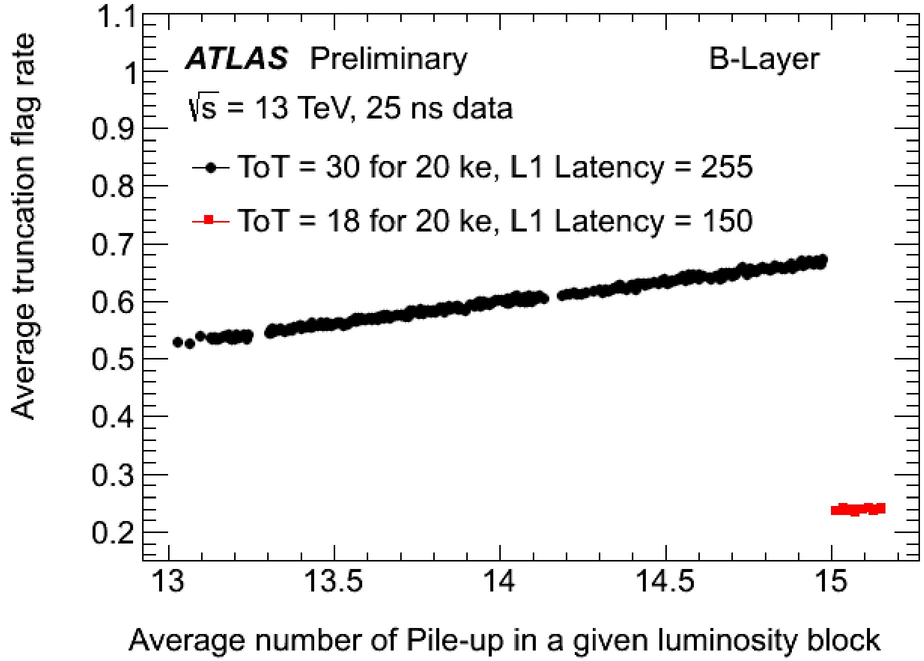


B-Layer FE efficiency

- No sign of efficiency loss in 2015 for B-Layer
- But with expected pile-up of 2016 up to 40 this would lead to uncontrolled level of truncation in the FE → truncation errors would saturate at 100%

- **Addressed by decreasing the FE Latency**
  - Buffer size latency 255 BC → 150BC
  - Each hit will clear the FE buffer 100 BC earlier
  - Retune ToT to keep the dynamic range, at reduced charge resolution

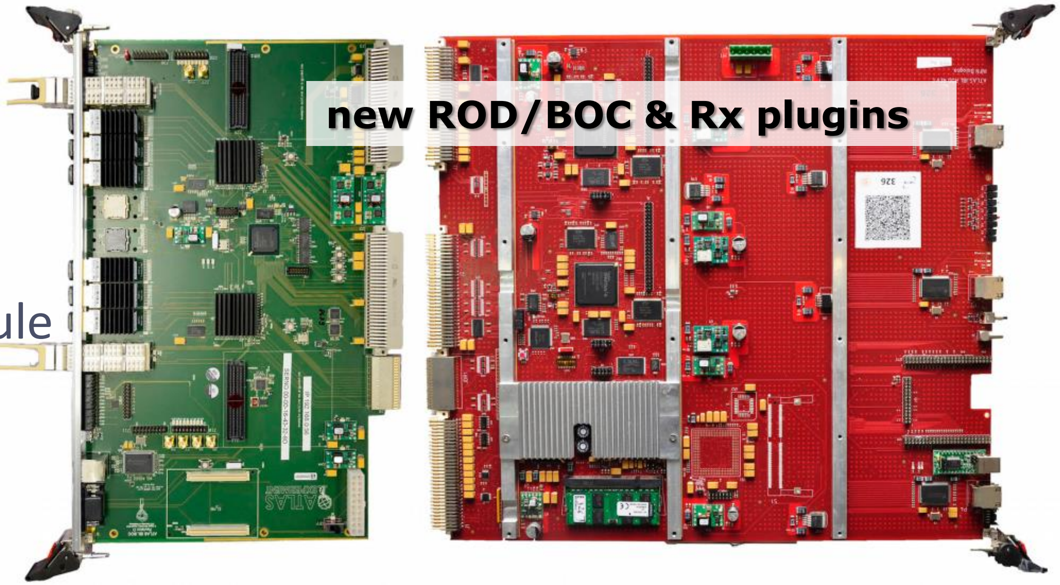
→ Truncation drastically reduced: < 10% in 2016



Bandwidth

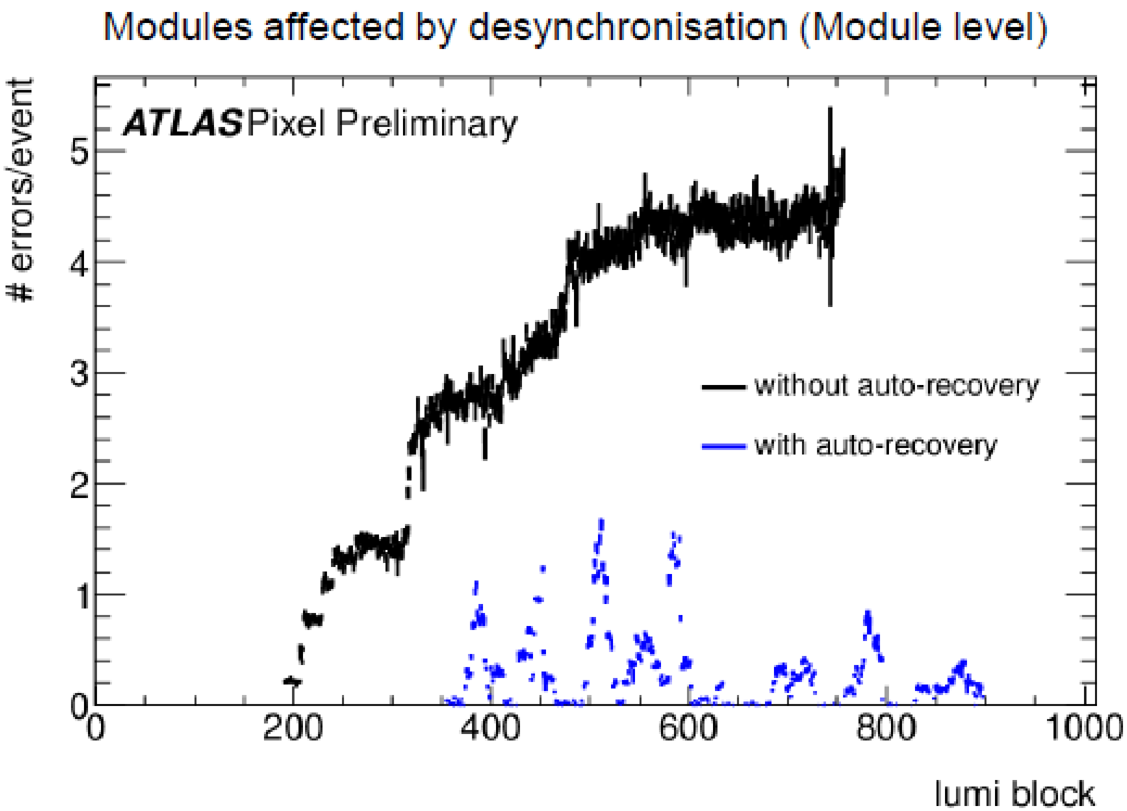
- Layer 2 was operated at 40 Mbit/s → Would be the first to be affected by bandwidth limitations
  - first signs already seen end of run 1 and also in 2015 →significant desynchronisation at high occupancy and trigger rate
  - **Layer 2 Upgrade completed during 2015 YETS** → bandwidth doubled to 80 Mbps, using IBL off-detector readout electronics

- **Layer 1 Upgrade foreseen for 2016 YETS**
  - bandwidth will be doubled to 160 Mbps
  - using Layer 2/IBL readout electronics
  - one additional fiber per module to allow 2X80 Mbit/s was installed during LS1



SEU

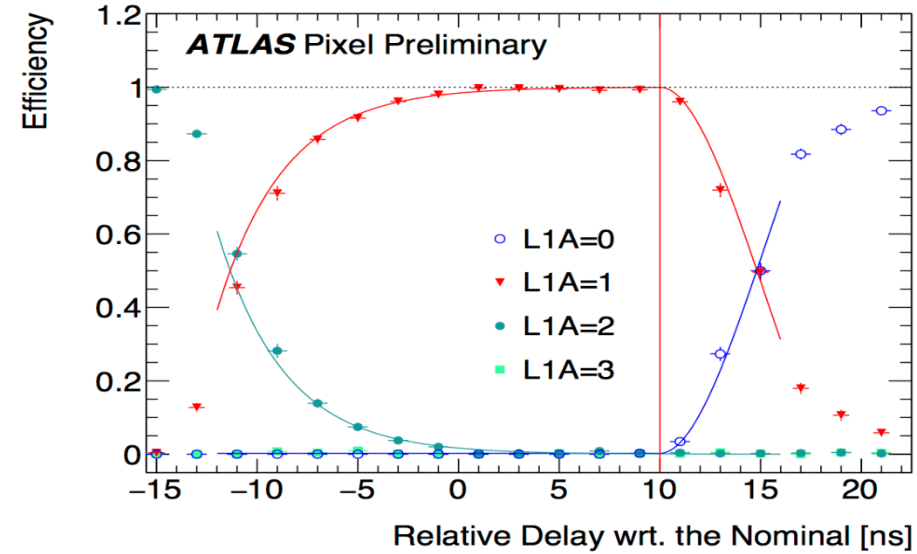
- SEUs lead to local inefficiencies with various symptoms (Desynchronization, efficiency loss, LV current steps, …)
- Recover by back-end and or module reconfiguration
- Effect is dominant in 2016 also for IBL

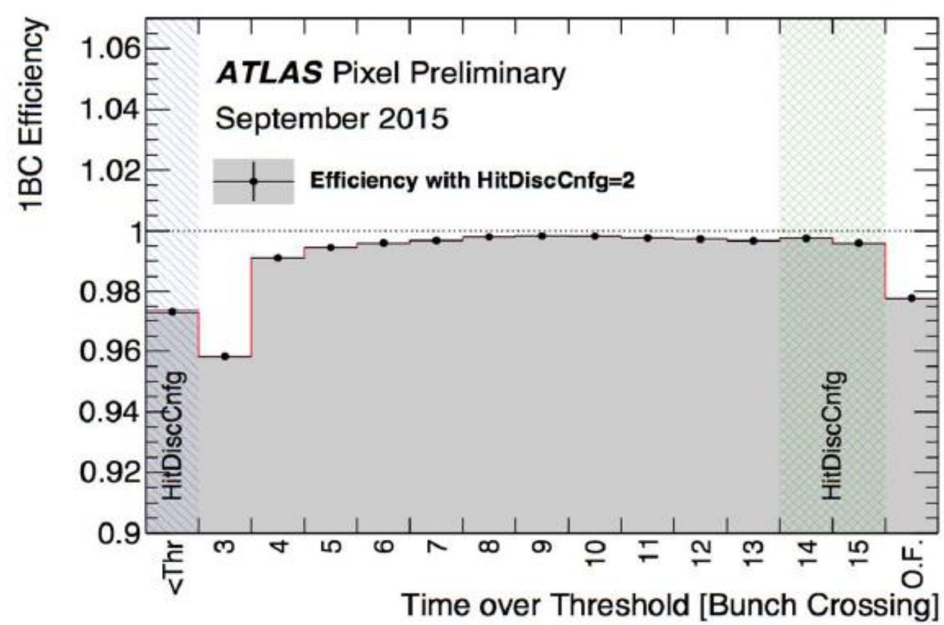


Detector Timing

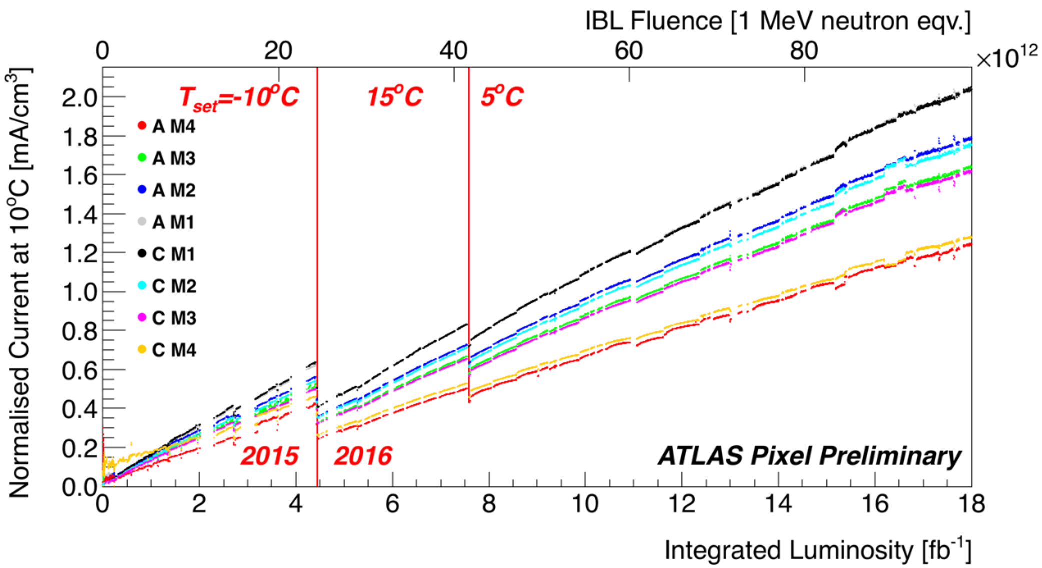
- Goal is to take data within 1 BC
- If timing not properly adjusted → inefficiencies
- Timing adjustment is done at the level of the module and FE granularity
- IBL is a new detector and fine tuning completed successfuly in 2015
- Fine tuning allows better 0.1ns

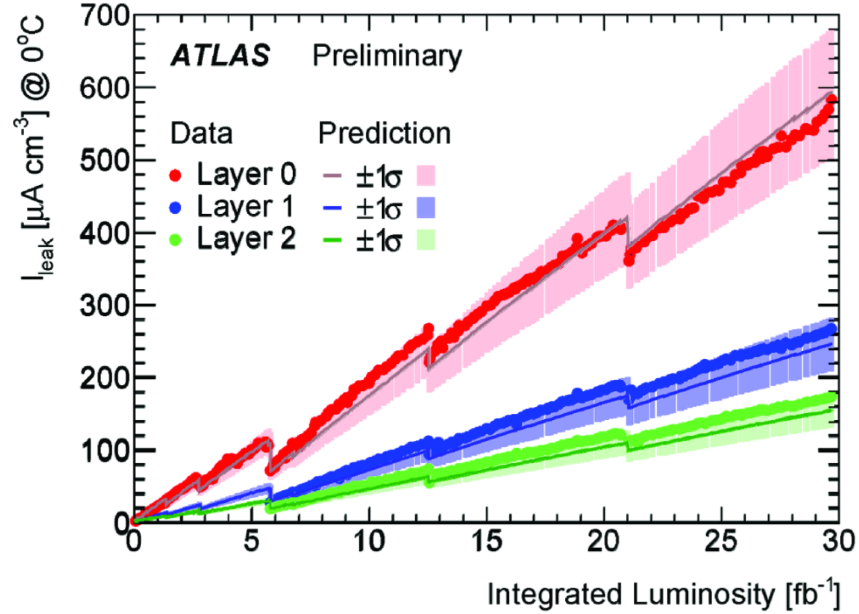
Pixel readout with 1BC
Since September 2010





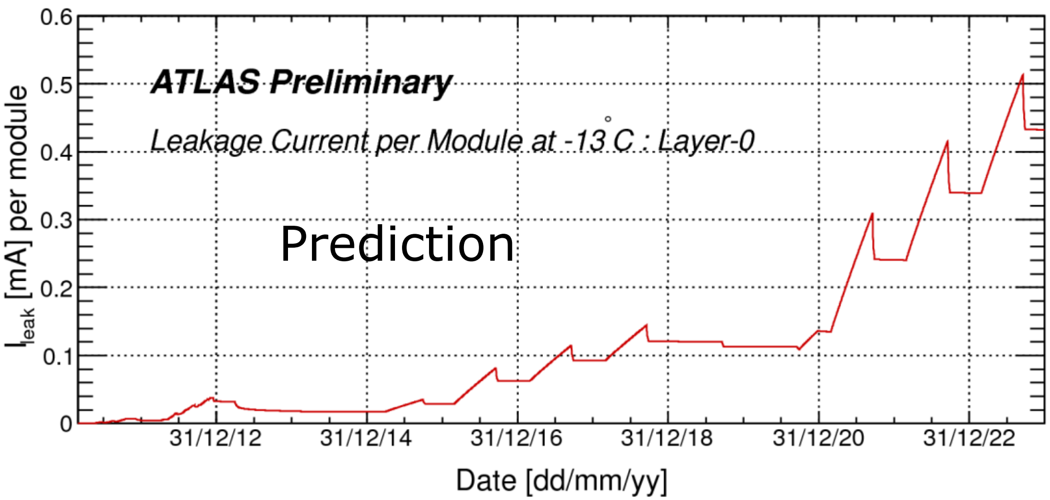
Leakage Current evolution





Expected increased sensor current is regularly monitored for both Pixel and IBL

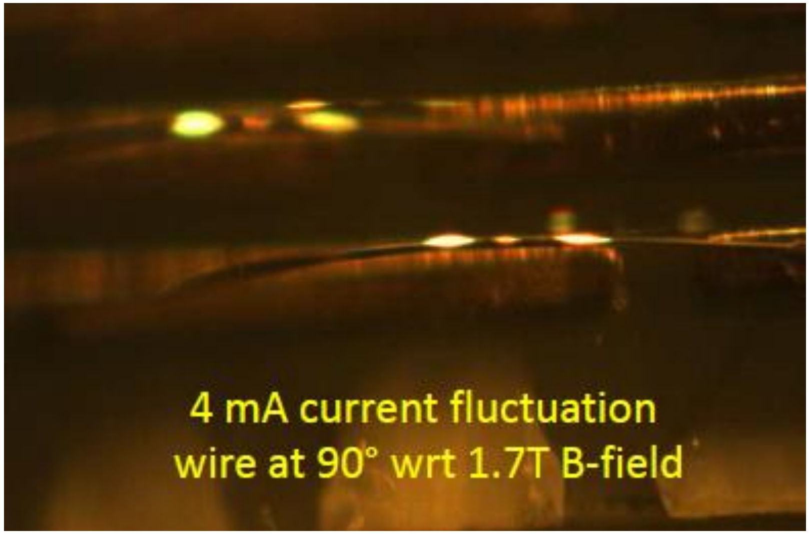
→ Power budget still comfortable wrt limitation

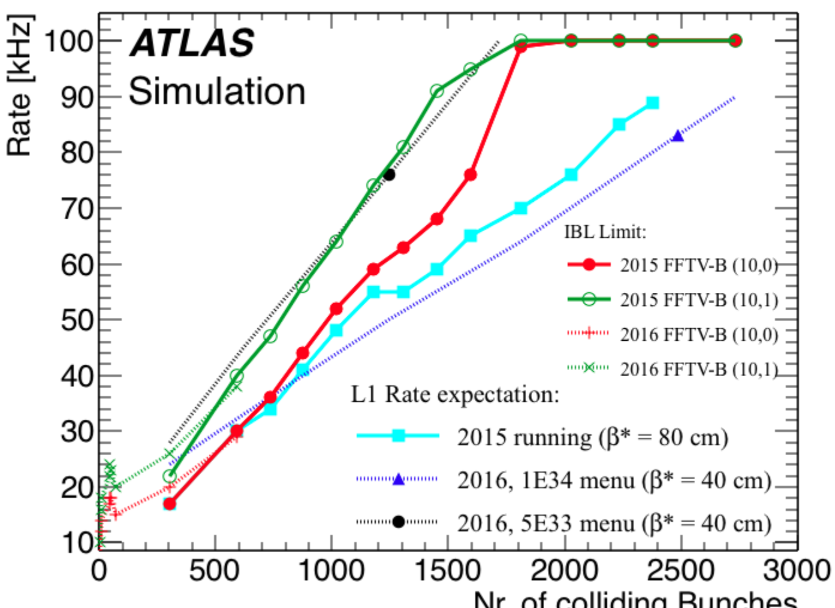


Other Challenges

- Detector features and protection
  - Wire bonding oscillation
  - Mechanical distortion#
  - FE LV current increase with TID
  - Readout limitations

IBL Wire Bond Oscillations



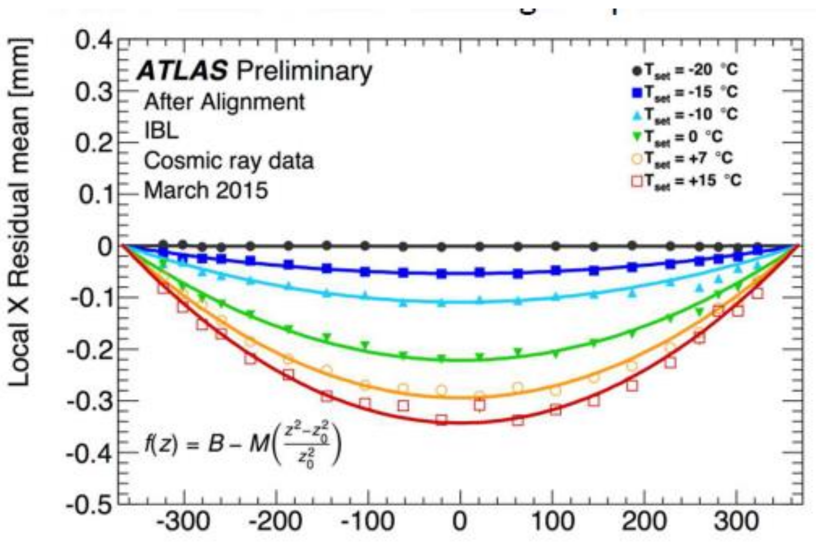


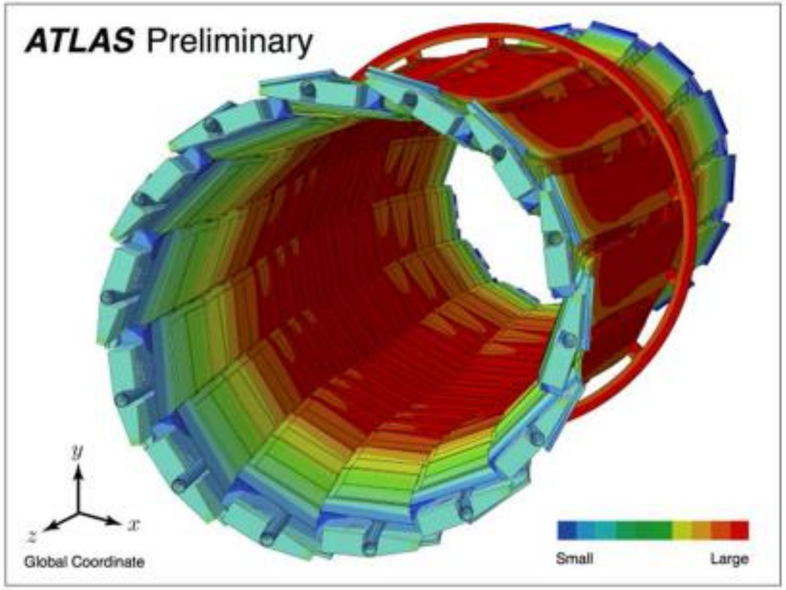
IBL wire bonds susceptible to some resonance frequencies during data taking

- Protection Scheme implemented into the readout chain for data taking and calibration
- Fixed Frequency Trigger Veto (FFTV): limiting the number of triggers in resonance region
- Trigger Veto is dependent on LHC filling scheme
  - no rate limitation in 2015
  - reviewed parameters in 2016 to avoid limiting rate while keeping the detector safe.
- Few occurrences in the experiment of fixed frequency trigger at 11 or 22 kHz → protection essential

IBL Mechanical Distortion

- During early cosmics run, temperature dependent distortion was observed in IBL, O(10um/K)
- Due to CTE mismatch between service bus and stave
- Impact on tracking performance → temperature dependent alignment correction → *Javier's poster*
  - large temperature excursion made a LB dependent correction necessary, implemented 2016
- *Avoid temperature cycles inducing mechanical stress*
  - *CO_2 cooling very stable and reliable* → *Bart's talk*



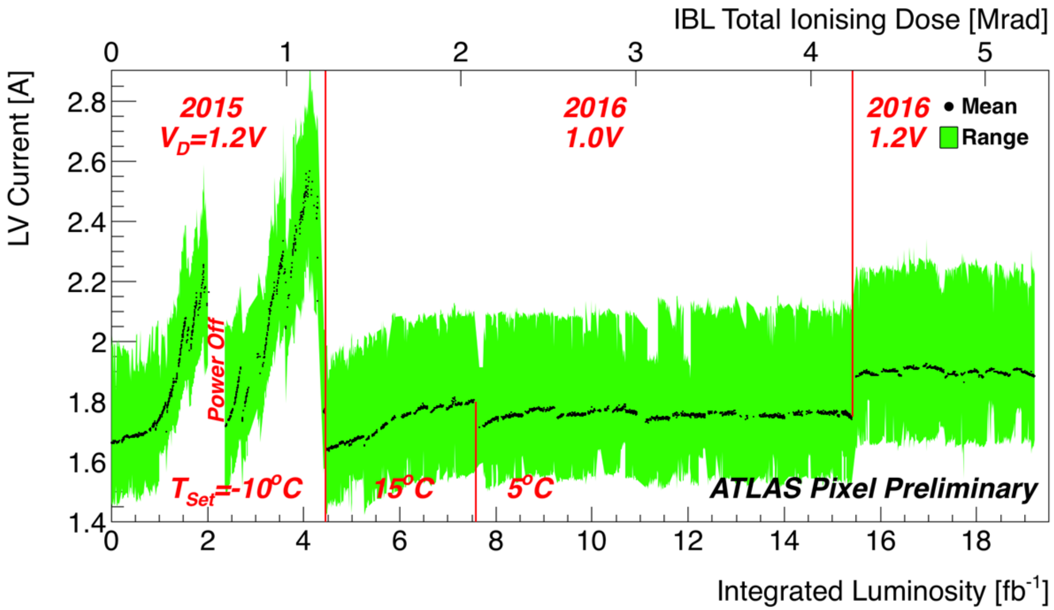


IBL LV current drift

→ *Karola's talk*

Starting from summer 2015, IBL frontends started to show a drift in LV current and fast detuning of threshold and ToT.

- ***With increasing TID, LV currents exceeded values beyond safe operation parameters***
  - Switched off IBL for one run in October, and module groups when reaching critical level
  - Detuning → regular monitoring and retune, phase space for tuning reduced



Task force was set-up:

Understand the cause of the issue
+
Lab measurements were essential to drive the operation conditions
+
Assessed the impact of running IBL warm for one year

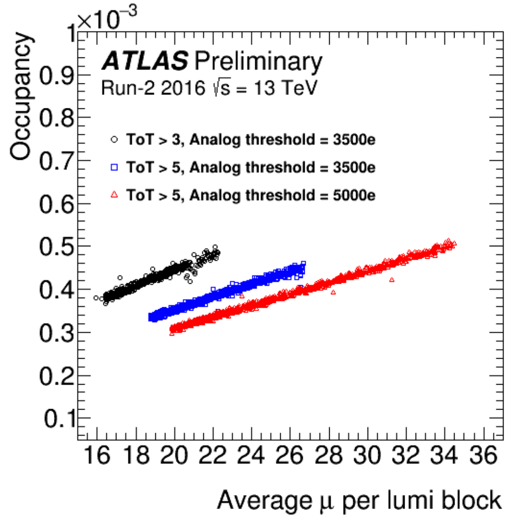
In 2016 the increased peak luminosity for the same detector condition would have led to operational issue…

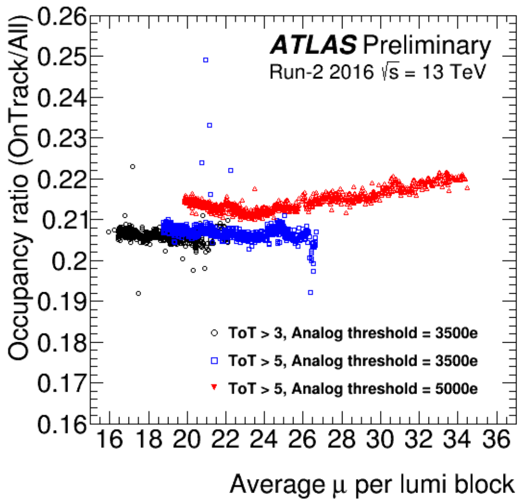
The recommendations were:

- Higher temperature
- Lower digital supply

B-Layer Limitation in 2016

- In Pixel B-Layer, bandwidth issues were not foreseen before a factor of 2-3 higher occupancy
- In 2016 readout problems were already observed at a luminosity of $1x10^{34}$ $cm^{-2}s^{-1}$
- Source was identified as:
  - LHC beam is not uniform: up to 30% fluctuation between bunch crossing ID
  - Readout is designed for average data rates: large events can cause problems
- Mitigation:
  - Occupancy reduction: TOT cut and higher analog threshold (impact on tracking limited)
  - Firmware improvements
- **B-Layer is working stable since then**

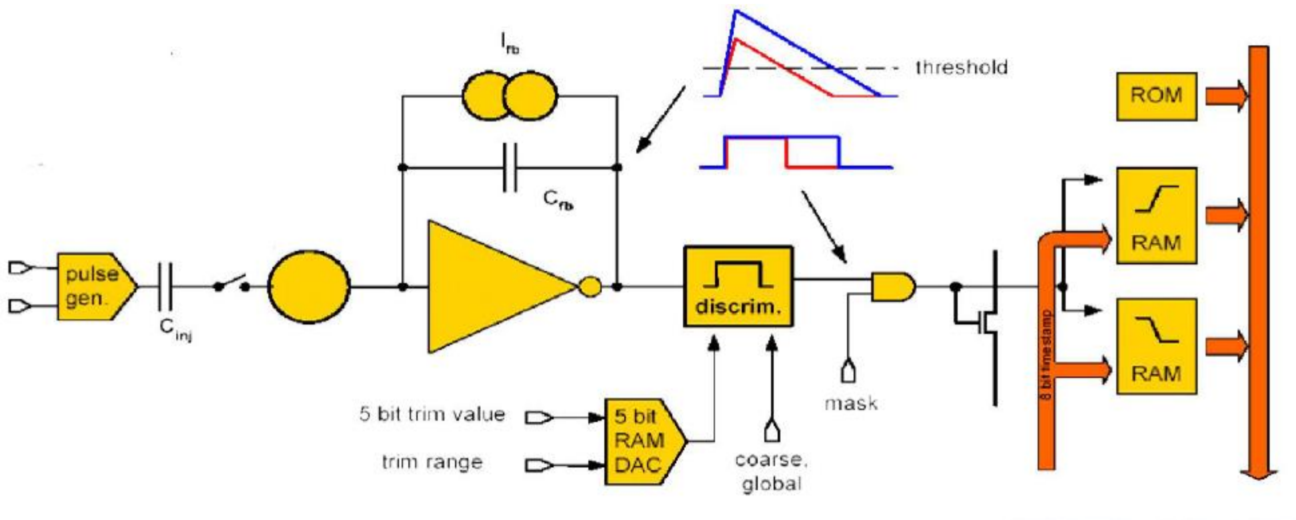




Conclusions

- **ATLAS tracking at Run-2 significantly improved** with IBL as new innermost Pixel layer
- **Good performance seen since beginning of run 2** for IBL and Pixel
- **Anticipated a number of limitations**, successful changes to the detector configuration and hardware in view of increased luminosity
- Unforeseen **challenges addressed and overcome**
- **Approaching stable operation for run conditions** beyond LHC design luminosity

BACKUP



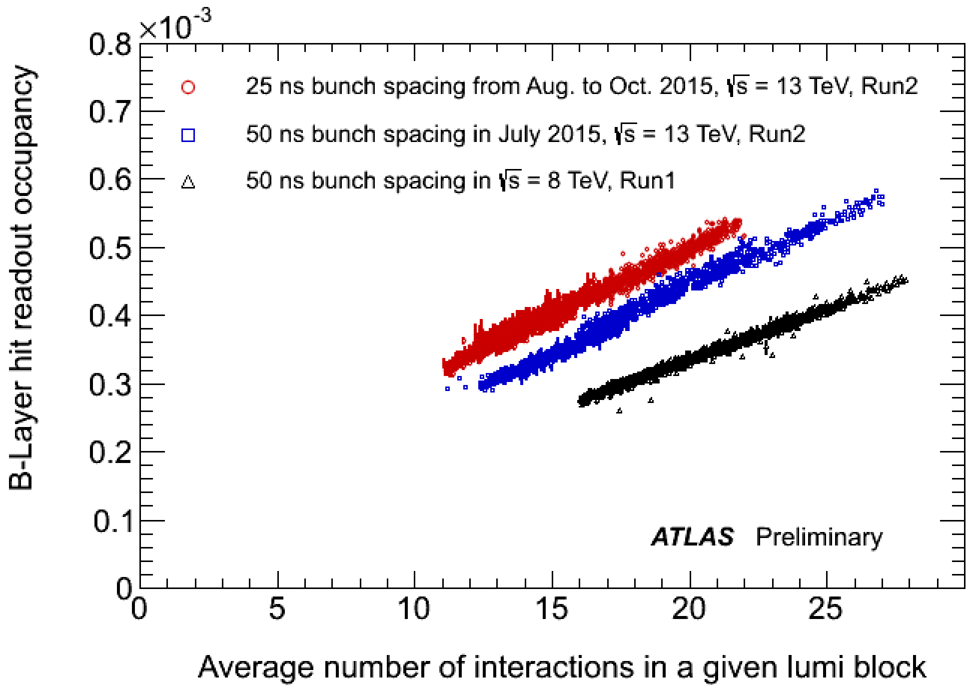
Pixel Cell

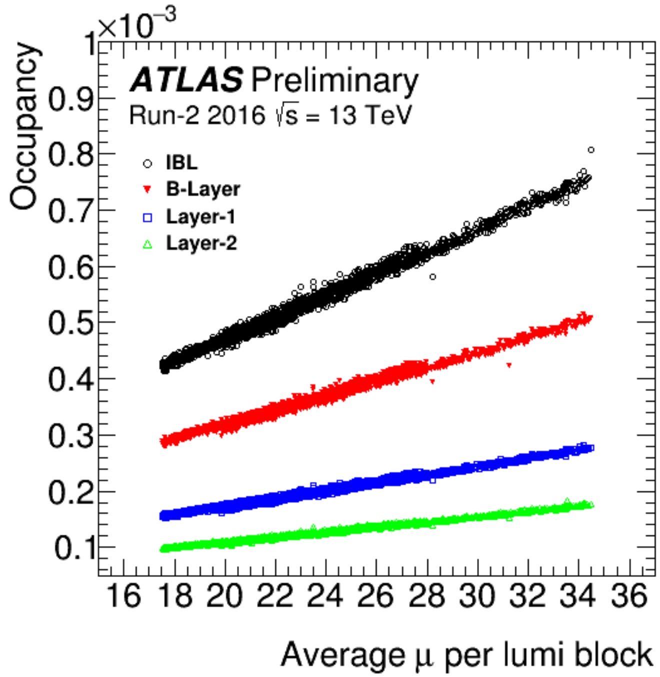
- Amplifier with *adjustable constant current feedback*
- Discriminator with *7-bit threshold* adjust
- Circuitry to measure *Time over Threshold* (ToT)
- Possibility for analogue and digital *test injection*

End Of Column

- *Hit storage* during Level-1 trigger latency
- *64 memory buffers* for each column pair of 2 x 160 pixels ("EoC Buffers")
- Hit data: pixel ID + timestamp + ToT

Occupancy vs Pileup





Run 2:

- additional material
- 25 ns operation
- increasing target luminosity