Contribution ID: **17** Type: **poster**

A 12-bit, 1 MS/s, Digitally-Calibrated SAR-ADC Used for CZT-Based Multi-Channel γ-Ray Imager

In this paper, we focus on the design of a 12-bit 1 MS/s radiation-hardened, digitally-calibrated SAR-ADC used for CZT-based multi-channel γ-ray imager. A 64-channel CZT-based imaging system developed in our laboratory comprises a CZT-pixelated detector, a 64-channel front–end readout chip, 64 analog-to-digital converter (ADC) chips, a digital signal processor, and an image-reconstruction platform (e.g., workstation or PC). The output analog voltages of 64 channels front-end readout chip are simultaneously sampled and digitalized using the 64 low-power and high-resolution SAR-ADC chips.

The previous works in digitally-calibrated SAR-ADC usually adopt 1.86-radix capacitors in both LSB and MSB with perturbation technique. However, for LSB-weights calibration, since the input of analog signal is very small, the perturbation could be beyond the level of ground, and the calibration can not be realized. Considering that the variation of the LSB capacitors contributes insignificant errors to the conversion accuracy, the new DAC structure with 2-radix capacitors in LSB and 1.86-radix capacitors in MSB is adopted in the proposed SAR-ADC for digital bit-by-bit calibration. The weights of LSB are fixed at 2-radix, and the weights of MSB are digitally-calibrated by the bit-by-bit calibration technique using the weights of LSB.

Two radiation-hardened design technologies are utilized in the layout design to improve the radiation tolerance of the SAR-ADC. Firstly, the P+ and N+ guard rings are added in NMOS and PMOS transistors, respectively, the guard rings provide a path for the large current leakage which is caused by high energy particles, to prevent latch-up from occurring. Secondly, the distance between PMOS and NMOS transistors is increased as compared with the ordinary situation, which can increase the base region of the parasitic bipolar, thus can reduce the current amplification factor and can prevent latch-up from occurring.

A 12-bit 1 MS/s SAR-ADC prototype chip is designed and implemented in 0.35μm mixed-signal 3.3V/5V CMOS process. The die size of the SAR-ADC core is 856μm ×802μm. Fast Fourier transform (FFT) techniques are used to test the dynamic performances of the ADC, including distortions and noises. When the frequency of the input sinusoidal signal is 9.9 kHz and the sampling rate is 1 MS/s, the simulation results show that, the signal-to-noise and distortion ratio (SINAD) is 70.10 dB and effective number of bits (ENOB) is 11.35-bit, the power dissipation of SAR-ADC is 3mW, and the figure of merit (FOM) is 1.15pJ/conversion-step.

The SAR-ADC developed in this paper is with the features of high precision, low power, small die size, and radiation-hardened, it can be used in the pixelated detector imaging system.

Primary authors: Dr LIU, Wei (School of Computer Science and Engineering, Northwestern Polytechnical University, Xi'an 710072, PR China); Prof. WEI, tingcun (School of Computer Science and Engineering, Northwestern Polytechnical University, Xi'an 710072, PR China)

Presenter: Prof. WEI, tingcun (School of Computer Science and Engineering, Northwestern Polytechnical University, Xi'an 710072, PR China)