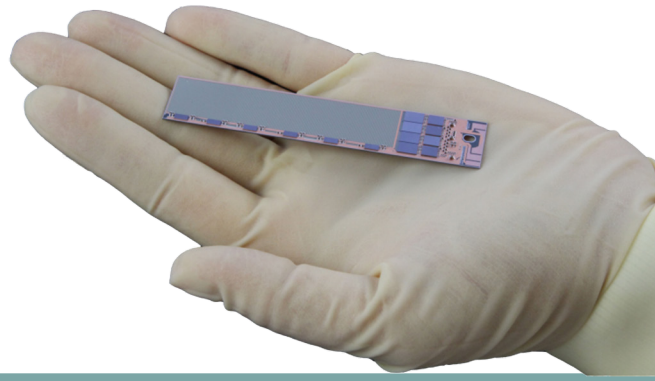
The Belle II Pixel Vertex Detector

8th International Workshop on Semiconductor Pixel Detectors for Particles and Imaging (Pixel 2016)

Sestri Levante, September 5th - 9th 2016

C. Koffmane for the DEPFET collaboration



Outline

- DEPFET Collaboration
- SuperKEKB and BELLE II experiment
- The BELLE II Vertex Detector
  - Phase 2 – Beast II
  - Phase 3 – complete VXD
- PXD Module
- Production and QA test results
- Electronic Shutter (Gated Mode)
- CO2 cooling and thermal mock-up
- VXD Combined Beam Test
- Summary and Outlook

Topics not covered in this talk … but equivalent important:

- Irradiation campaigns of ASICs and DEPFETs
- Power Supply
- Grounding
- DAQ Hardware/Firmware
- Slow Control
- DQM
- Cables, PCBs and connectors …

DEPFET Collaboration

- Original Collaboration: DEPFET pixel detector @ ILC (since 2002)
- now: design, deliver and operate the PXD for Belle II

IHEP Beijing, China (Z.A. Liu)
Charles University, Prague, Czech Rep. (Z. Dolezal)
DESY Hamburg (C. Niebuhr)
University of Bonn (J. Dingfelder)
University of Hamburg (C. Hagner)
University of Heidelberg (P. Fischer)
University of Giessen (W. Kühn)
University of Göttingen (A. Frey)
University of Karlsruhe (T. Müller, I. Peric)
University of Mainz (C. Sfienti)
MPG Semiconductor Laboratory, Munich (J. Ninkovic)
Ludw.-Max.-University, Munich (T. Kuhr)
MPI for Physics, Munich (H.-G. Moser)
Technical University, Munich (S. Paul, A.Knoll)
Struct. Biol.Research Center, KEK (S. Wakatsuki)
IFJ PAN, Krakow, Poland (M. Rozanska)
University of Barcelona, Spain (A. Dieguez)
CNM, Barcelona, Spain (E. Cabruja)
IFCA Santander, Spain (I. Vila)
IFIC, Valencia, Spain (J. Fuster)
University of Tabuk, Saudi Arabia (R. Ayad)

DEPFET@Belle II

Management

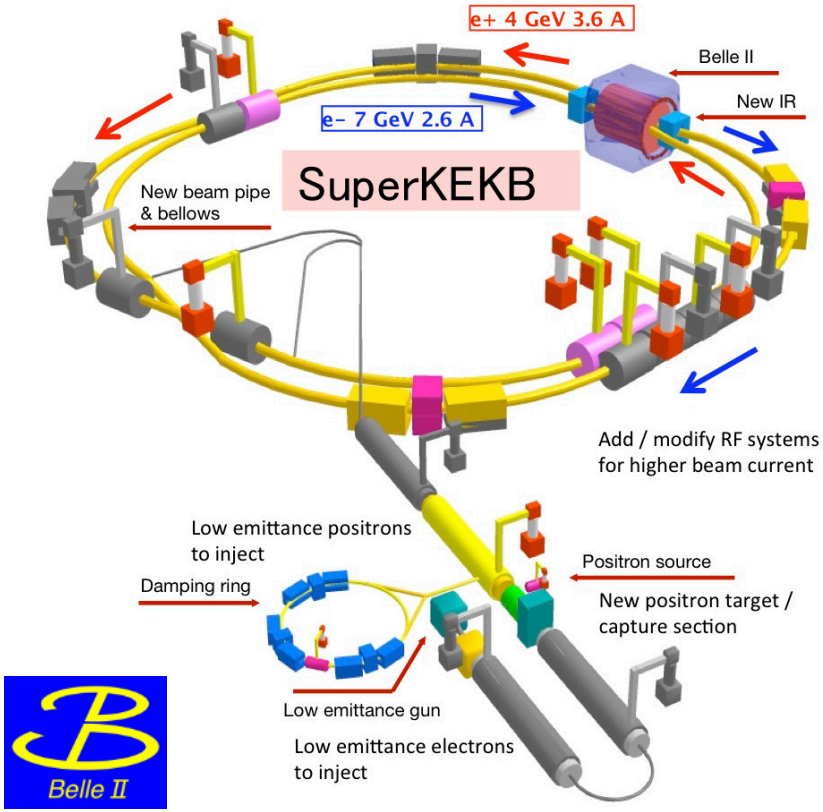
Project Leader
C. Kiesling (MPI)

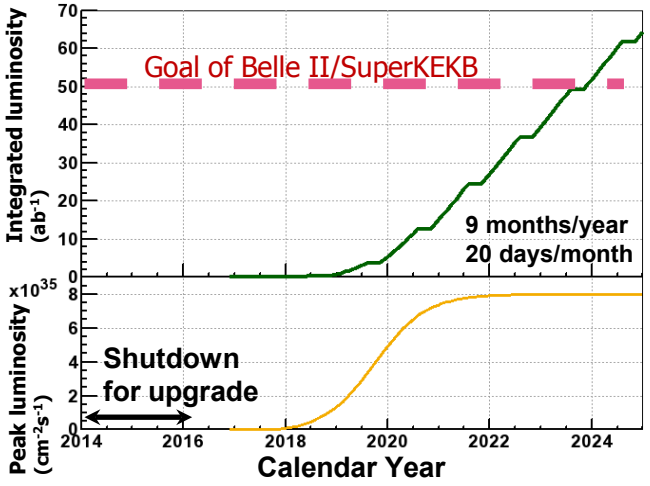
Technical Coord.
L. Andricek (HLL)

IB- Board
Chair: J. Dingfelder (Bonn)

Integration Coordinator
Shuji Tanaka (KEK)

SuperKEKB and the BELLE II experiment

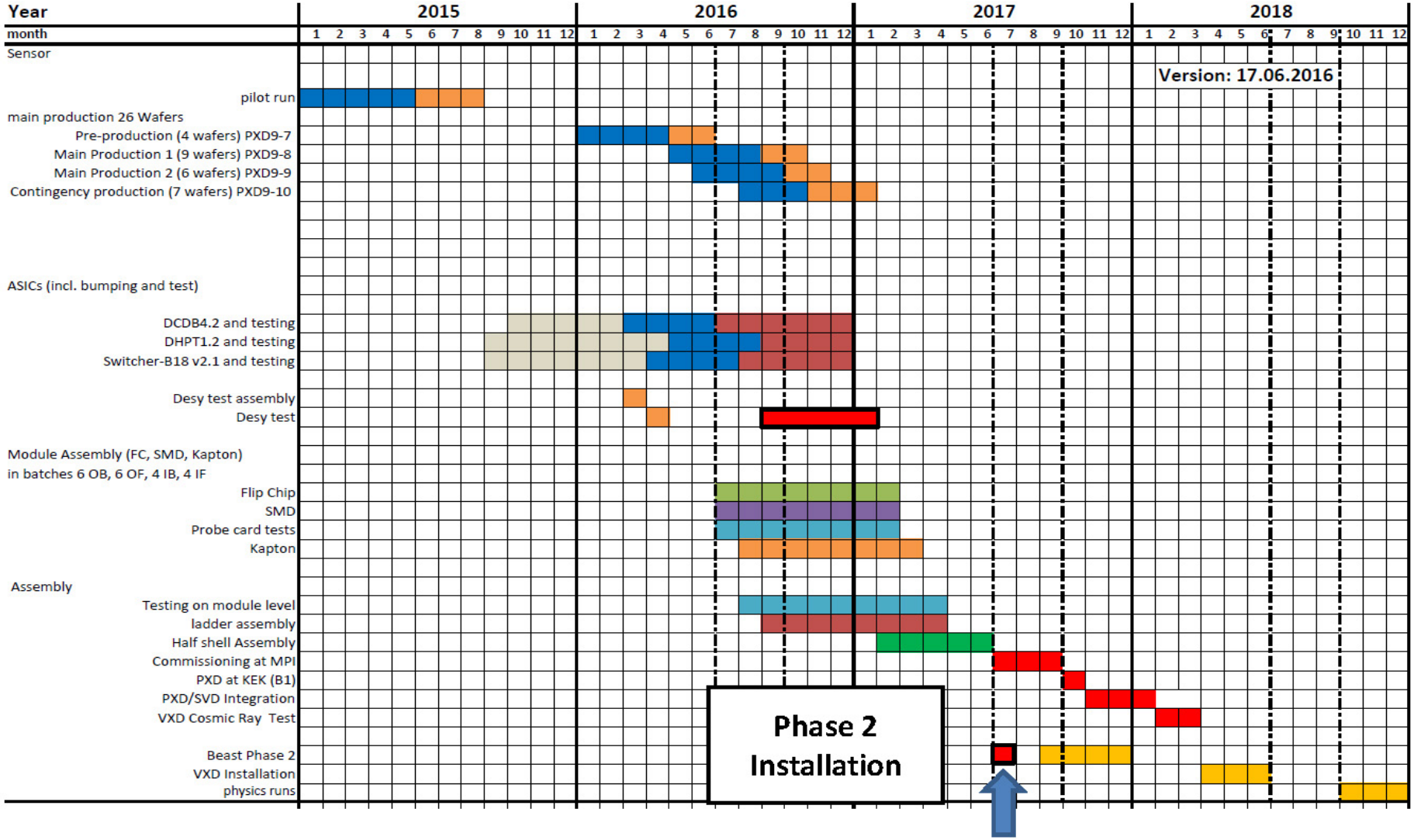




Beam parameters		KEKB		SuperKEKB		units
		LER	HER	LER	HER	
Beam energy	E_b	3.5	8	4	7	GeV
Vertical beam size	d_V	0.94	0.94	0.048	0.056	µm
Horizontal beam size	d_H	150	150	10	11	µm
Beam currents	I_b	1.64	1.19	3.60	2.60	A
Luminosity	L	2.1×10^{34}		8×10^{35}		$cm^{-2}s^{-1}$

- Asymmetric energy (4 GeV, 7 GeV) e+e- collider at the E_{cm} = 10.58 GeV – Y(4S) to be realized by upgrading the existing KEKB machine
- Final luminosity $\mathcal{L} = 8 \times 10^{35}$ cm^{-2} s^{-1}, 40 times higher than the existing KEKB Factory
- Luminosity will be achieved by squeezing the beams (nano beam)
- Talk on **Impact of the Belle II Pixel Detector on CP-Violation Measurements** by Fernando Abudinen, Sept. 6th

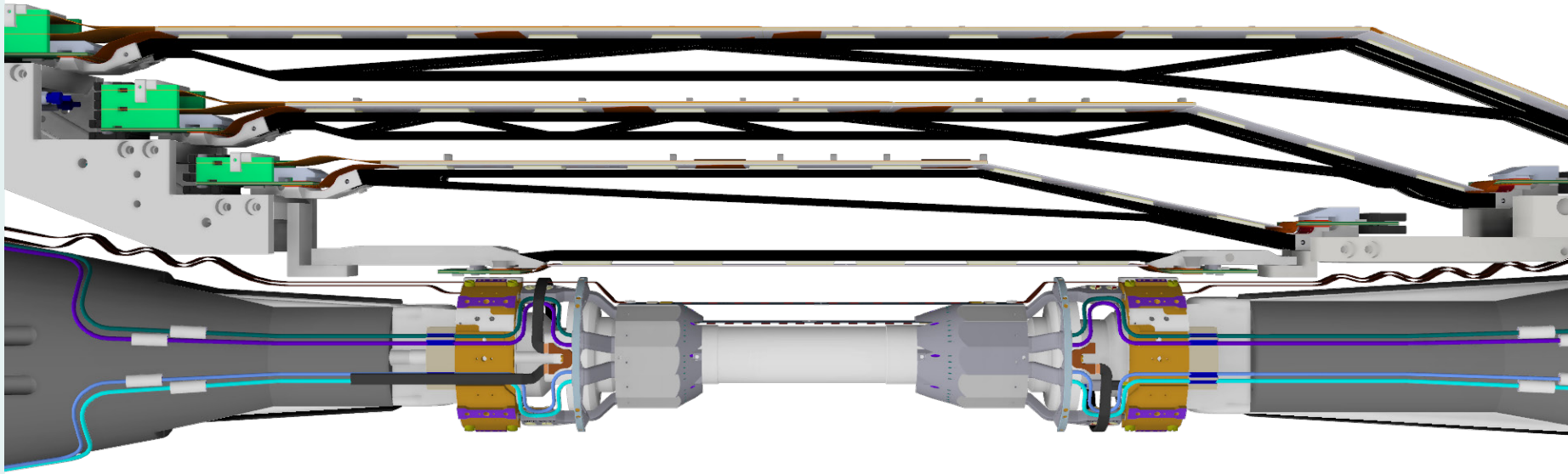
Commissioning Schedule



24th Belle II General Meeting: https://kds.kek.jp/indico/event/21740/

VXD Phase 2 Hardware

- Machine commissioning
- Radiation safe environment for the VXD
- Two PXD and four SVD layers
- +X direction, horizontal plane (highest background sensitivity)

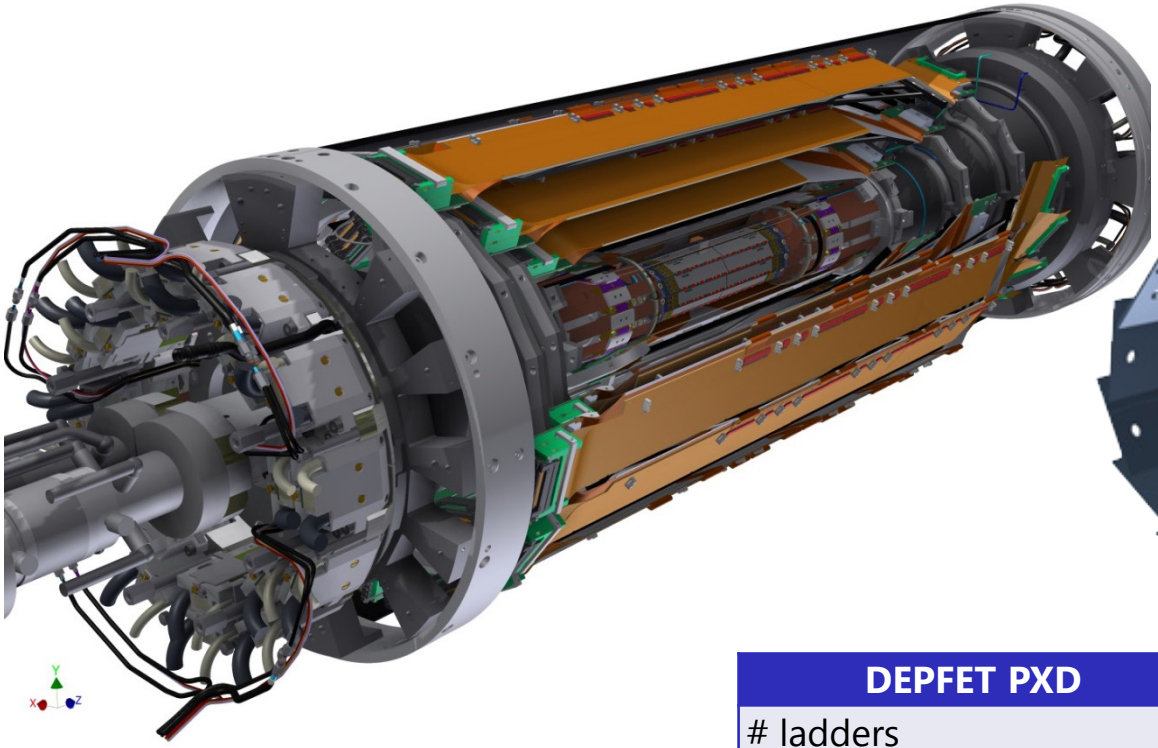


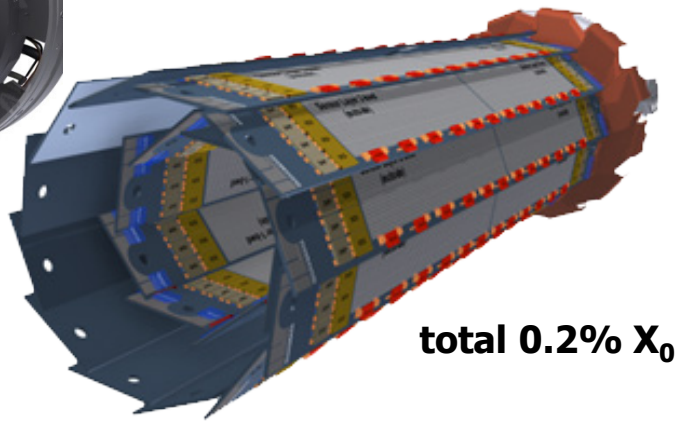
Integration of the phase 2 hardware (incl. other radiation monitors): November 2016 @ DESY

Installation at KEK: July 2017

+X

The BELLE II Vertex Detector



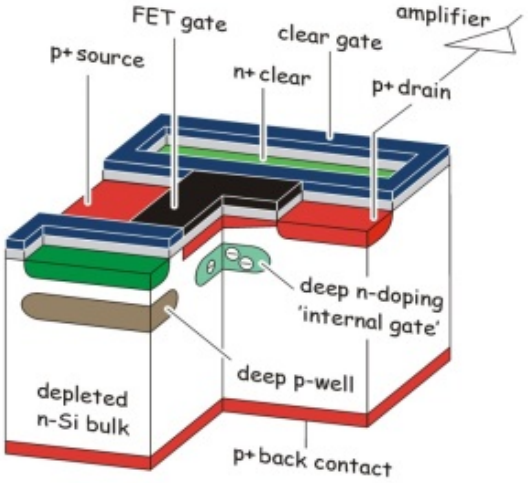


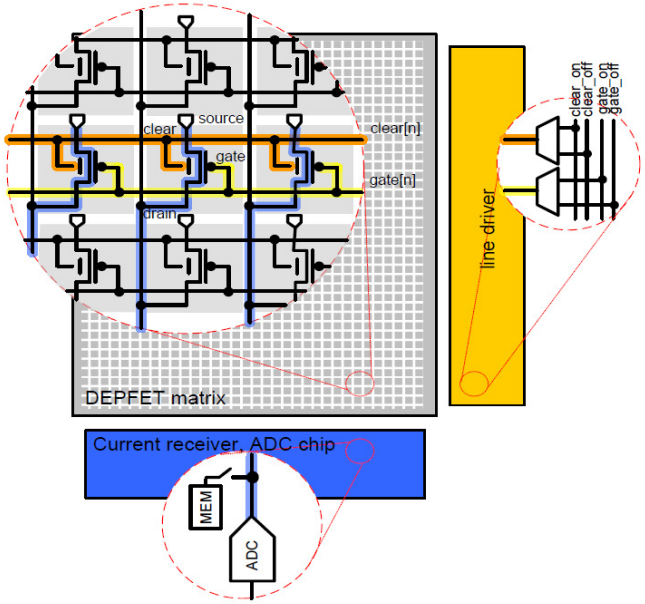
total 0.2% X_0

- 2 DEPFET layers (PXD)
- 4 Double Sided Si-Strip Detector layers (SVD)
- **PXD + SVD integration Nov. 2017**

DEPFET PXD	L1	L2
# ladders	8	12
Distance from IP (cm)	1.4	2.2
Sensitive thickness (µm)	75	75
#pixels/module	768x250	768x250
Total no. of pixels	3.072×10^6	4.608×10^6
Pixel size (µm^2)	55x50 60x50	70x50 85x50
Frame/row rate	50kHz/10MHz	50kHz/10MHz
Total sensitive Area (cm^2)	89.6	176.9

DEPFETs in a nutshell

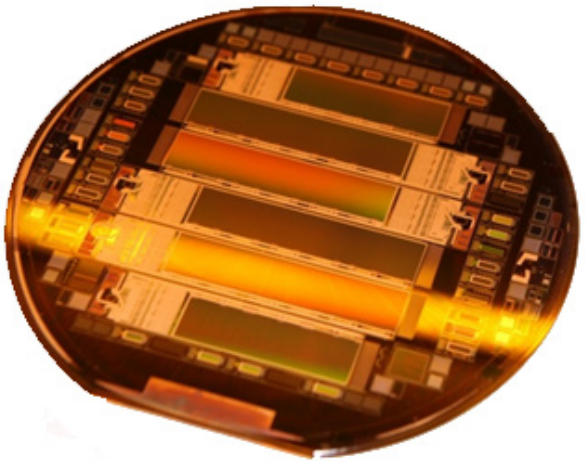


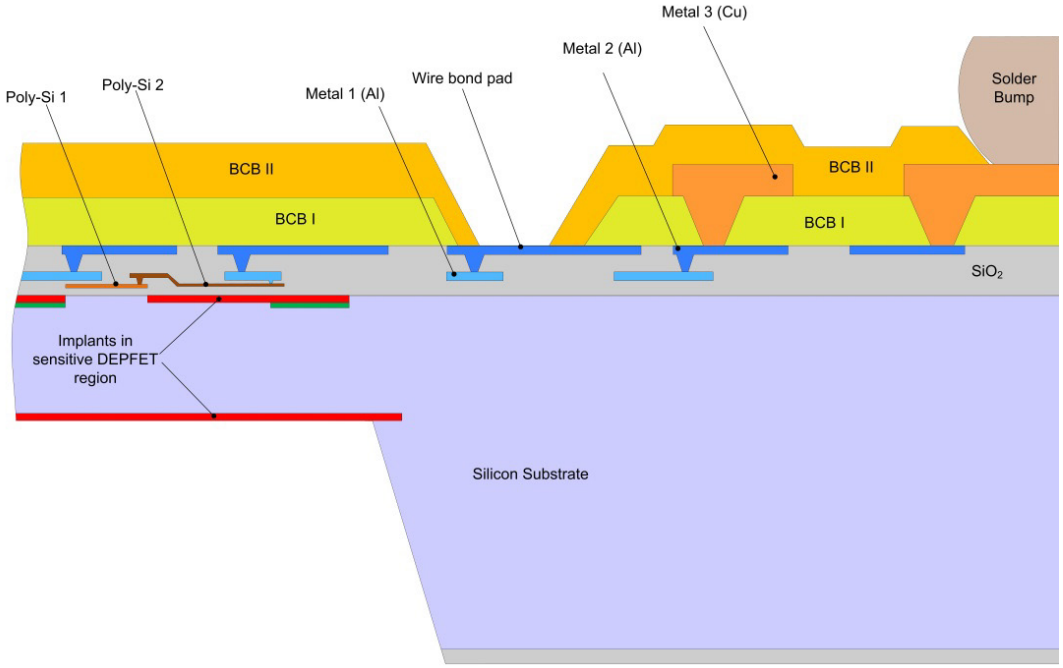


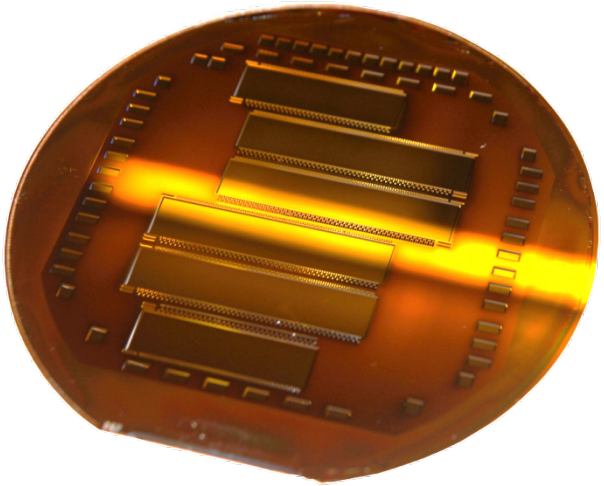
- **fully depleted sensitive volume**
  - fast signal rise time (~ns), small cluster size
- In-house fabrication at MPS Semiconductor Lab
  - **Wafer scale devices possible**
  - **Thinning to (almost) any desired thickness**
  - no stitching, 100% fill factor
- no charge transfer needed
  - faster read out
  - better radiation tolerance
- **Charge collection in "off" state, read out on demand**
  - potentially low power device
- **internal amplification**
  - charge-to-current conversion
  - r/o cap. independent of sensor thickness
  - **Good S/N for thin devices → ~40nA/µm for mip**

In-house MPG HLL DEPFET Sensor Production

- Starting material SOI wafer: 75µm top, 450µm support
- Production in three phases, 19 lithography steps
  - ↳ 9 implantations, 2 poly-silicon layers
  - ↳ 2 aluminum layers
  - ↳ last metal copper and thinning of sensitive area

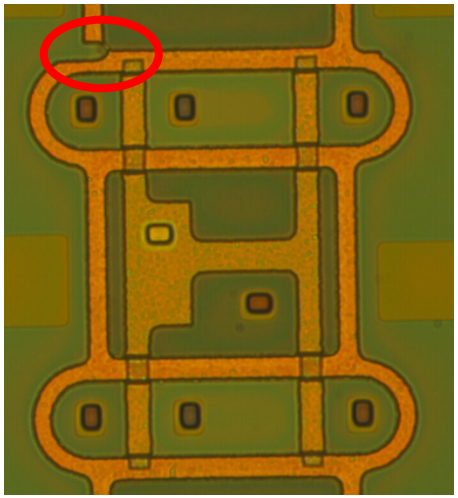


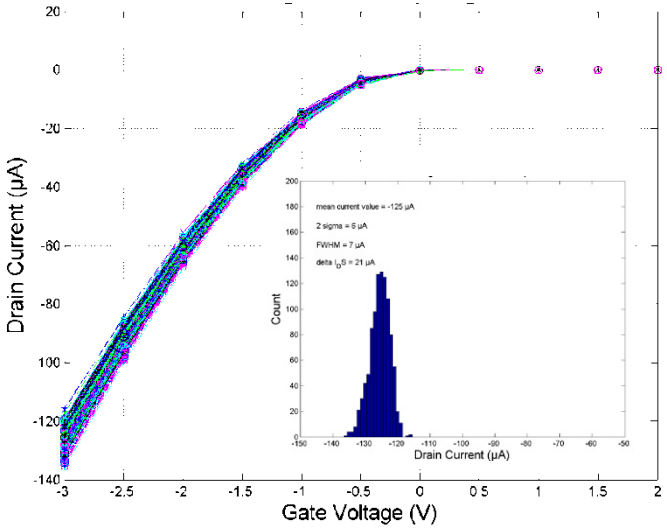


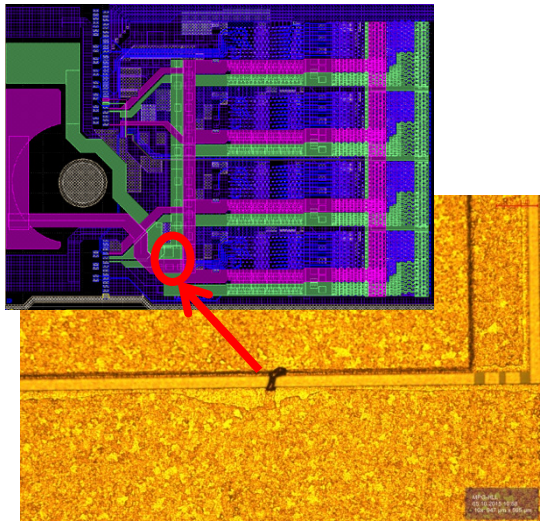


PXD Production Wafer-level QA Tests

- Test after phase I (Alu-1)
  - Manual probe headers used to bias poly-silicon and implant regions
  - Detect shorts which are lethal for module or individual rows
- Test after phase II (Alu-2)
  - Probe card + switching system to measure the DEPFET transistor characteristic of one row (1k pixel) and the integrity of the Drain line
- Test after phase III (Cu)
  - Flying probe station to check the integrity of the power supply, data and control lines







PXD Production Wafer-level QA Tests

- Percentage of live pixels

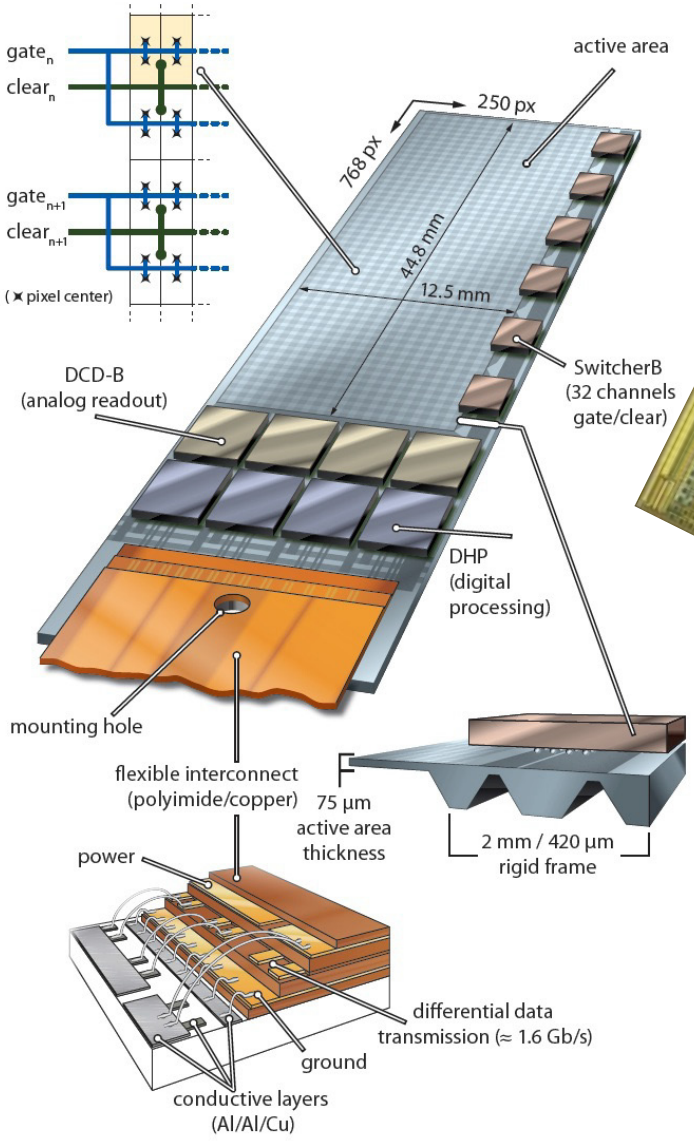
**failure due to operator error during testing*

	Pilot run			Pre-production			
	W30	W35	W36	**W31**	**W37**	**W38**	**W40**
IF	0*	98.44	98.96	98.8	98.4	98.8	100.0
OF1	100.00	98.44	98.96	99.0	98.1	0	99.5
OF2	99.48	98.96	99.48	99.0	0	0	99.3
OB1	97.72	99.40*	0	99.4	98.4	97.9	100.0
OB2	99.48	0	98.96	99.5	99.5	0	99.9
IB	97.92	0	99.48	100.0	99.0	99.0	100.0
Total	**83.3%**	**66.6%**	**83.3%**	**100%**	**83.3%**	**50%**	**100%**

- 34/42 (80.1%) working sensors
- 25/42 (59.5%) prime grade sensors (>99% pixels)
- 9/42 (21.4%) second grade sensors

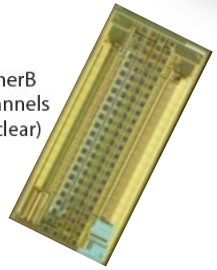
Main production of 22 wafers ongoing

PXD Module - Readout Electronics



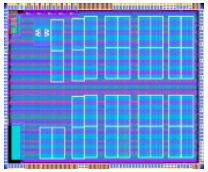
Low mass vertex detectors with highest possible integration!

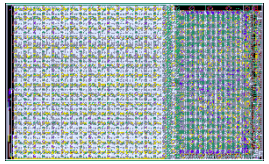
- Thin sensor area
- EOS for r/o ASICs
- Thin (perforated) frame with steering ASICS



SwitcherB - Row Control

- AMS/IBM HVCMOS 180 nm
- Size 3.6 × 1.5 mm^2
- Gate and Clear signal
- Fast HV ramp for Clear
- Rad. hard proved (36 Mrad)





DCDB - Drain Current Digitizer

Amplification and digitization of DEPFET signals.

- UMC 180 nm
- 256 input channels
- 8-bit ADC per channel
- 92 ns sampling time
- Rad. hard proved (10 Mrad)

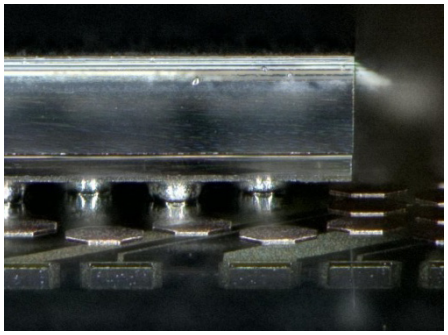
DHP - Data Handling Processor

- TSMC 65 nm
- Size 4.0 × 3.2 mm^2
- Stores raw data and pedestals
- Common mode and pedestal correction
- Data reduction (zero suppression)
- Timing and trigger control
- Rad. Hard proved (100 Mrad)

Module Assembly

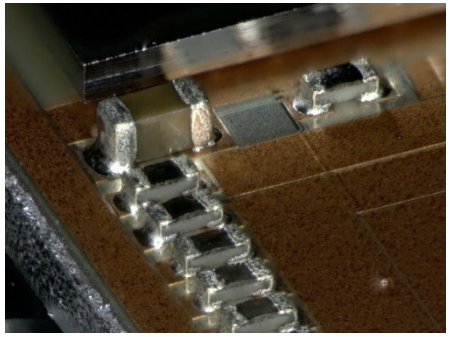
Flip Chip of ASICs (~240°C)

- Bumped ASICs have the same solder balls (SAC305)
  - DHP bumping at TSMC, DCDB bumping via Europractice
  - SWB bumping on chip level
- Flip Chip of PXD modules at IZM Berlin



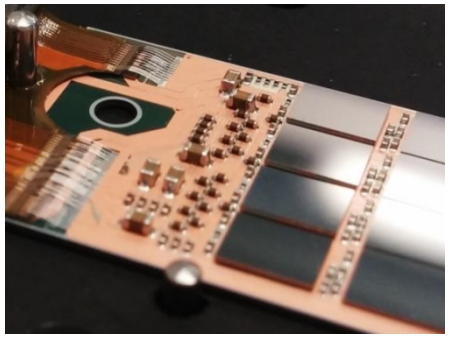
SMD placement (~200°C)

- Passive components (termination resistors, decoupling caps)
- Dispense solder paste/jetting of solder balls, pick, place and reflow
  - PbSn 37/63 solder

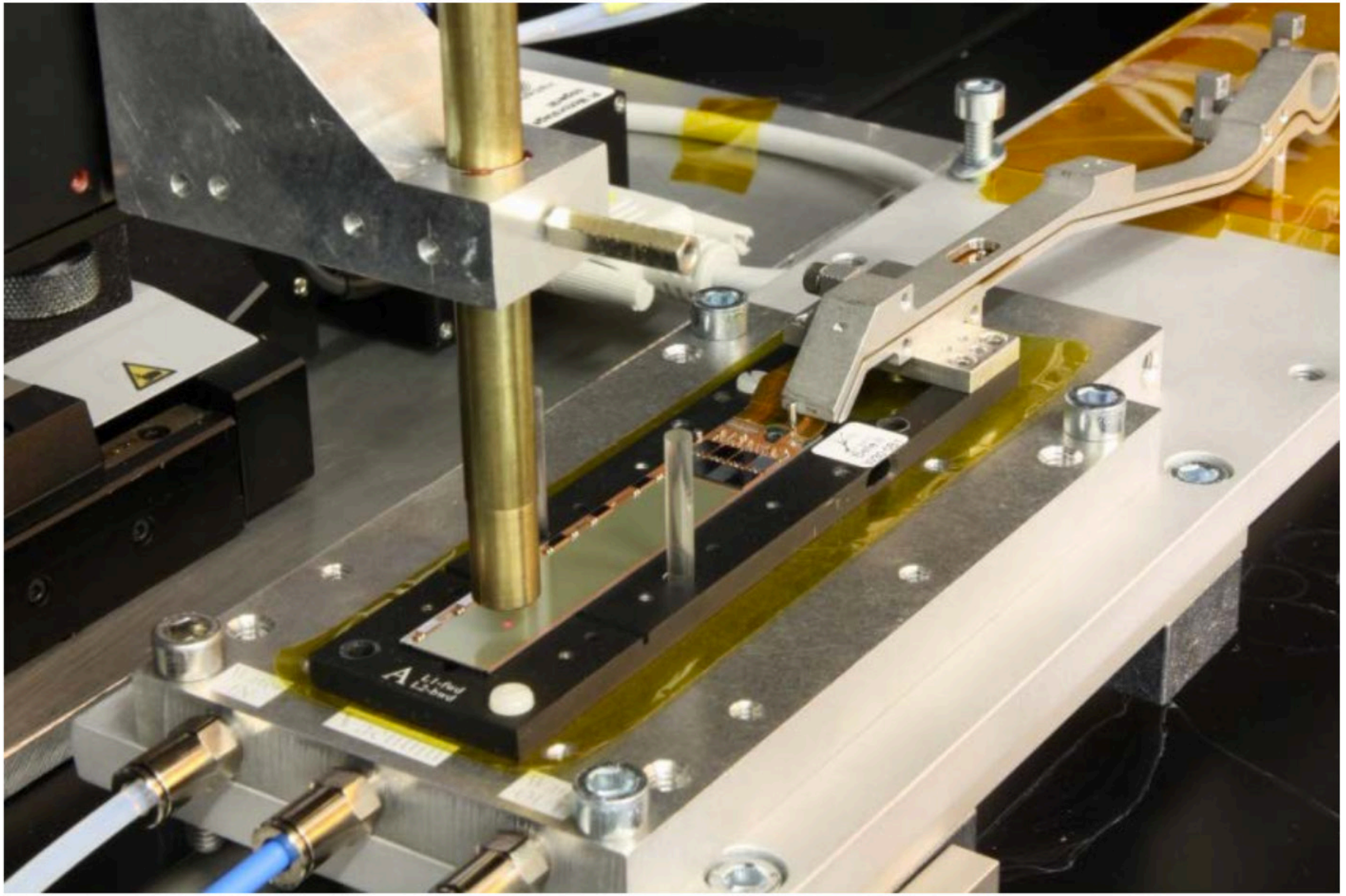


Kapton attachment (~170°C), wire bonding

- Solder paste printing on kapton,
  - SnBi solder
- Wire-bond, wedge-wedge, 32 µm Al bond wires

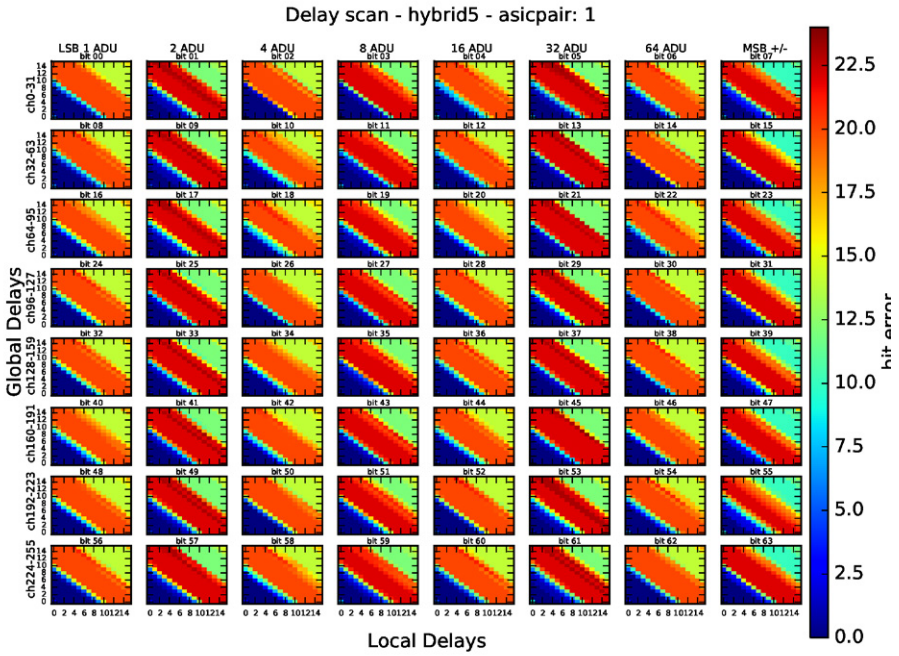


PXD Module Test

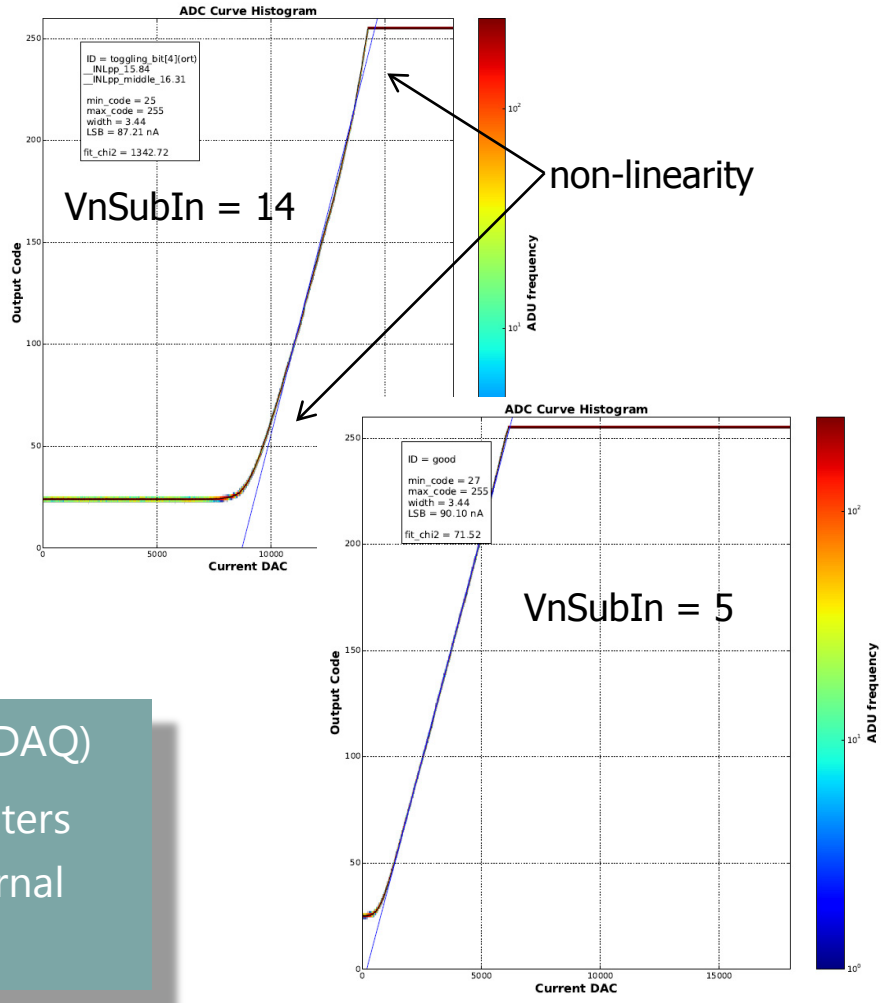


ASIC Parameter Optimization

Error free DCD-DHP communication



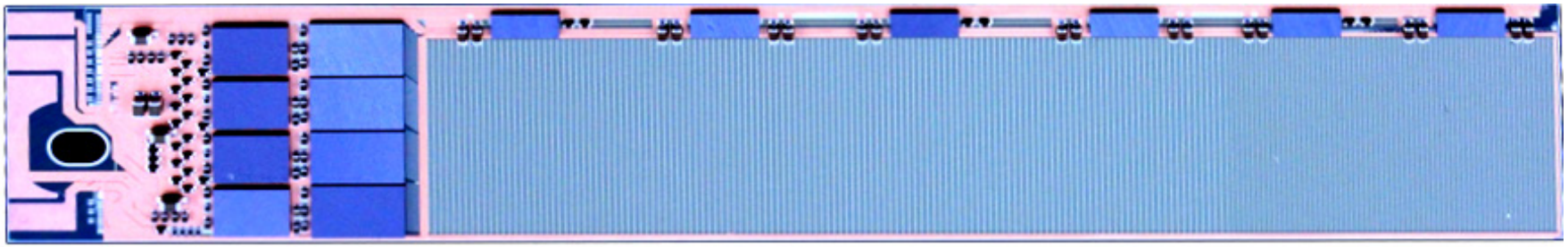
ADC Transfer Curve



- Lab framework and PC-based DAQ (BonnDAQ)
- Script-based optimization of ASIC parameters e.g. DHP input delay elements, DCDB internal current source

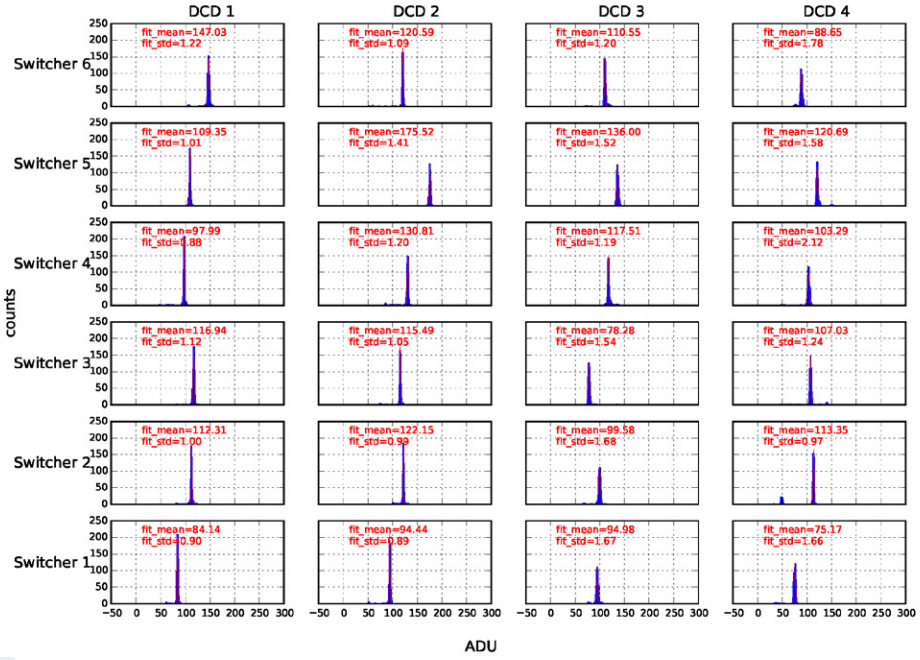
PXD Module Test

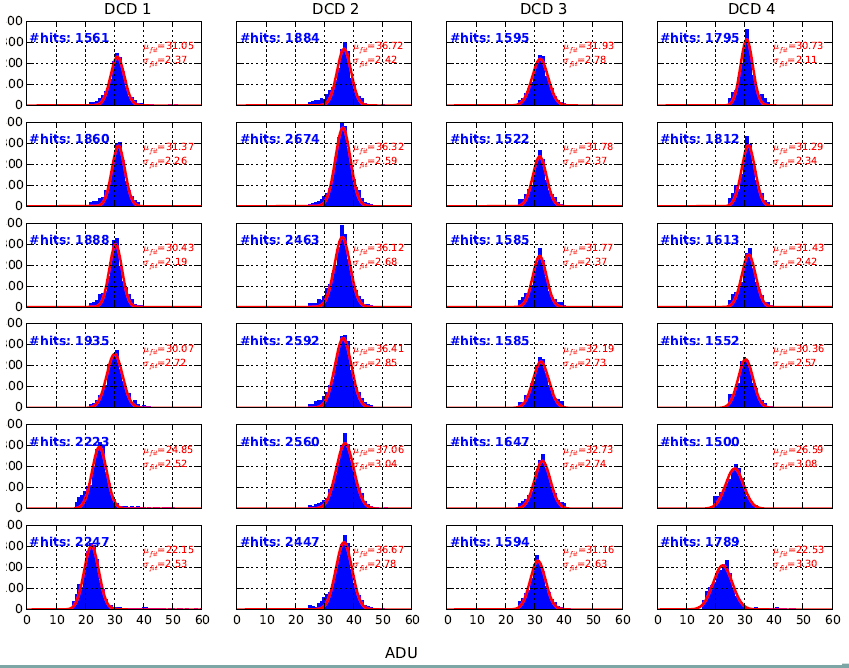
distance between mask and sensor ~4 mm



Laser signal ~2-4mip,
read out at full speed (105ns/row)

^{109}Cd Source measurement – 250MHz
Non optimal sensor settings **S/N>30**





PXD Module Test

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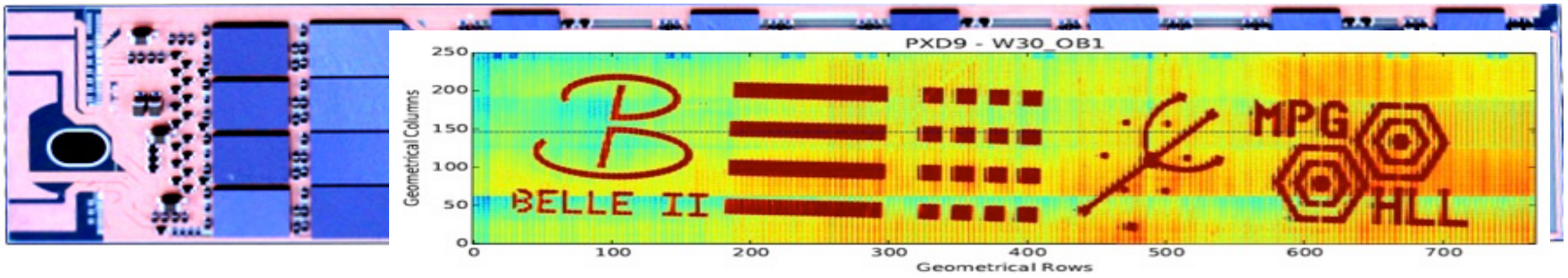

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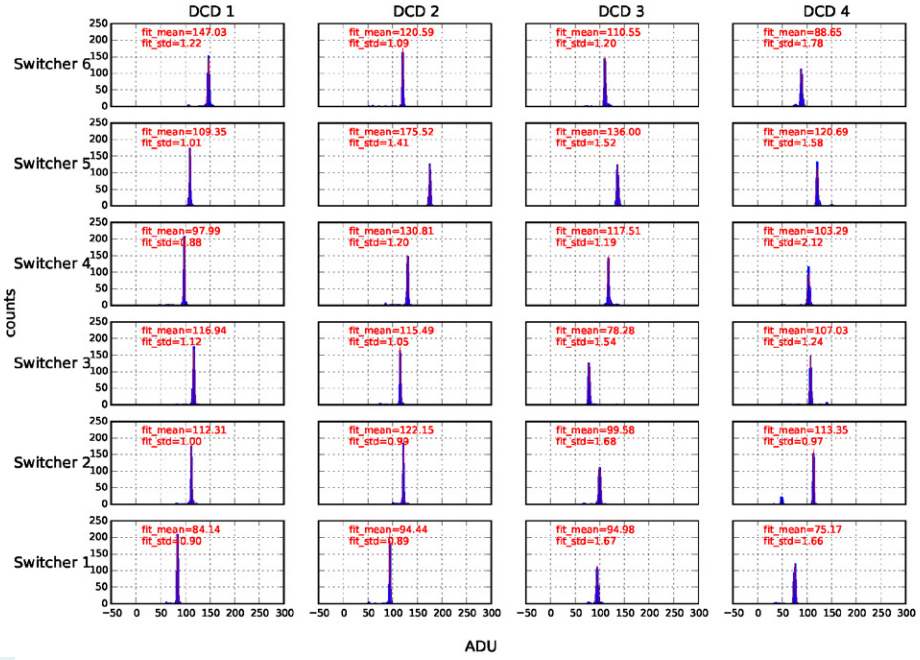
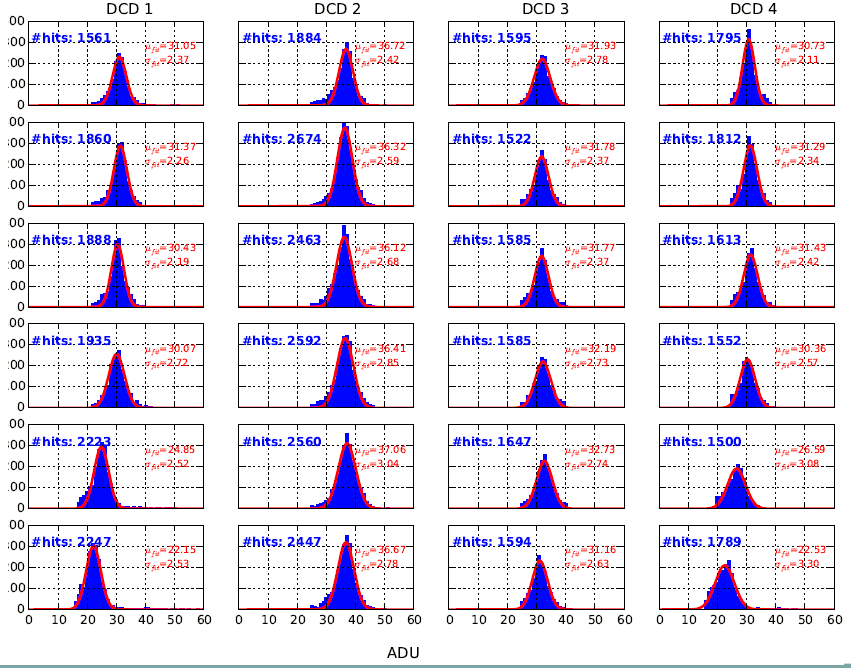
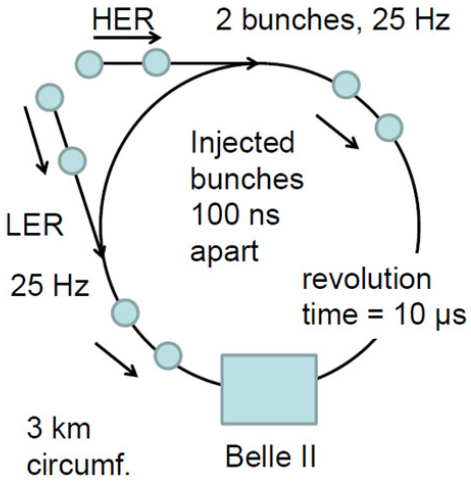
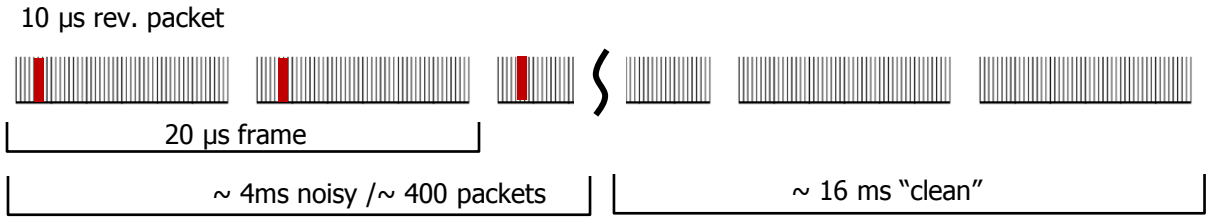




SuperKEKB Injection Scheme – Need of Electronic Shutter



10µs packets with 2503 bunches , 200 ns gap in-between (TDR)



- continuous injection → ~ 400 revolutions with two noisy bunches (100ns apart) every 20 ms
- DEPFET integrates two trains, these noisy bunches would blank the frames → 20% loss of data

- the best solution: gate the DEPFET during the passage of the noisy bunches
- ~100ns gate, with some rise and fall times, twice per frame → 2x2µs of 20 µs blind
- assuming 4 ms relaxation time (not clear), ~200 consecutive frames with gate cycles

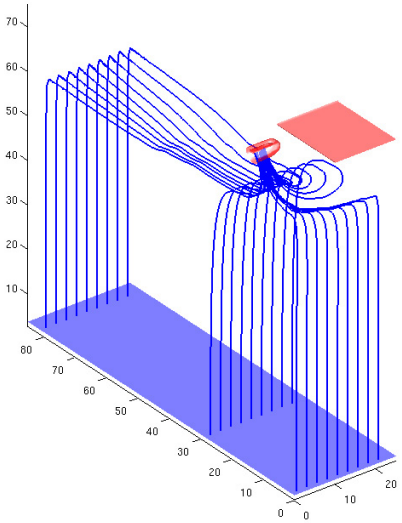
- DEPFET operation mode during gating: DEPFET off, Clear active (Vgs=3 .. 5V, Vclear=16 .. 20V)

DEPFET Gated Mode Operation

Switching to gated mode:

» DHE receives signal from acc., sends "veto" → DHPT switches to gated sequence → controls Switcher

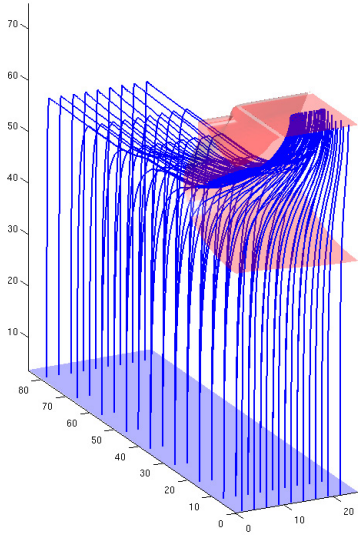
» DCD operation mode remains untouched



Normal charge collection

» Vgs=4V, Vclear=5V

» all signal charge collected in internal gate



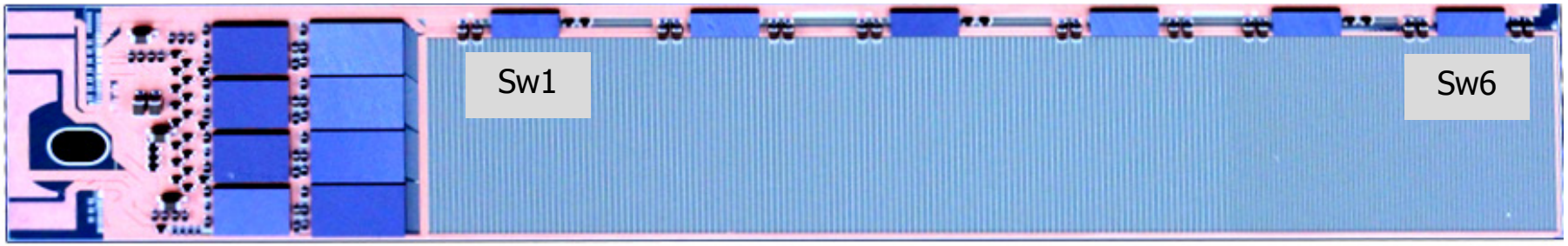
Gated mode

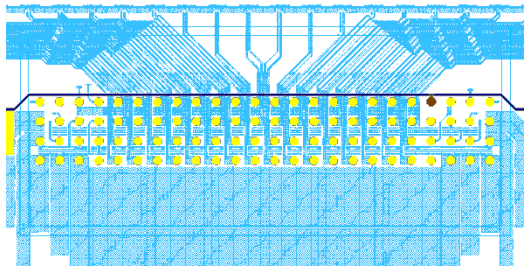
» Vgs=4V, Vclear=20V

» all signal charge dumped to *Clear*

Challenge: switch all *Clear* contacts in the matrix from ~5V → ~20V
shown on small matrix, but as expected, it's more difficult on large modules

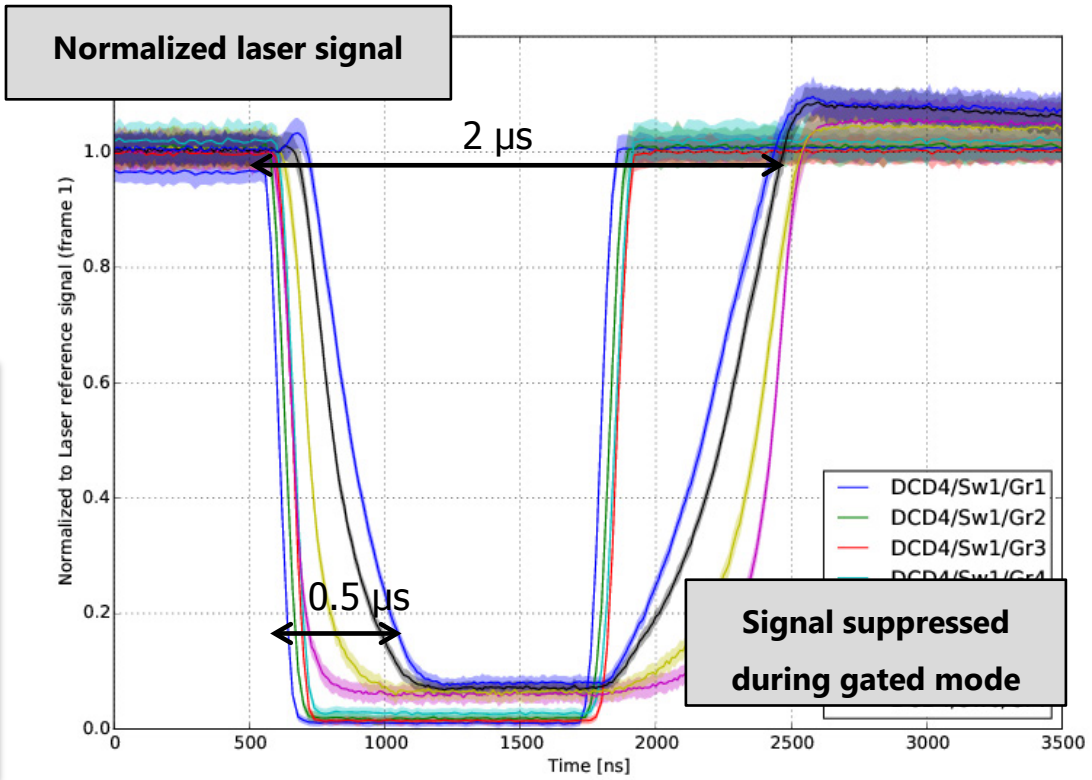
DEPFET Gated Mode Operation





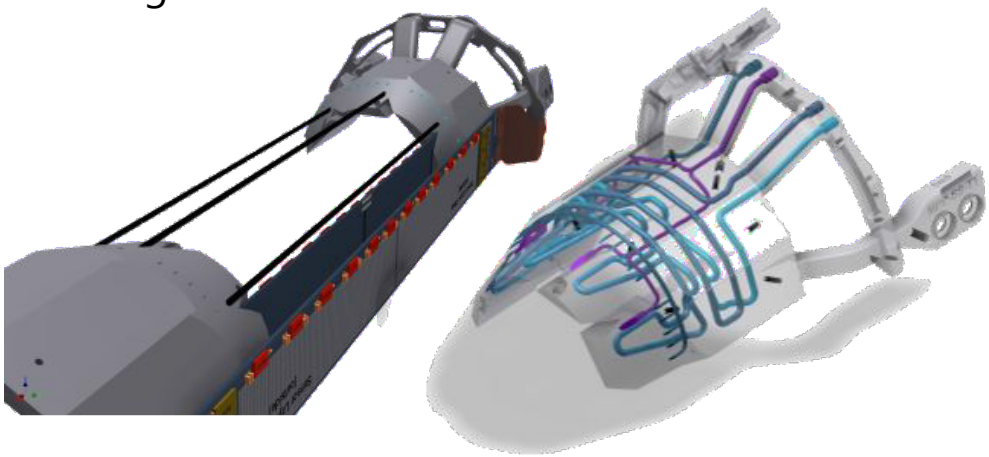
V_Substrate line

- Measurements on PXD pilot modules revealed too small trace width of Switcher V_Substrate
- Could be changed for the PXD production



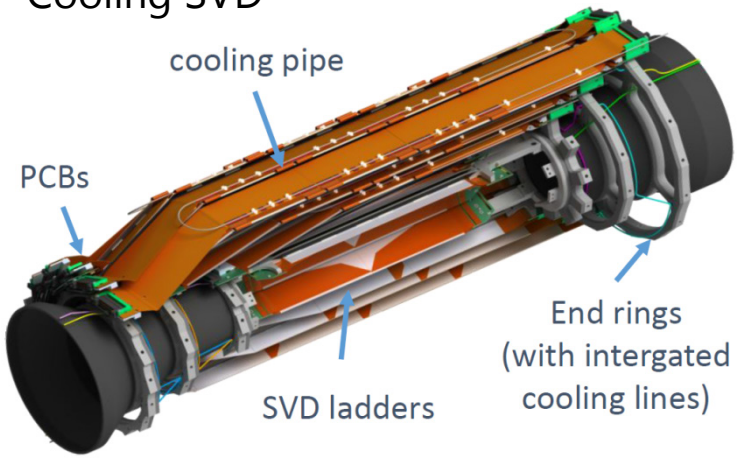
VXD Cooling System

Cooling PXD



Support Cooling Block (SCB), manufactured using 3D printing technology, with CO2 and N2 channels inside

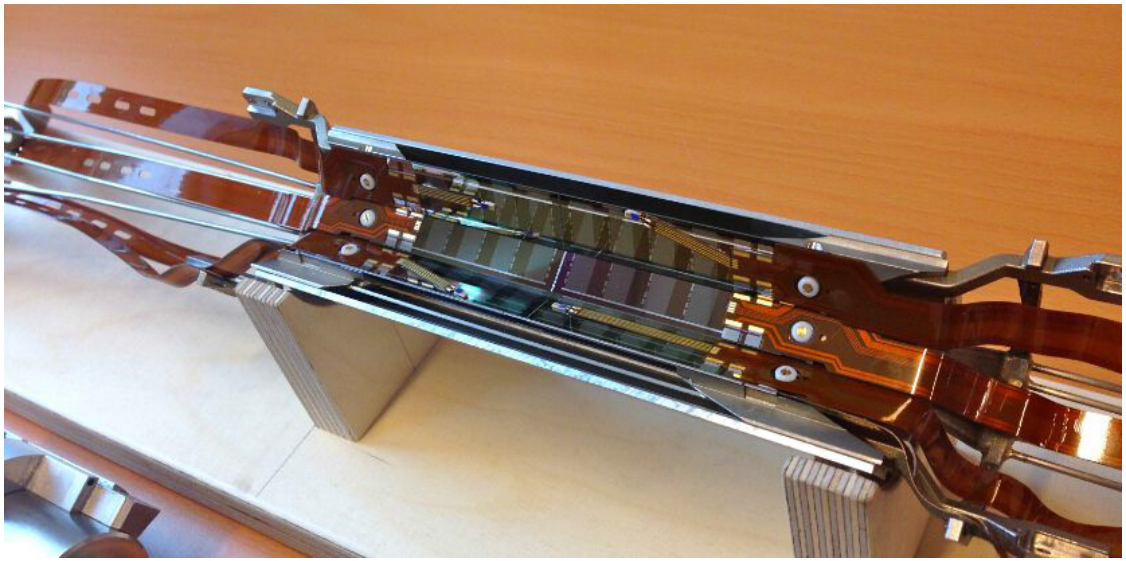
Cooling SVD

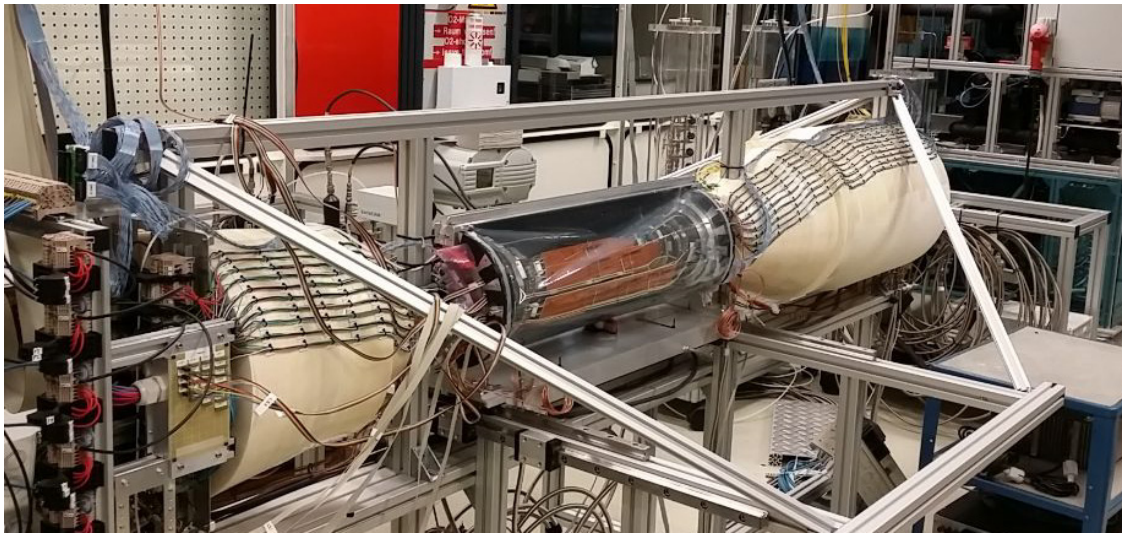


Requirements

- PXD: Sensor < 25 °C to minimize shot noise due to leakage current; ASICs < 50 °C to avoid risk of electro-migration
- SVD: APV25 readout chips surface@~0 °C for SNR improvement
- Power consumption: PXD 360W; SVD 700W, together with the heat load through 9m of vacuum isolated flex lines; required cooling capacity of 2-3kW
- VXD needs to be thermally isolated against CDC and beam pipe. Room temperature at the inner surface of CDC is required for stable calibration and dE/dx performance
- IBBelle CO2 cooling plant in collaboration with CERN (currently shipped to Japan)

VXD Thermal Mockup



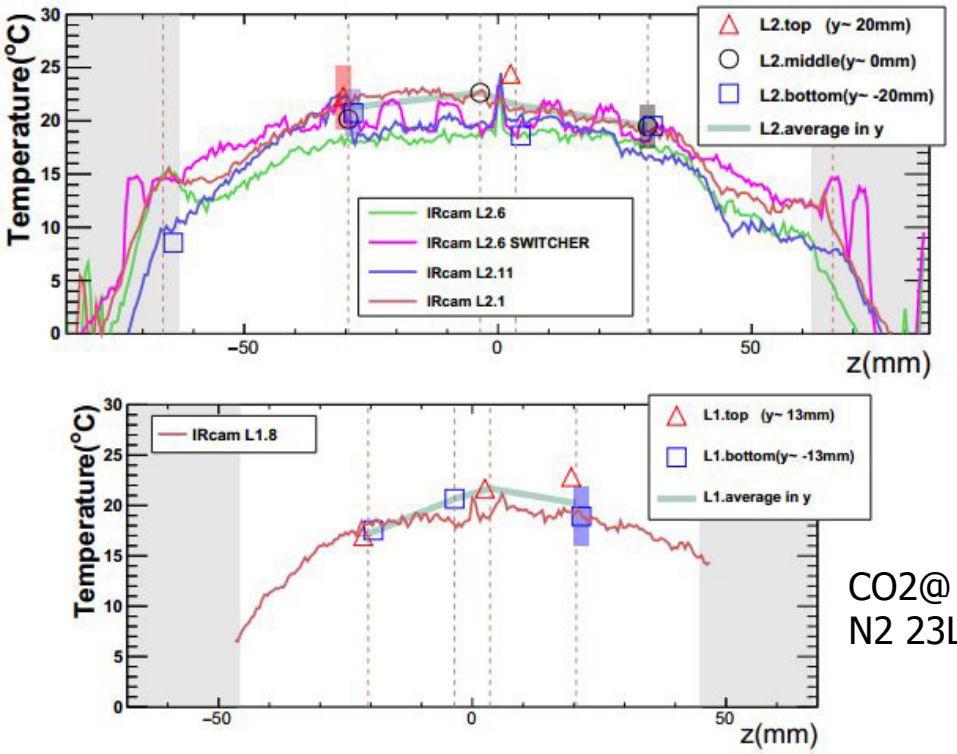


- 75µm thin Si-substrates with Belle II geometry
- Glued at the narrow edge + ceramic insert to get ladders
- Resistors integrated on Si-substrates to simulate the power distribution
- Additional power of 25 W is given on the kapton cables to simulate their power dissipation
- Thermal mock-up consist of 2-layer PXD and 4-layer SVD (half of L.6 cooling pipes are under preparation)

Temperature on PXD

- Thermal and mechanical measurements to PXD have been finished. Maximum temperature along the sensor is around **20 °C in VXD volume**

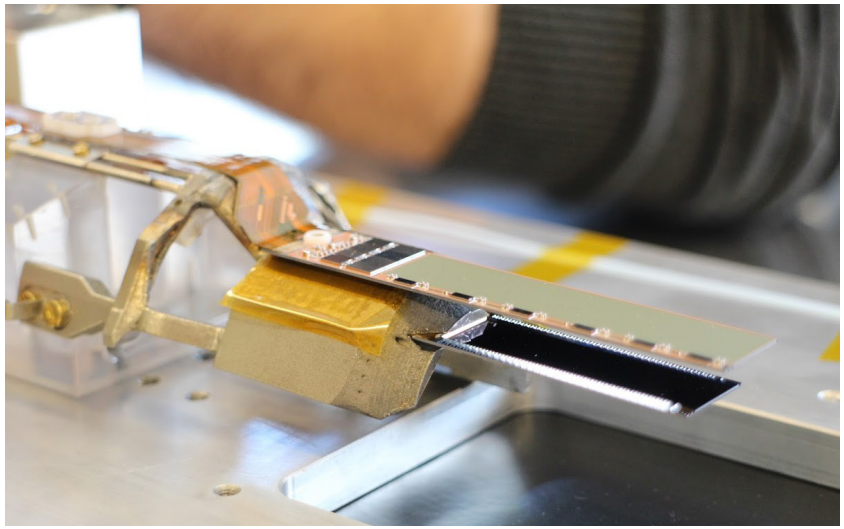
H. Ye, Thermal mock-up studies of the DEPFET pixel vertex detector for Belle II, submitted to Nucl. Instrum. Meth. A, arXiv:1607.00663

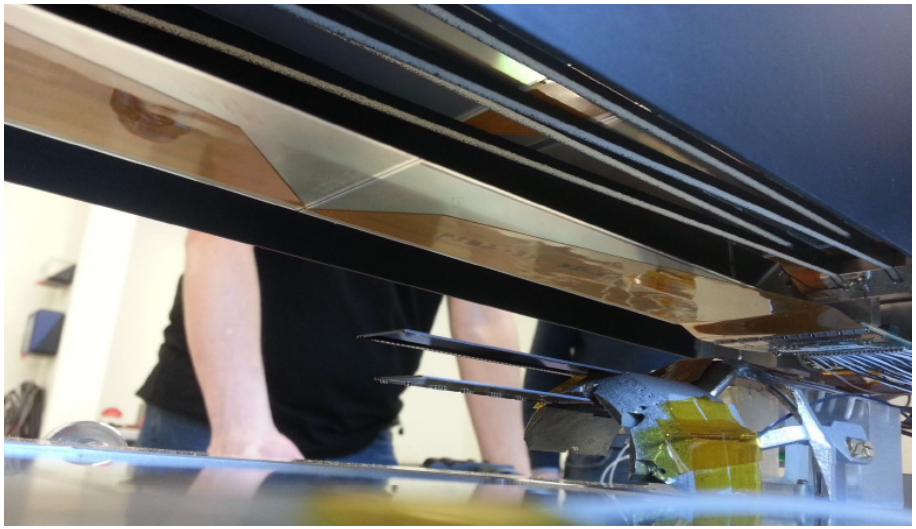


CO2@ -30°C;
N2 23L/min

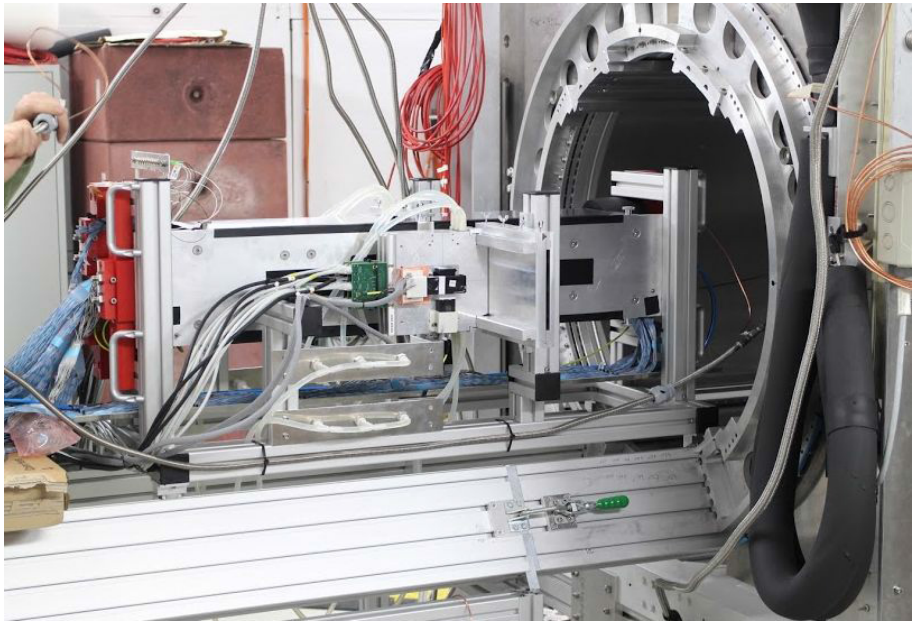
Figure 5: The temperature distribution of PXD ladders along the z-direction. BW(FW) is on the left(right) side. The gray areas indicate the regions of DCD/DHP, while the 75μm thick sensitive area is shown in the center. The thick solid line indicates the averaged temperature along z-direction measured from the Pt100s. Different markers show the average temperature in y-direction at certain position along z-axis, the error bar on the marker represents the temperature range in x-direction. Thin solid lines show the temperature distribution measured by the IR camera on selected ladders.

PXD + SVD Combined Beam Test @ DESY



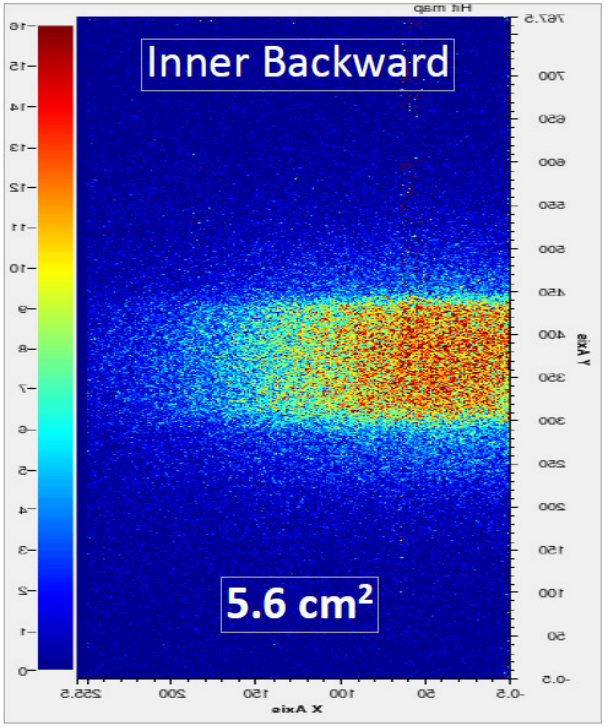


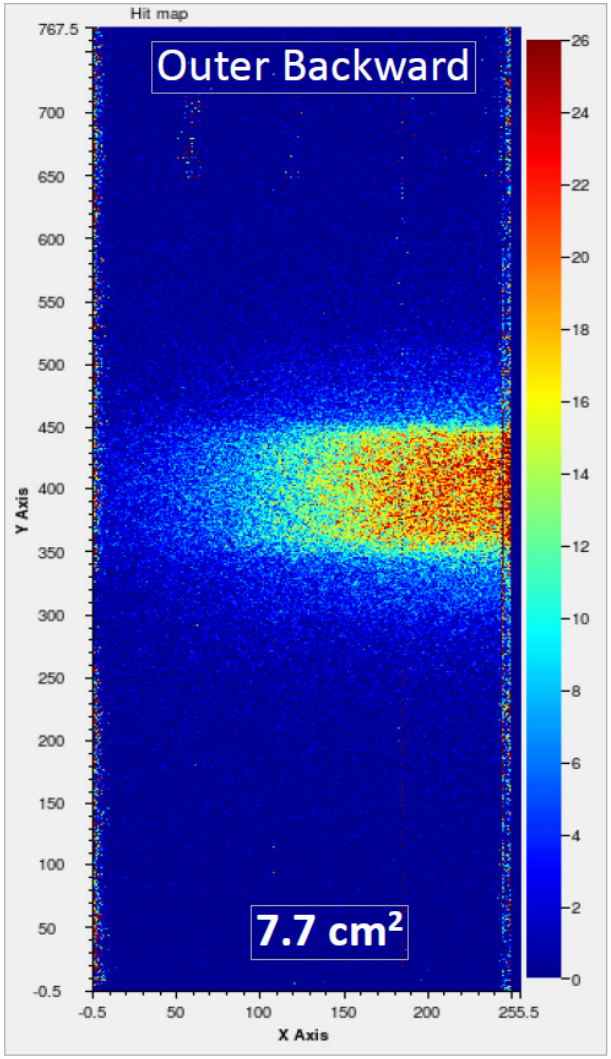
- Combined beam test PXD+SVD
- Illumination with (up to) 6 GeV e- under solenoid magnetic field (PCMAG)
- Full readout chain (40kHz frame rate)
- Beast II geometry
- CO2 cooling, slow control, environmental sensors
- Total of ~340 runs in 4 weeks



PXD Hit Maps

Threshold = 5 (~1200 electrons)

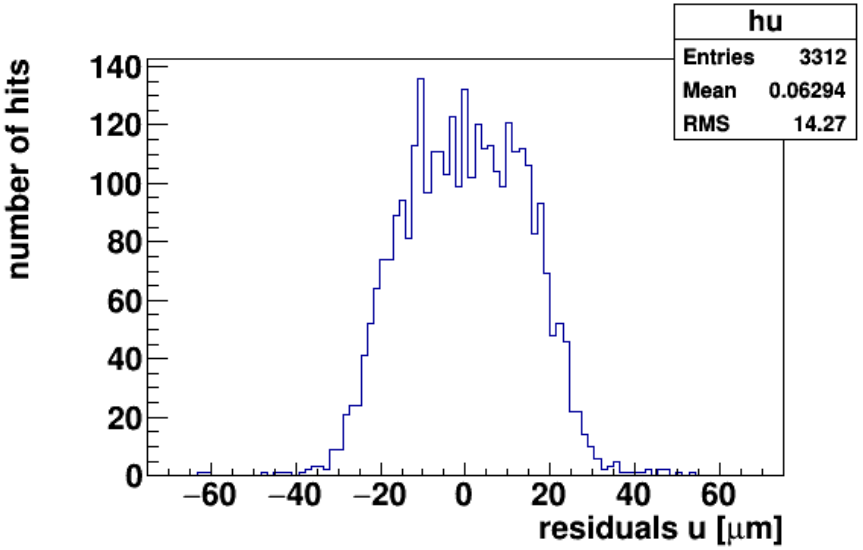


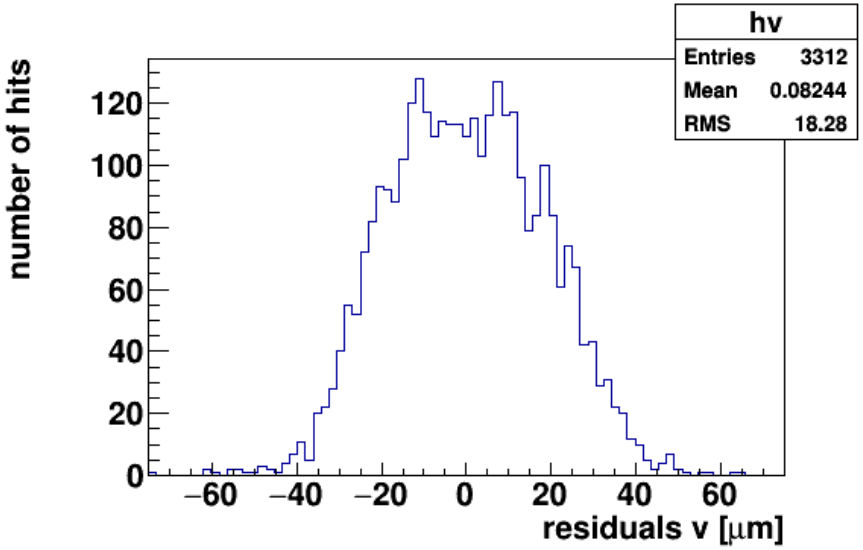


Both detectors fully functional. Only a few ø(20) pixels masked

Trigger on 4 scintillators Collimated beam No magnetic field

PXD Residuals



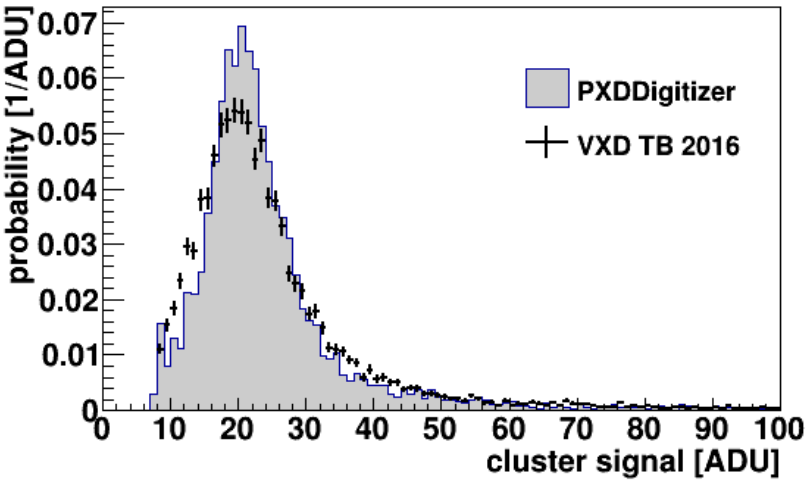


Residuals for perpendicular incident MIPs

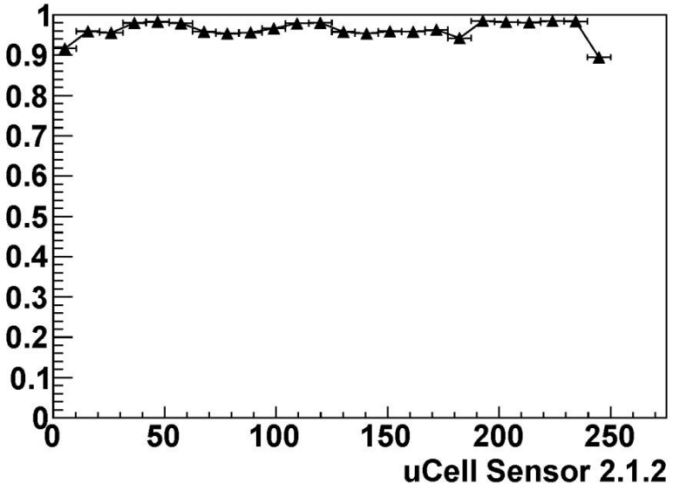
- 14 µm (50 µm pitch)
- 18 µm (60 µm pitch)
- Measured residuals very close to digital resolution
- Spatial resolution of perp. tracks is worst case (small charge sharing → small clusters)

PXDDigitizer in Belle II Software Framework and Efficiency

PXDDigitizer in basf2 vs. TB data



Efficiency >95%



Combined PXD-SVD Beam Test

- 2 PXD layers fully operational
- Sensor with homogeneous response
- Hit maps as expected in both layers
- SNR OK
- PXD residuals according to specs
- VXD correlations (mapping and timing)
- Efficiency >95%
- Operation under realistic environmental conditions (CO2 @ -27 °C)

Summary and Outlook

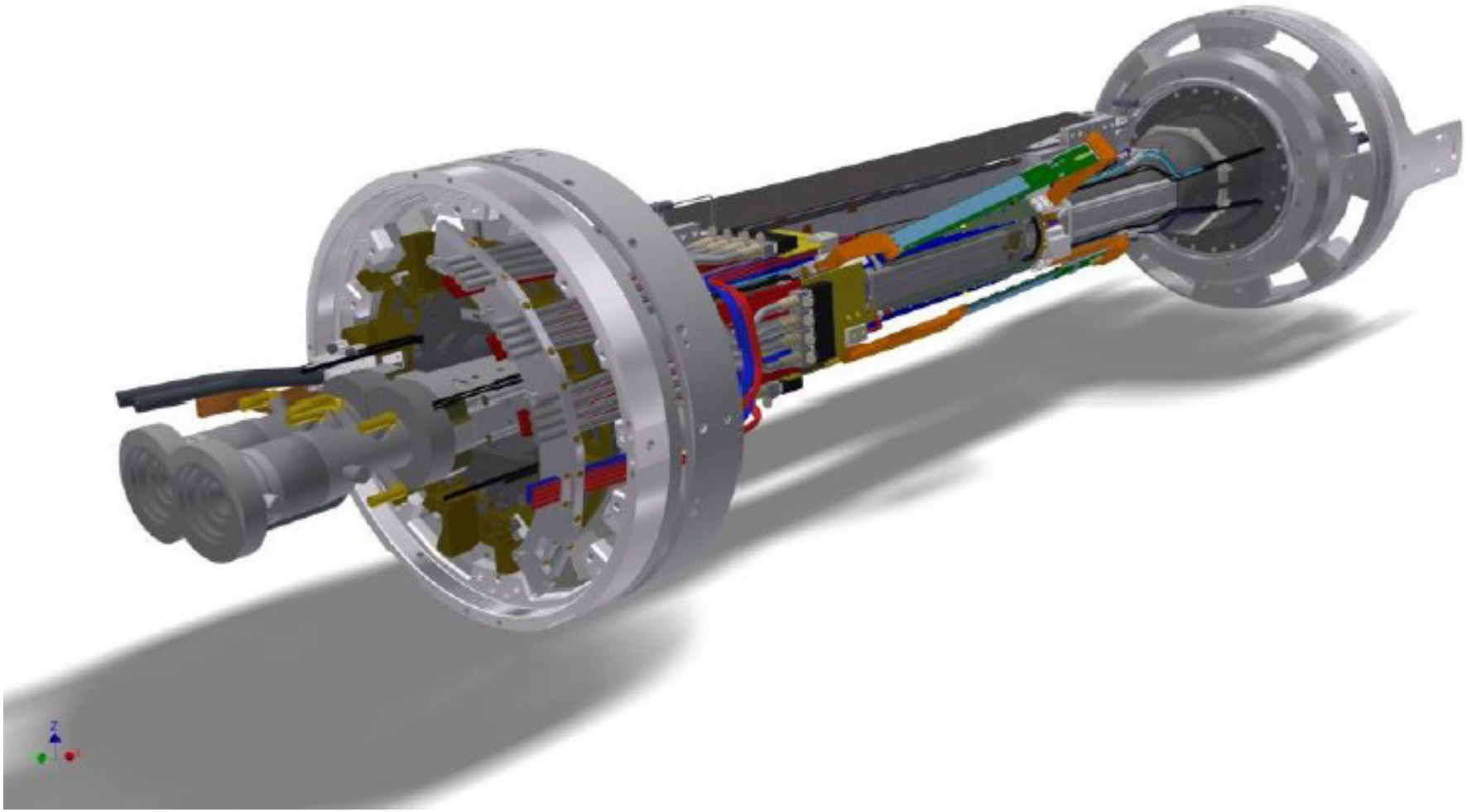
Belle II PXD takes shape

- Integration of the phase II PXD (2-layers) at DESY in **November 2016**
- Installation phase II detector @ KEK in **summer 2017**
- Production of the phase III detector is ongoing
- Integration and test of PXD half-shells @ DESY in **spring 2017**
- **Transport PXD to KEK October 2017**

Further reading: CERN Courier September 2016

Thank you for your attention!

Phase 2 Integration Campaign



PXD9 Sensor Production: 29 Wafers

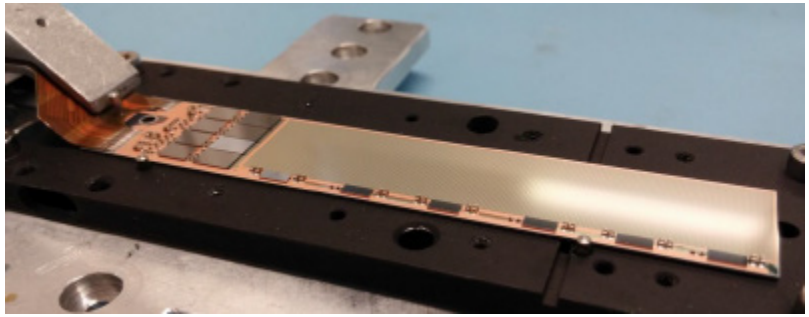
- PXD9-6: 3 wafers pilot run First module assembly, DESY test, gated mode tests

- PXD9-7: 4 wafers pre-production Lessons from pilot run incorporated (improved periphery routing)
- Modules for Beast2, module pre-production ….

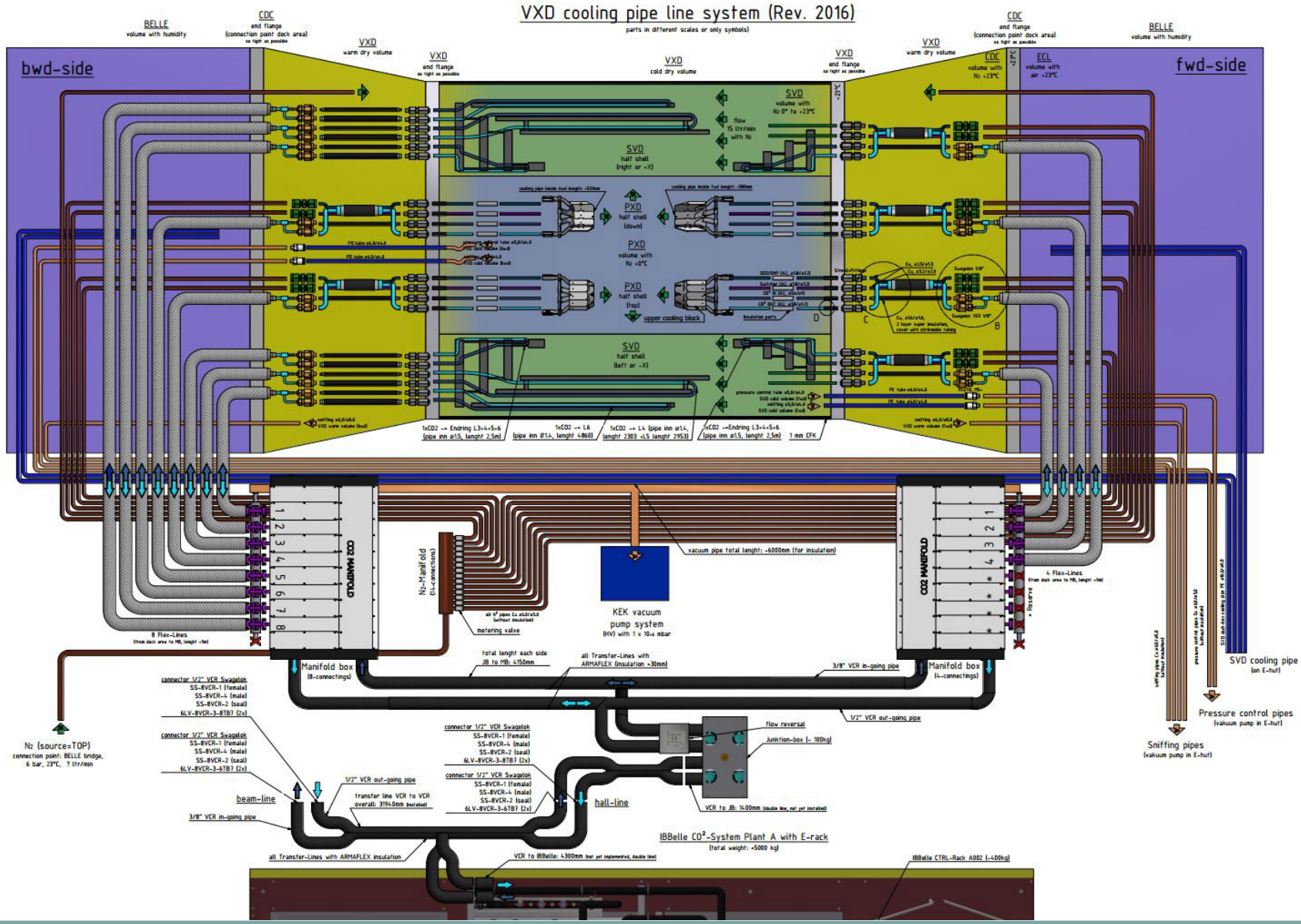
- PXD9-8: 9 wafers, main production I Final modules
- Status: Phase II - Metal 1 structuring finished, first electrical measurements ongoing

- PXD9-9: 6 wafers, main production II Final modules
- Status: Phase II - Metal 1 lithography ongoing

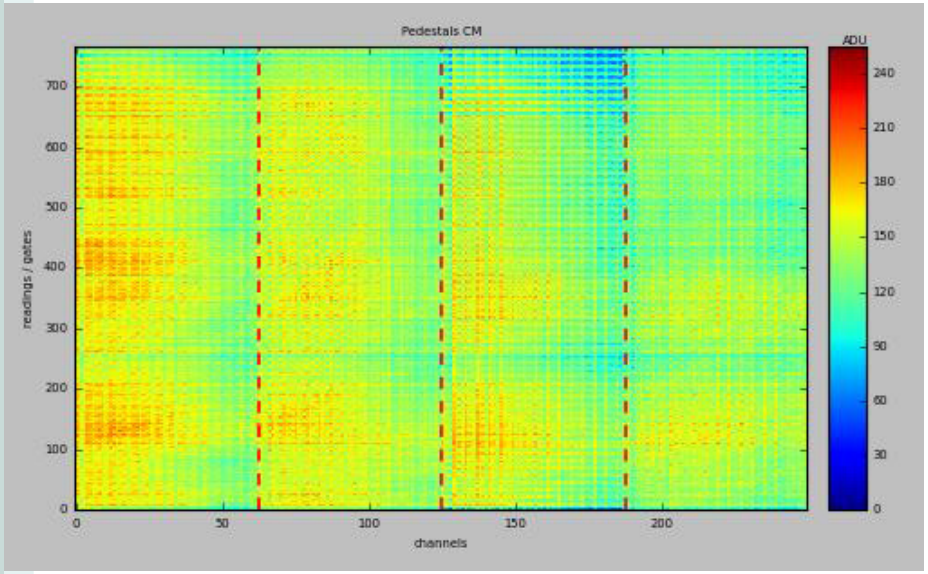
- PXD9-10: 7 wafers, contingency… Status: Phase I finished - in stand-by before Phase II



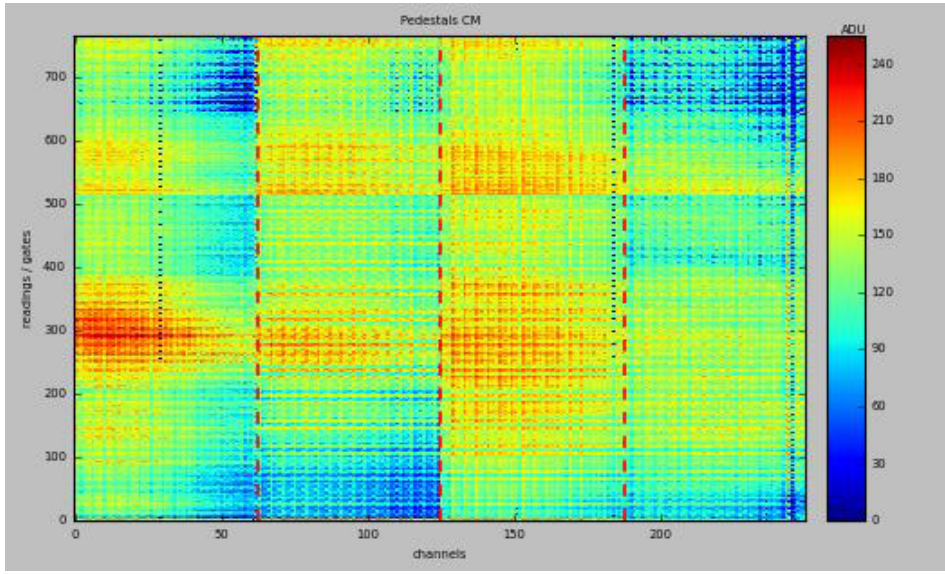
Belle II VXD Cooling Pipe Line System



PXD Pedestal Distributions

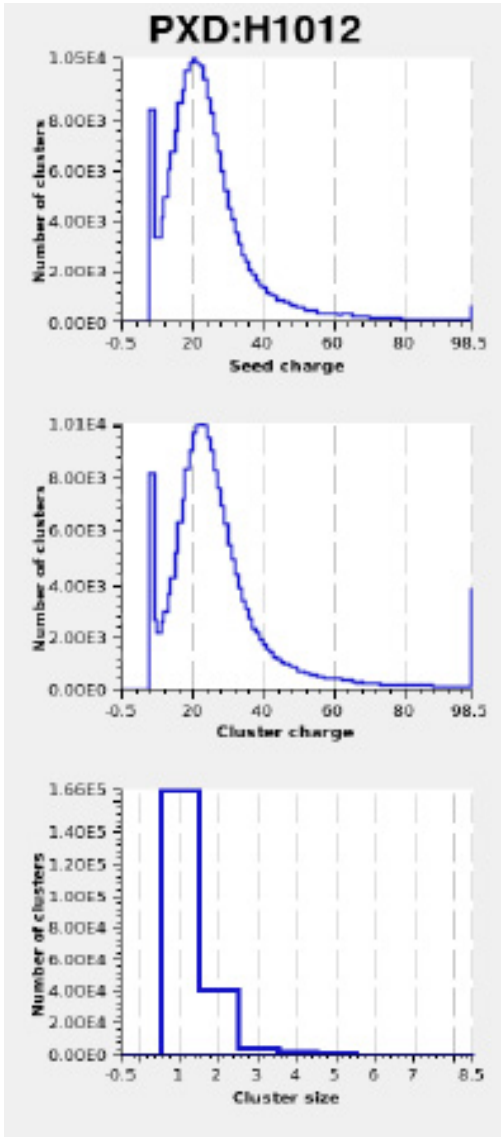


Inner Layer

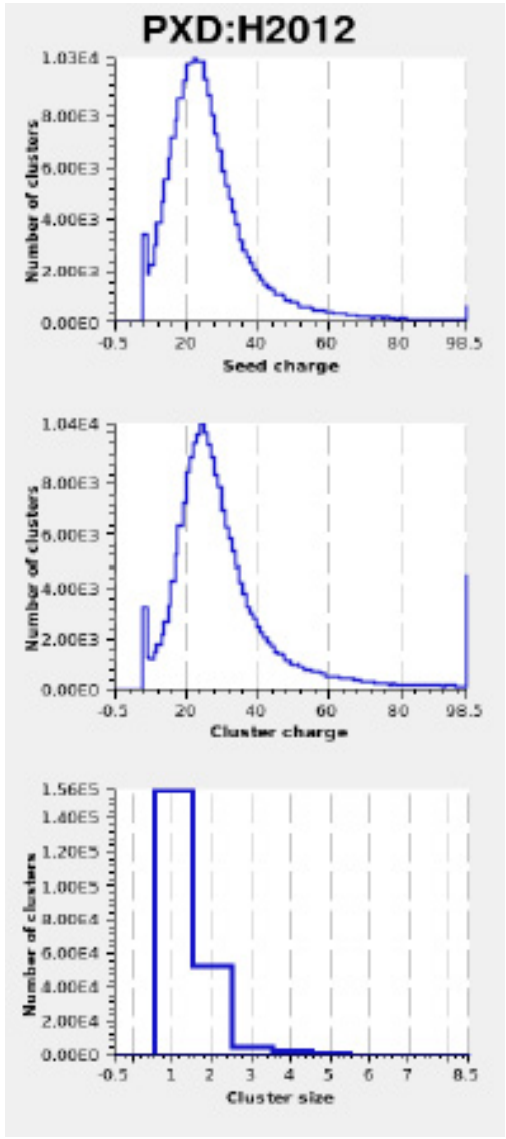


Outer Layer

ll ASICs operational
All regions within the DCD dynamic range



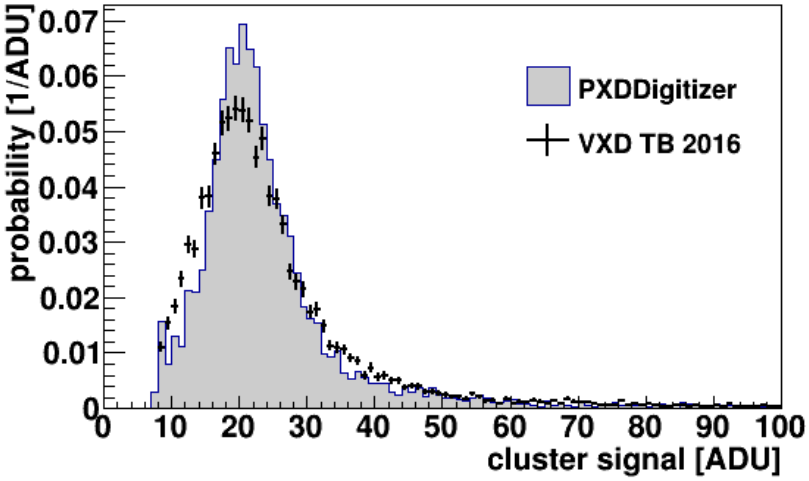
SNR ~ 32 for perpendicular incident MIPs

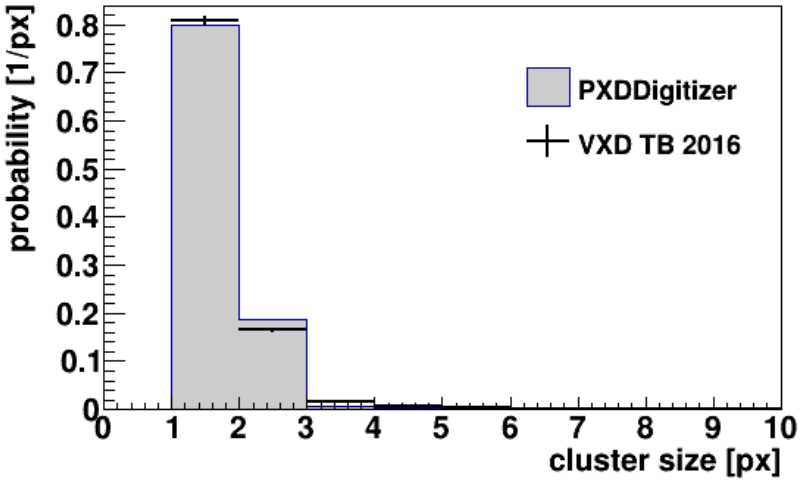


Inner Layer

Outer Layer

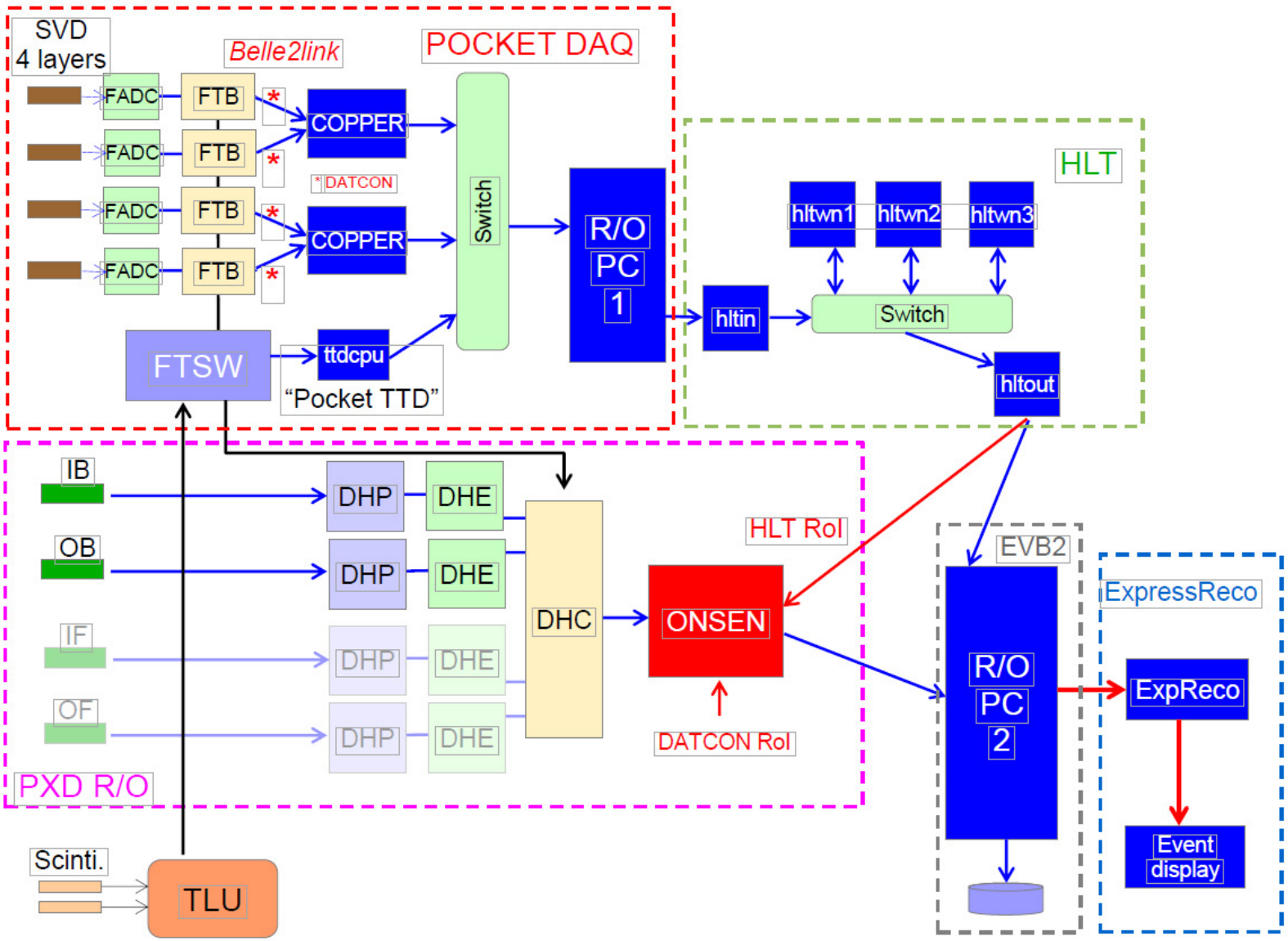
PXDDigitizer in basf2



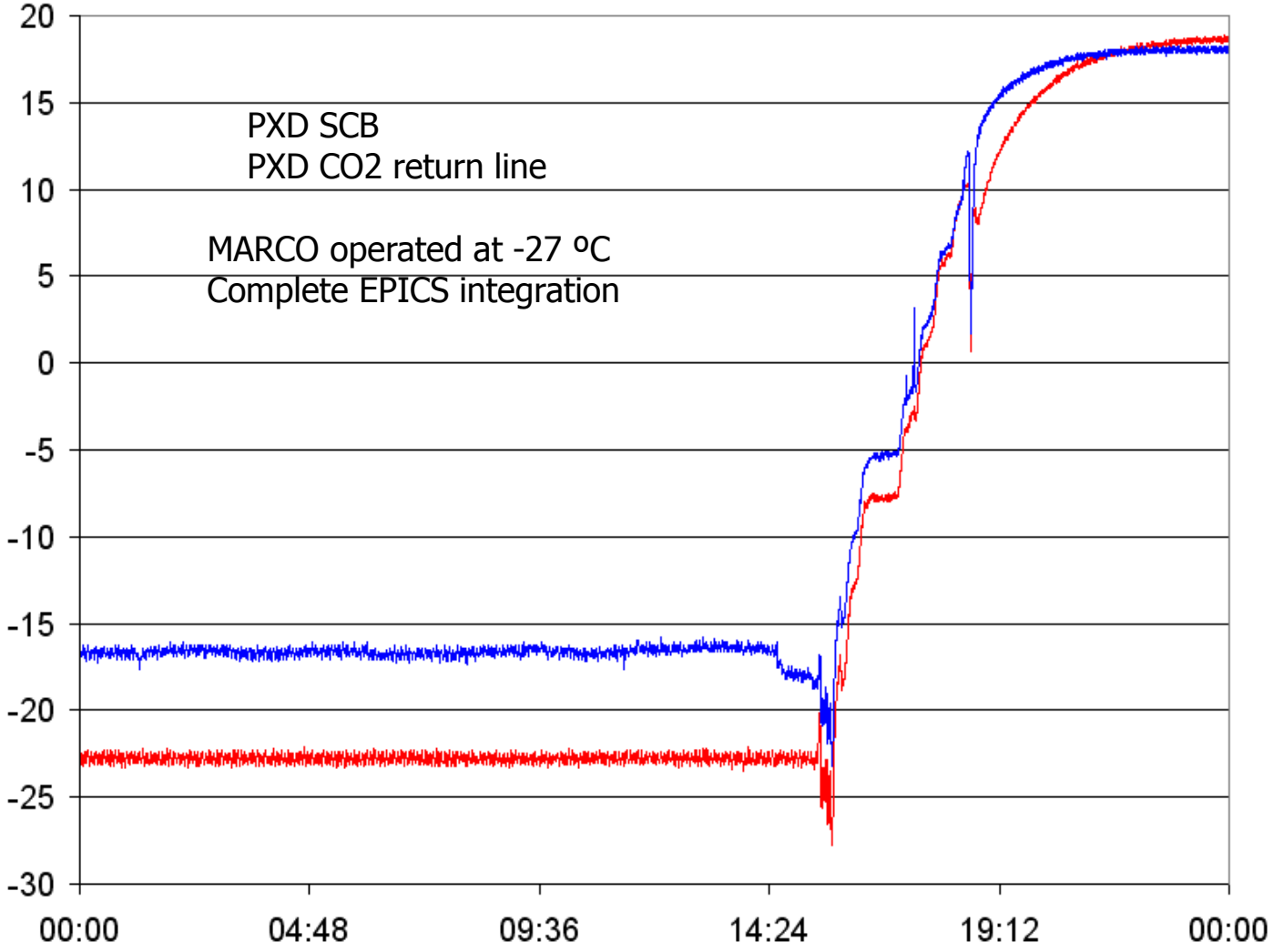


- PXD inner half-ladder in run 329
- after masking faulty pixels
- PXD simulation done using
  - Gq is 500pA/e
  - LSB ~130nA (low gain)
  - hit threshold 7ADU
  - rate of noise hits <5E-8
- Signal non uniformity in real sensor not
- accounted in simulation.
- threshold of 7 cuts a bit into the signal (→ can explain some efficiency loss)
- Cluster size agrees well with simulation

VXD-Test Beam DAQ Structure

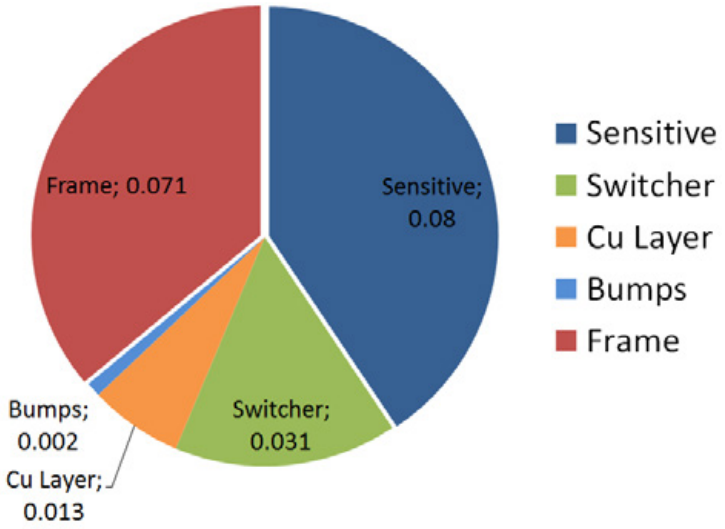


PXD Environmental Monitoring

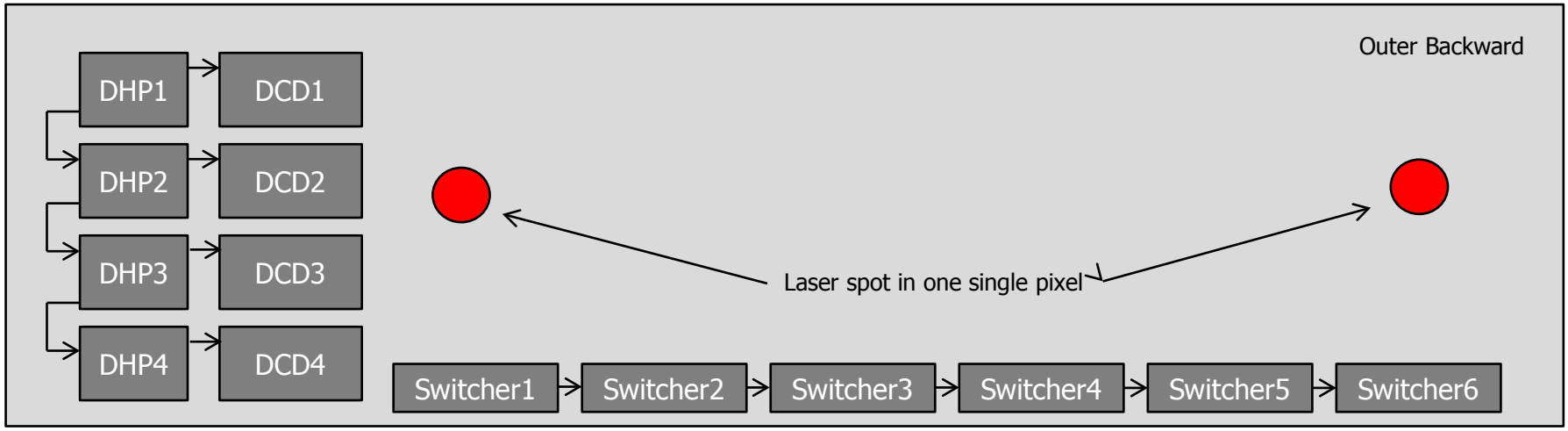


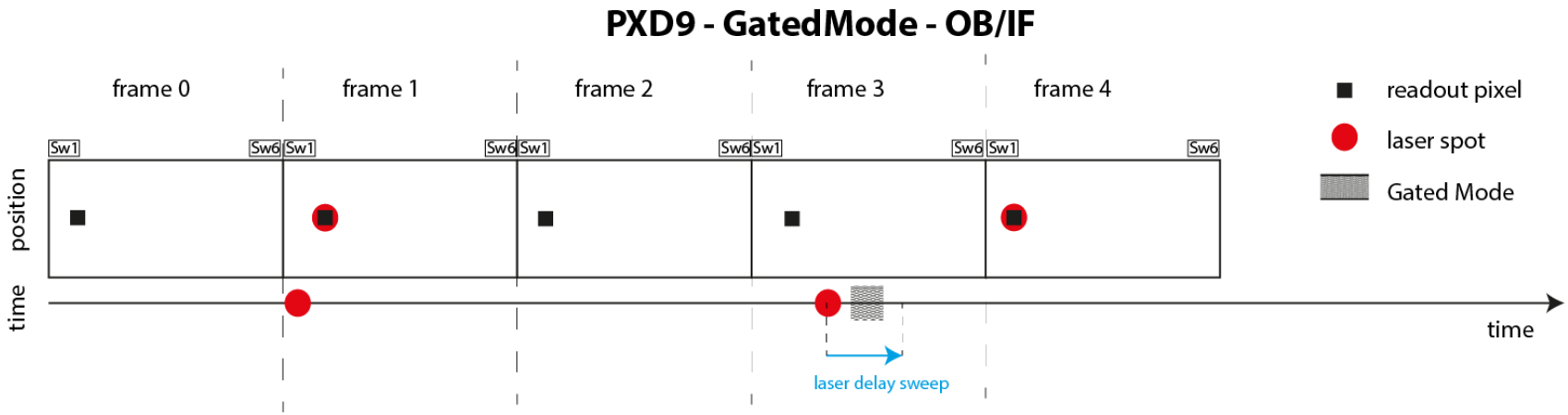
The BELLE II PXD layout

total 0.2% X_0



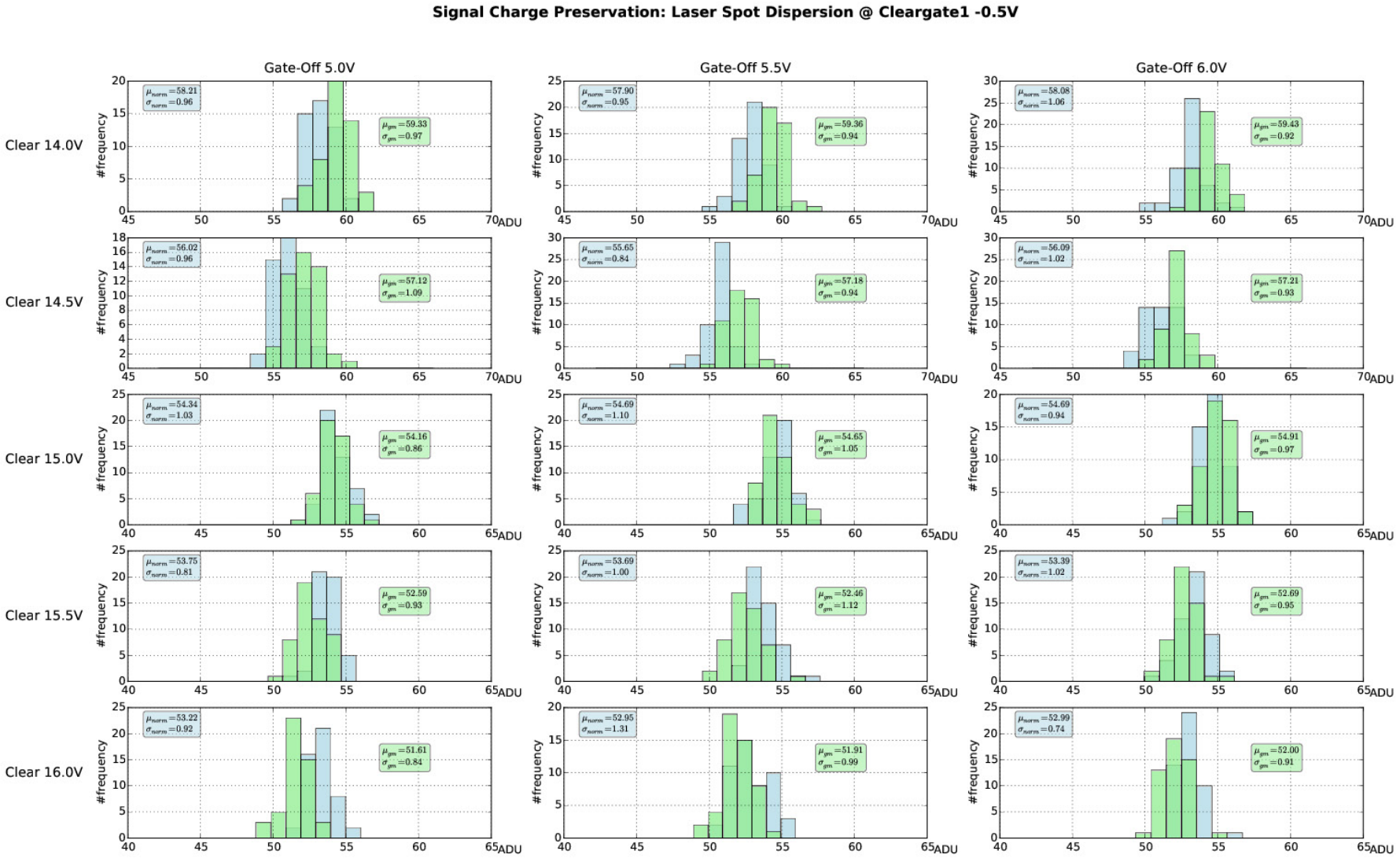
Laser tests





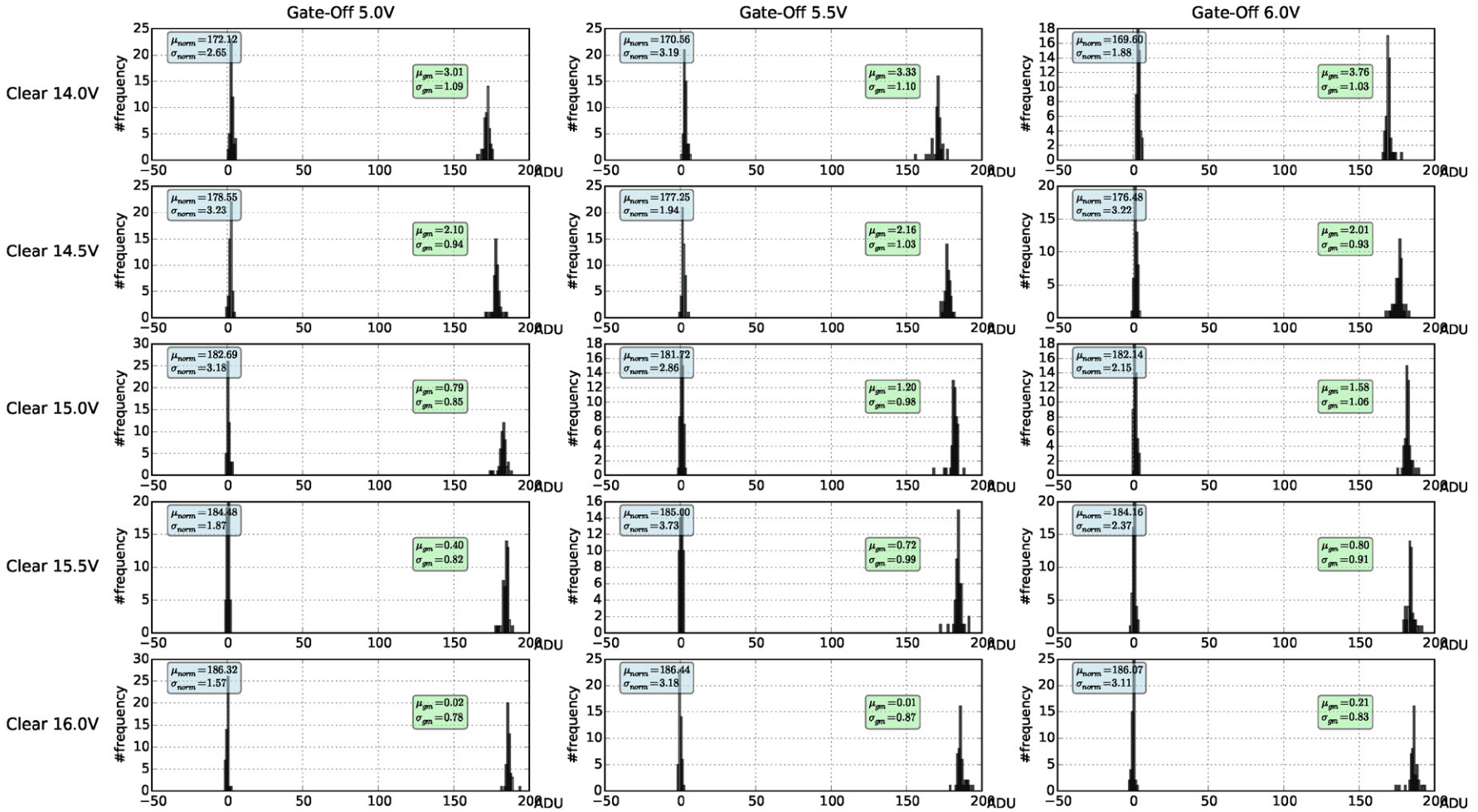
frame 0: pedestals
frame 1: pixel shows signal of the laser impinging in frame 1 (right before the pixel is read)
frame 2: pixel shows Clear efficiency
frame 3: pixel shows pedestal value; gated mode is switched on ; laser is impinging
frame 4: pixel shows signal (charge conservation & junk charge prevention), depending on timing of laser

Voltage Scan: SCP – Signal Charge Preservation



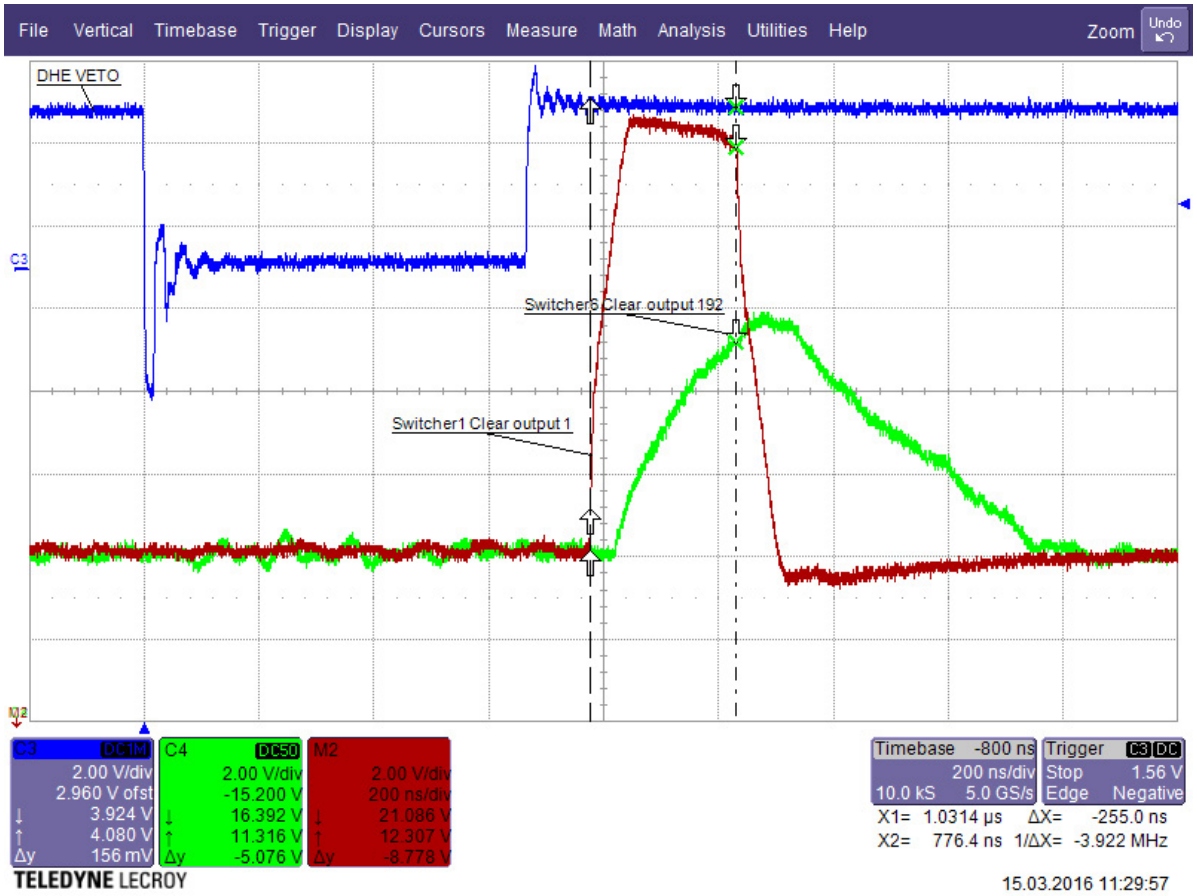
DCD analog CM off

Voltage Scan: JCP – Junk Charge Prevention, CCG =-0.5V



DCD analog CM off

Direct measurement of the *Clear* pulse



- voltage drop along Vsub line on the balcony (SWB) causes worse behaviour of output driver of last SWB