The ATLAS Insertable B-Layer: from construction to operation

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The ATLAS Insertable B-Layer (IBL)



Module assembly & QA Stave assembly & QA

Integration

Commissioning

Operation

The ATLAS Insertable B-Layer (IBL)

Motivation

- ♦ Retain excellent vertex detector performance
- Improve heavy flavor tagging, primary and secondary vertex reconstruction/ separation
- Add additional redundancy of the detector in case of failures caused by radiation damage

Detector overview

- Length: ~64cm (~7m including services in both sides)
- 14 local support structures (staves) at 3.27 cm overlapping in phi
- 32 R/O chips per stave
- New R/O chip: FE-I4 in IBM 130 nm CMOS
 - Cell size (50 x 250) μm²
 - 80 columns x 336 rows = 26880 channels / FE
- Data transfer at 160 MHz
- CO₂ cooling integrated into the staves



... seen as a first tech step to HL-LHC

> New **sensors** with higher radiation hardness

 \Rightarrow 5 x 10¹⁵ n_{eq} cm⁻² NIEL (improved radiation hardness by factor 5)

- New readout chip with finer segmentation, larger active fraction and increased hit-rate capability
 - $\diamond~$ New readout architecture and smaller cell size (250 x 50) μm^2
 - ♦ Large single-chip (20.2 x 18.8) mm²
- Lighter detector: less radiation length of support and cooling structures
 - Improved radiation length per layer from 2.7% to 1.9% to minimize multiple scattering in innermost layer
 - ♦ High efficiency CO₂ cooling at -40°C coolant temperature

See dedicated talk by B. Veerlat on Friday

New off-detector readout system

 \diamond Increased readout speed by a factor 2

Sensor technologies

Two technologies chosen: Planar and 3D

- Planar (produced by CiS)
 - 200 µm thick n⁺-in-n sensor
 - Inactive edge minimized by shifting guard rings (13) underneath pixel region
- **3D** (produced by CNM and FBK)
 - 230 µm thick n+-in-p sensor
 - Column through almost the full bulk with two electrodes per pixel

Sensor specification:

- Qualified up to 5 x 10¹⁵ n_{eq}cm⁻²
- Sensor max power dissipation: 200 mW cm⁻² at -15°C
- Single-hit efficiency > 97%

Population of sensors on the staves:

- 75% Planar (central)
- 25% 3D (at both sides, i.e. large η)







p⁻ sub.

Detector construction: flow chart



Module assembly, production and QA

Planar/Double-chip



3D/ Single-chip



~710 modules produced in total (in ~1-year)

- Verification of basic functionality at 15°C after the assemblage
- Thermal stress: 10x (-40°C to +40°C) ٠
- Final qualification at -15°C •
- Module yields (lower than expected, see next): •
 - Planar (double-chip: CiS) ~75%
 - 3D (single-chip: FBK and CNM) \sim 62%
- Ranking and module selection IBL spec < 1% pixel defects/FE



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ATLAS **IBL** Preliminary Number of Modules 160 All Produced All Produced CNM B.B. Fail. B.B. Fail. B.B. Fail. Other Fails Other Fails. Other Fails 140 Bare Fail. Bare Fail 120 100 80 60 40 20 20 F 17 14 13 Bad Module Fraction 0.8 Average (Batch ≥ L2): 0.37 Average (Batch > L2): 0.3 **0.6** Average (Batch ≥ L2): 0.25 0.4E 0.2Ē 0 L1 L2 L3 L4 L5 L1 L2 L3 L4 L5 L1 L2 L3 L4

Bump bonding

Two kind of defects observed on the first batches

- Large area of unconnected bumps (opens)
- Areas or single bump defects distributed over the module (shorts)
- Stopped production in late September 2012
- Intense investigation program
 - Open bumps traced back to excessive flux in flip- \diamond chip process
 - ♦ Lack a convincing explanation of the opens origin but problem vanished switching to flux-free flipchip
- Restarted production with flux-free flip-chip \geq process in February 2013



Crosstalk of a batch-3 module







Stave loading

- 20 production staves built in ~1-year
- 428 modules loaded in total
 - Including module replacement (28)
 challenging and risky operation for
 nearby modules but possible!

Reason of module replacement





- First stave quality check at the loading site
 - Optical inspection and basic electrical/functional tests

Stave quality assurance

- **Tuning at different temperature** and Source (⁹⁰Sr) scans on the full stave
 - Mimic real detector operation in clean-room

Pixel defects

- Classified as related to sensor, FE or bump bonding
- 73% of all chips loaded onto staves have less than 0.1% bad pixel
- Percentage of disconnected bumps is less than 0.06% for the produced staves

Selection of the best 14 staves

- Arranged modules & staves in final IBL for uniform low η-φ distribution of dead pixels for η < 2
- Total bad pixel ratio for the integrated staves is < 0.1%</p>





Wire bonds corrosion

- Two staves were accidentally exposed to a severe condensation during QA
- Observed corroded wire bonds which triggered a detailed inspection of all staves
- Stopped production in earlier September 2013
- Intensive investigation program & solution:
 - Found Halogen (Cl or F) associated with corrosion product (residue)
 - Aggressive cleaning helped but also weakened the gold metallization
 - Coating with Uretan showed a very good protection (too late for being applied in the production)
 - > Rework of the affected staves already produced
 - 1) Wire bonds removal and cleaning
 - 2) Re-boning all FE and wings pads
 - 3) Keep the detector dry as much as possible





Stave integration onto IPT





Integrated staves on support tube (IPT) within one month

- Stave was mounted with a support structure onto the IPT (clearance less than 0.8mm between IPT and stave) after cooling pipe extensions were made by brazing
- Staves were connected on both ends to power and readout services and then tested

> Tests confirmed the results obtained during stave QA

Installed, connected and tested





- May 2014: the detector was completed and installed
- End of June 2014: the detector was connected to power, readout and cooling, and then the detector commissioning started

From electrical/ functional-tests no deterioration observed

Calibration

Tuning: Threshold at 2500e- and TOT of 10 at 16000e- (Temp=-15 °C)



Commissioning with cosmic rays



November 2014:

First track with **IBL** integrated into the ATLAS data-taking

First tracks with the 4-Layer Pixel detector included into ATLAS data-taking collisions at 13 TeV, May 2015.



See next talk by S. Tsuno

Wire bonds oscillation

Wire bonds operate in the 2 T B-field and most of them at low currents except for voltage regulator connections

- High currents can be caused by consecutive triggers or calibration scans (max possible AC current is ~ 100 mA)
- Test and simulation showed that wires can break at the resonance frequency or in one harmonic
 - Digital supply lines are susceptible to current fluctuation when receiving triggers





Fixed Frequency Trigger Veto (FFTV) implemented into the readout chain to limit the number of trigger in resonance region

Mechanical distortion

- Observed in early 2015 during cosmic runs at the level of few μm/K
 - Origin: **CTE mismatch** between service buses and staves that manifests itself in a r- ϕ **twisting** of staves at the level of few μ m/K
 - The impact of this effect is manageable by a careful temperature control at the level of ~0.2K (alignment correction every 100 luminosity block)



FE-I4 low voltage current drift



FE low voltage current and parameters (threshold, ToT) drifted with integrated luminosity in 2015

Consequences: Temperature increase and electrical failures

- Understood to be caused by a N-MOS transistor leakage current due to defects built-up at the silicon oxide interface (STI) and accumulated with increasing by the total ionization dose (TID)
- Parametrization of the leakage current was computed
- Using special detector operation procedures, a successful data taking was possible





Lessons for the future

- **IBL** is a new detector **built relatively quickly** and with a short R&D time
- **Major issues discovered** late in the production, during commissioning and data-taking but **no showstoppers**.

Lessons learned:

A new detector even if built by experts needs time for R&D, review and extensive qualification in all its domains.

- ➤ Mechanical distortion → stiff structure low susceptibly to temperature variation (low CTE).
- ➢ Wire bonds oscillation → potting, thick wires or no wires at all (TSV + RDL + Laser soldering).
- ➢ FE chip (NMOS transistor leakage current) → qualification to radiation should not be done only for intermediate and high doses.



Summary



The Long-Shutdown-1 was realized as an opportunity and finally a great success for the Pixel Detector upgrade:

- 4th Layer Pixel (IBL) successfully installed and in operation with good performance
- First and successful use-case of **3D-Si** sensors in HEP experiment !

References

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