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PFM2: a 32x32 Processor for X-ray Diffraction Imaging at FELs

This work presents the results from the characterization of a readout chip for application to experiments at the next generation X-ray free electron laser (FEL). The ASIC, named PixFEL Matrix (PFM2), has been designed in a 65 nm CMOS technology and consists of 32x32 pixels. Each cell covers an area of 110x110 um2 and includes a low-noise charge sensitive amplifier (CSA) with dynamic signal compression, a time variant shaper used to process the signal at the preamplifier output, a 10-bit successive approximation register (SAR) analog-to-digital converter (ADC) and digital circuitry for channel control and data readout. Two different solutions for the readout channel, based on different versions of the time variant filter, have been integrated in the chip. Both solutions can be operated in such a way to cope with the high frame rate (exceeding 1 MHz) foreseen for future X-ray FEL machines. The ASIC will be bump bonded to a slim/active edge pixel sensor to form the first demonstrator for the PixFEL X-ray imager. This work has been carried out in the frame of the PixFEL project funded by Istituto Nazionale di Fisica Nucleare (INFN), Italy. The members of the PixFEL Collaboration are affiliated with Università di Bergamo, Università di Pavia, Università di Pisa, Università di Trento and INFN, Italy.

Summary

The experimental environment at the next generation X-ray free electron laser (FEL) facilities requires that the electronic instrumentation be able to cope with very challenging specifications in terms of space and amplitude resolution, frame rate, input dynamic range, frame storage capability and radiation hardness. The PixFEL collaboration aims at developing a multilayer, hybrid pixel detector for X-ray diffraction imaging applications compliant with these severe requirements [1]. The sensing layer will be based on a fully depleted slim edge silicon pixel detector to minimize the dead area at the sensor edge. The readout processor will result from the vertical integration of two layers, one for the integration of the analog front-end and the ADC, the second one to dedicated memories used to accumulate data in applications with high X-ray pulse rates. In the first stage of the project, the main building blocks of the readout channel have been designed and successfully tested [2,3]. Moreover, the initial steps have recently been taken in the characterization of slim/active edge sensors from the first production batch [4].

Following the outcomes from the characterization of the first prototype front-end [2,3], a readout chip, consisting of 32x32 square cells and called PFM2, has been designed and submitted to the foundry at the end of March 2016. As for the prototype, a 65 nm CMOS technology has been chosen for the design of the PFM2 chip in order to accommodate all the pixel functionality in a pitch of 110 um. Each cell includes a low-noise charge sensitive amplifier with dynamic signal compression, a time variant shaper, which implements a trapezoidal weighting function, a low power, small area 10-bit SAR converter, relying on a time interleaved method and elementary digital circuitry for channel control and data readout.

In the new chip, starting from the compression idea already validated with the first channel prototype, a more complex feedback network has been designed for the charge sensitive amplifier. The feedback transistor, responsible for the dynamically changing sensitivity of the CSA, is split into four devices with the same channel length and different channel widths. Three switches, in series with three of the four feedback elements and controlled with two programming bits through a binary-to-thermometric decoder, determine the total area of the feedback MOS capacitor. By a suitable choice of the configuration bits, the amplifier is made capable

of processing signals from photons at 1, 2, 4 or 10 keV while preserving its capability of complying with an input dynamic range of 1 to 10^4 photons.

Two different solutions of the time variant shaper have been integrated in the PFM2 chip. Half of the cells in the 32x32 array is equipped with the filter already implemented and tested in the channel prototype, based on a transconductor, which converts the voltage at the output of the CSA into a current, and on the so called flip-capacitor filter (FCF) [5]. The other half of the array incorporates a new version of the time variant shaping stage named differential gated integrator (DGI). The new proposed architecture is based on a differential integrator designed around the same forward gain block already implemented for the FCF. The two input terminals of the differential integrator are switched between the reference voltage (Vref) and the output of the CSA (Va) to obtain, by means of a correlated double sampling (CDS) technique, a trapezoidal weighting function. More in details, during the baseline integration interval, the non-inverting input of the DGI is connected to the output of the CSA, whereas the other terminal is shorted to Vref. In the subsequent signal settling interval, both the terminals are left floating while the charge generated in the detector by the diffracted laser pulse induces a signal at the CSA input. A second integration is performed in the subsequent period, during which the inverting input of the DGI is connected to the CSA output and the non-inverting terminal is connected to the reference voltage. At the end of this time interval, the amplitude of the signal at the output of the DGI block (Vo) is proportional to the difference between the CSA output level after the photon signal arrival (Va+), and the baseline level (Va-): Vo=Vref+(T/RC)(Va+ - Va-), where T is the integration time and R and C are the resistance and the capacitance in the differential integrator. At the end of the cycle, after the voltage level has been sampled by the ADC, the feedback capacitances of the charge sensitive amplifier and of the filter are reset. The new filter has been simulated by referring to the target processing frequency of 5 MHz of the European XFEL. The total power consumption for the channel with the DGI (including the ADC) is about 230 uW for an integration time of 50 ns (a quarter of the minimum processing period of 200 ns), to be compared to the 350 uW power dissipation for the channel with transconductor and FCF.

At the time of the conference, besides discussing in detail the readout channel and array architecture, results from the experimental characterization of the chip will be presented.

[1] L. Ratti, D. Comotti, L. Fabris, M. Grassi, L. Lodola, P. Malcovati et al., "PixFEL: developing a fine pitch, fast 2D X-ray imager for the next generation X-FELs", Nucl. Instrum. Meth., vol. 796A, pp. 2-7, 2015, doi:10.1016/j.nima.2015.03.022

[2] M. Manghisoni, D. Comotti, L. Gaioni, L. Ratti, V. Re, "Dynamic compression of the signal in a charge sensitive amplifier: from concept to design", IEEE Trans. Nucl. Sci., vol. 62, no. 5, pp. 2318-2326, 2015. doi:10.1109/TNS.2015.2477461

[3] L. Lodola, "Interleaved SAR ADC for in-pixel conversion in future X-ray FEL application", 2015 11th Conference on Ph.D. Research in Microelectronics and Electronics (PRIME), pp. 81- 84, 2015. doi:10.1109/PRIME.2015.7251339

[4] G.-F. Dalla Betta, G. Batignani, M.A. Benkechkache, S. Bettarini, G. Casarosa, D. Comotti et al., "Design and TCAD simulation of planar p-on-n active-edge pixel sensors for the next generation of FELs", Nucl. Instrum. Methods, available online, http://dx.doi.org/10.1016/j.nima.2015.08.027.

[5] L. Bombelli, C. Fiorini, S. Facchinetti, M. Porro, and G. De Vita, "A fast current readout strategy for the XFEL DePFET detector", Nucl. Instrum. Meth., vol. 624, pp. 360-366, 2010. doi:10.1016/j.nima.2010.03.123

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