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Large Area Thinned Planar Sensors for Future High-Luminosity-LHC Upgrades

Planar hybrid silicon sensors are a well proven technology for past and current particle tracking detectors in HEP experiments. However, the future high-luminosity upgrades of the inner trackers at the LHC experiments pose big challenges to the detectors. A first challenge is an expected radiation damage level of $2E16 \text{ n}_{\text{eq}}/\text{cm}^2$. For planar sensors, one way to counteract the charge loss and thus increase the radiation hardness is to decrease the thickness of their active area. A second challenge is the large detector area which has to be built as cost efficient as possible, i.e. it is aimed for low-cost and large-sized sensors.

The CiS research institute has accomplished a proof-of-principle run with n-in-p ATLAS-Pixel sensors where cavities are etched to the sensors back side to reduce its thickness. One advantage of this technology is that thick frames remain at the sensor edges and guarantee mechanical stability on wafer level while the sensor is left on the resulting thin membrane. During the dicing step, the frames can be removed in order to obtain completely thin sensors. For this cavity-etching technique, no handling wafers are required which represent a benefit in terms of process effort and cost savings.

The membranes with areas of up to $\sim 4 \times 4 \text{ cm}^2$ and target thicknesses of 100 and $150 \mu\text{m}$ feature a sufficiently good homogeneity across the whole wafer area. The processed pixel sensors show good electrical behaviour with an excellent yield for such a prototype run. First sensors with electroless Ni- and Pt-UBM are already successfully assembled with read-out chips. The technology is currently transferred to 6" wafer size. First results of etching trials with dummy wafers with larger thinned areas will be shown as well.

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