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Recent Progress of RD53 Collaboration towards the Next Generation of Pixel Readout Chips for HL-LHC

This talk will be a overall review of recent progress of RD53 Collaboration. Results obtained on the study of the radiation effects on 65nm CMOS have matured enough to defined first strategies to adopt in the design of analog and digital circuits. Critical IP-blocks and analog very front ends chains have been designed, tested before and after 5-800 MRad. Small prototypes of 64x64 pixels with a complex digital architectures have been produced, and point to address the main issues of dealing with extremely high pixel rates, while operating at very small in-time thresholds in the analog front end. The collaboration is now proceeding at full speed towards the design of a large scale prototype, called RD53A, in 65nm CMOS technology.

Summary

The scope of CERN/RD53 collaboration is the development of pixel readout Integrated Circuits (IC) for the next generation of pixel readout chips to be used for the ATLAS and CMS Phase 2 pixel detector upgrades and future CLIC pixel detectors. The IC challenges include: smaller pixels to resolve tracks in boosted jets, very high hit rates due unprecedented particle fluence, much higher output bandwidth, radiation and large IC format with low power consumption in order to instrument large areas while keeping the material budget low. Nineteen institutes from nine countries, for a total of about 120 members are part of RD53, coming from CMS and ATLAS experiments.
This talk will be a overall review of recent progress of RD53 and the preparation towards the large scale prototype, called RD53A, in 65nm CMOS technology. Principal outcomes of the characterization of the radiation effects on electronics will be remind here, together with strategy adopted in the design of analog and digital circuits.
A total of 15-20 IP-blocks have been identified of interest for future pixel chips and four different designs of very front end analog chains have been developed, each one adopting a different architecture. All crucial IP-blocks and very front end analog chains needed for RD53A production have been designed and sent for production: most of those have been successfully tested before and after 5-800Mrad total dose: an extraction of main results will be presented.

Two small size demonstrators, consisting of a matrix of 64x64 pixels each of dimension 50x50 um2 have been designed as intermediate step, and point to address in a complementary way to: address the low noise, low in-time threshold (1000e-) performance; integrate the different analog front end chains and of several IP-blocks developed; to develop a complex digital architecture with high efficiency for the very high pixel rate of 3 GHz/cm2 foreseen in the inner layer of HL-LHC pixel detectors. One of the demonstrators (FE65-P2) has been produced and it is now under test; the other one (CHIPIX65) will be submitted for production in June.
The design of RD53A is on going, with a team of about ten designers working together. Main strategies, progresses and challenges will be presented.

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