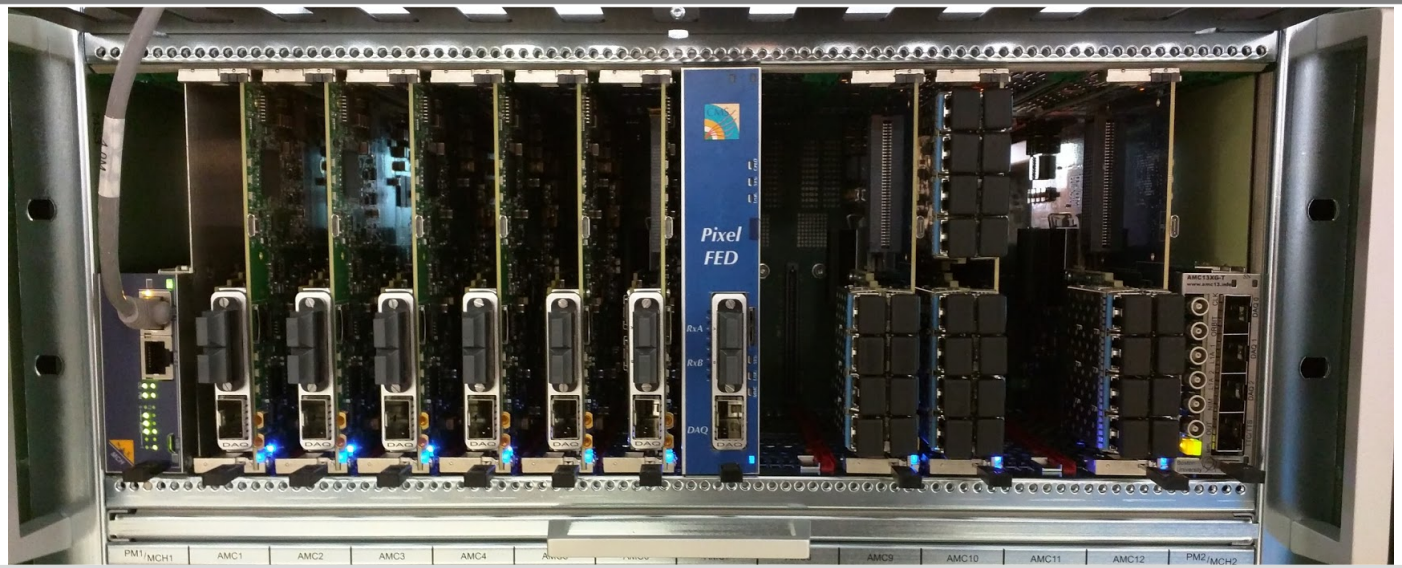
A new Data Acquisition System for the CMS Phase 1 Pixel Detector

Andreas Kornmayer on behalf of the CMS Pixel DAQ WG

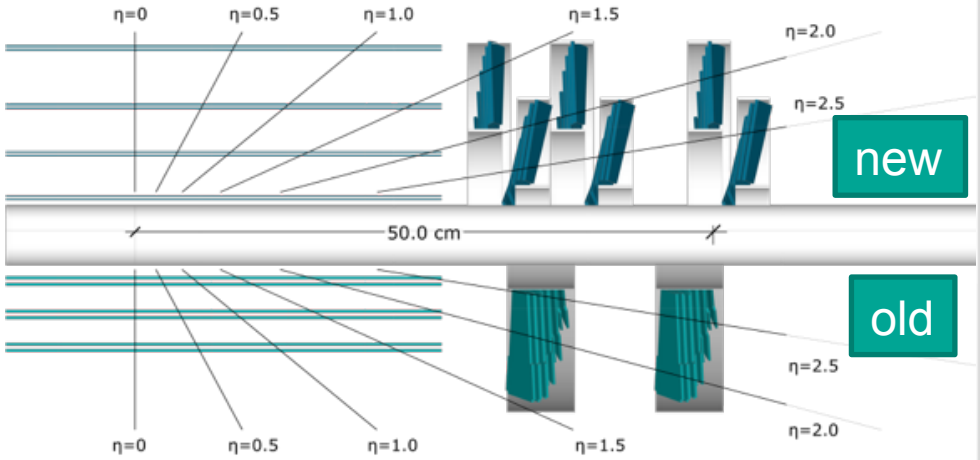
CERN



The CMS Phase 1 Upgrade in a Nutshell

Motivation:

- Increase of instantaneous luminosity until Long Shutdown 3
  - → Higher pile-up, higher track density and higher occupancy on detector
  - → Higher data rates, old readout chips (ROCs) become inefficient
- During an extended YETS 2016/2017 the entire CMS Pixel Detector is being replaced and upgraded
  - one additional layer in barrel (BPIX) and forward region (FPIX), gives a 4th point for vertex reconstruction
  - number of channels increases from 66M to 123M
  - new digital readout scheme (PSI46dig + PROC600)
  - CO_2 cooling
  - reduction of material budget



More info in talk from Vittorio Raoul Tavolaro, "The Phase1 CMS Pixel detector upgrade"

System requirements for the new Pixel DAQ

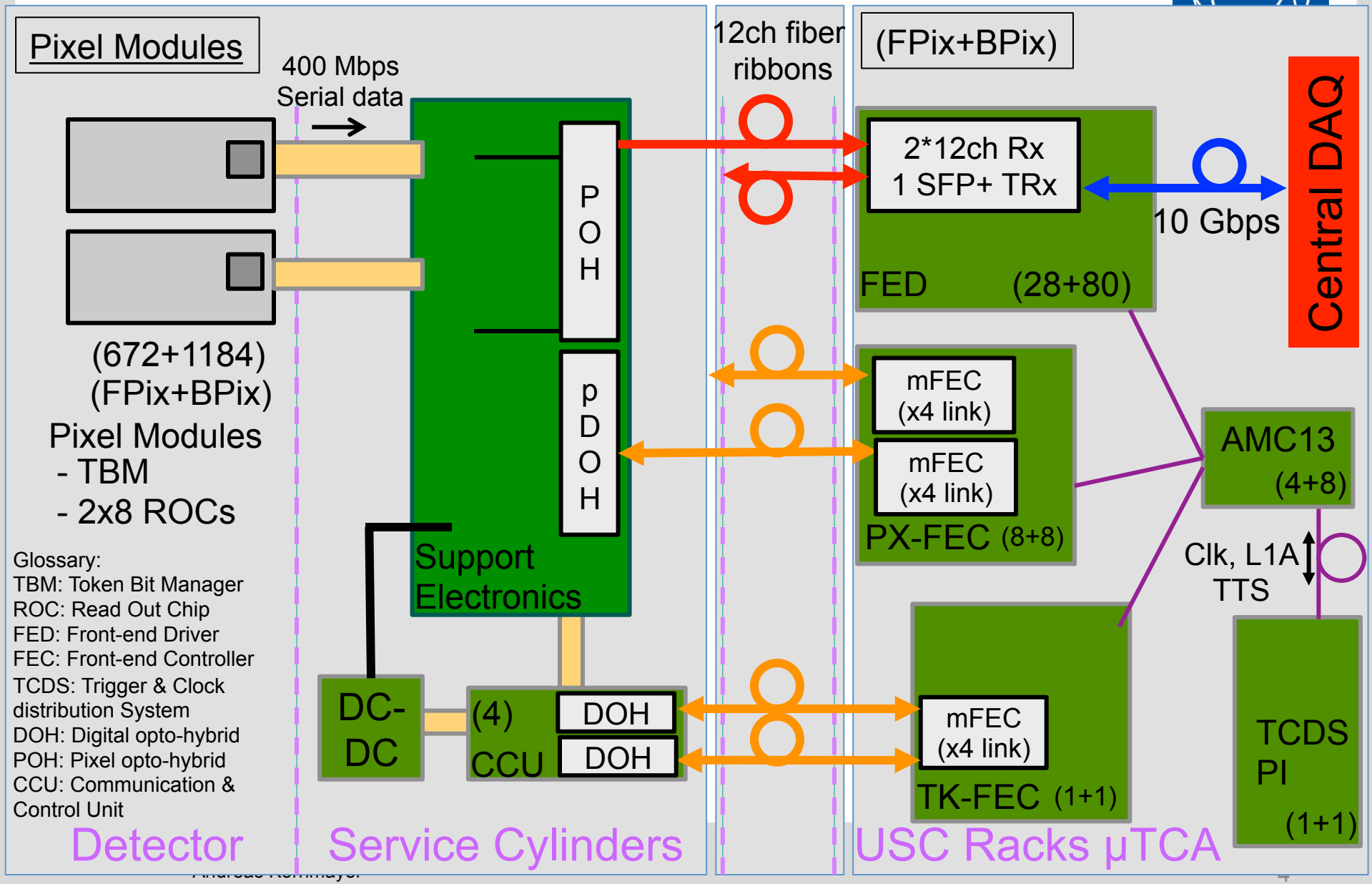
- digital 400 Mb/s readout scheme
- 2x number of readout channels (1856 modules, 2368 links)
- increased data rate per link due to improved front-end

- increased number of control links
- VME parts out of production

→Upgrade of the Front End Driver (FED)

→Upgrade of the Front End Controller (FEC)

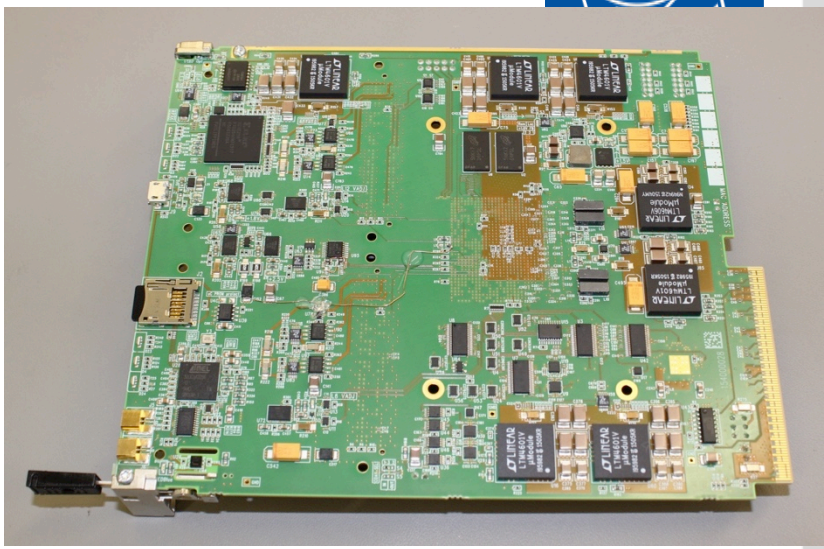
Readout architecture

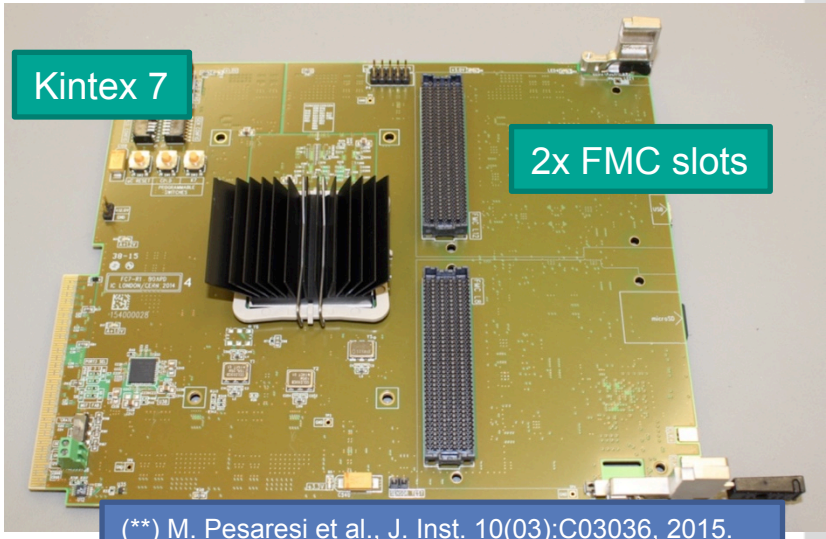


The Phase 1 Pixel FED and FECs

FC7 board

- full size, double width µTCA AMC
- common standard in CMS (TCDS, HCAL, CT-PPS)
- Kintex 7 FPGA
- 4 GB DDR3 RAM for data buffering
- 12 high speed links to backplane (10Gb/s)
- 2 FMC (FPGA Mezzanine Card) slots
  → decide flavor of card (FED or FEC)



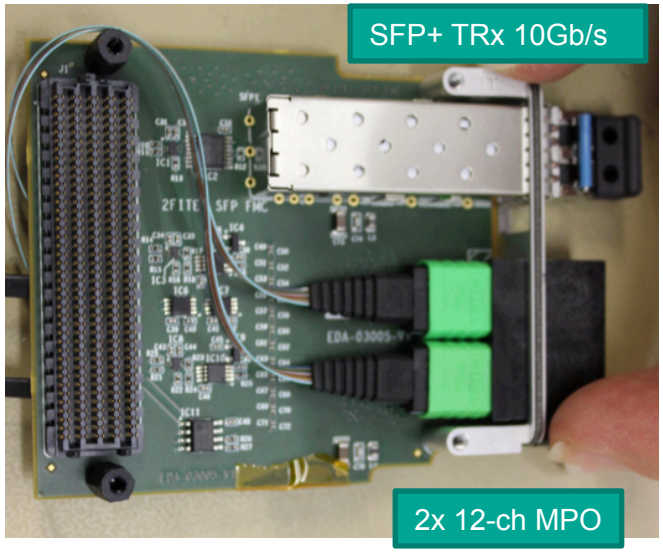


(**) M. Pesaresi et al., J. Inst. 10(03):C03036, 2015.

The Phase 1 Pixel FED and FECs

FC7 board

- full size, double width µTCA AMC
- common standard in CMS (TCDS, HCAL, CT-PPS)
- Kintex 7 FPGA
- 4 GB DDR3 RAM for data buffering
- 12 high speed links to backplane (10Gb/s)
- 2 FMC (FPGA Mezzanine Card) slots
  → decide flavor of card (FED or FEC)



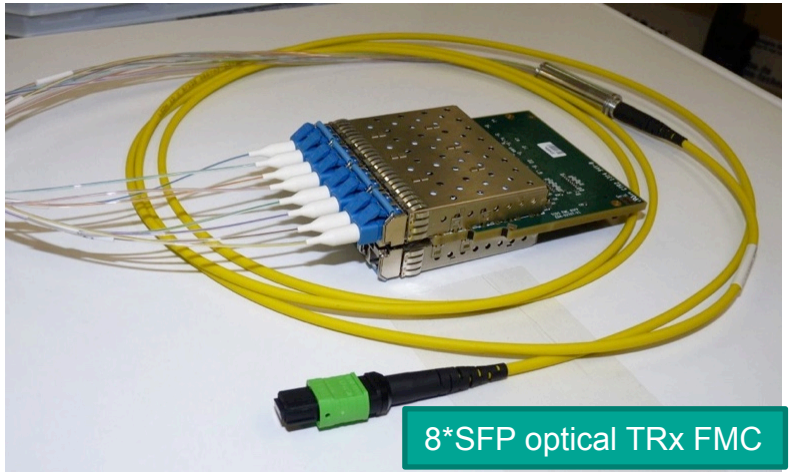
To make it a FED:

- 24 optical input channels
  - 2 FITEL 12 channel optical receivers, optimized for the 400Mb/s optical signal at 1310nm
- 1 DAQ output
  - SFP+ 10Gb/s transceiver for S-Link Express DAQ output to CMS Central DAQ
- Firmware:
  Decode incoming data links, detect possible errors, build events, transfer data to central DAQ

The Phase 1 Pixel FED and FECs

FC7 board

- full size, double width µTCA AMC
- common standard in CMS (TCDS, HCAL, CT-PPS)
- Kintex 7 FPGA
- 4 GB DDR3 RAM for data buffering
- 12 high speed links to backplane (10Gb/s)
- 2 FMC (FPGA Mezzanine Card) slots
  → decide flavor of card (FED or FEC)

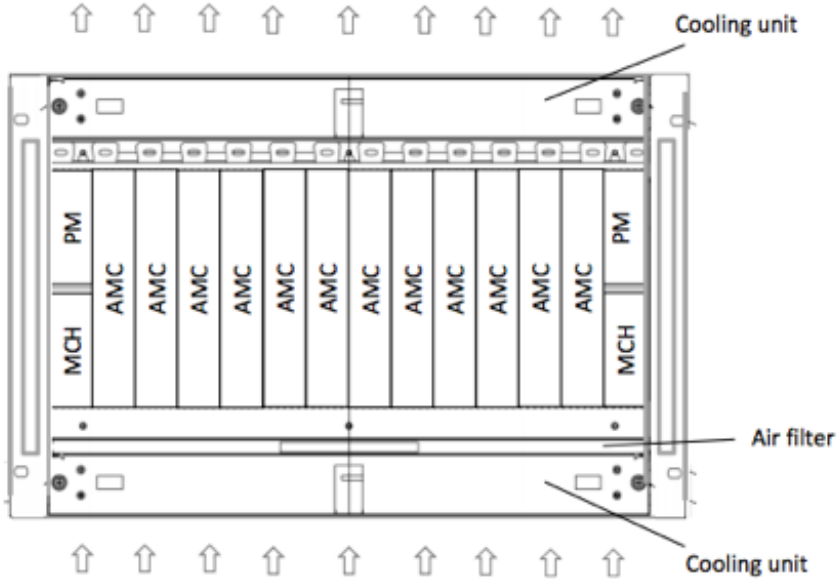


To make it a FEC:

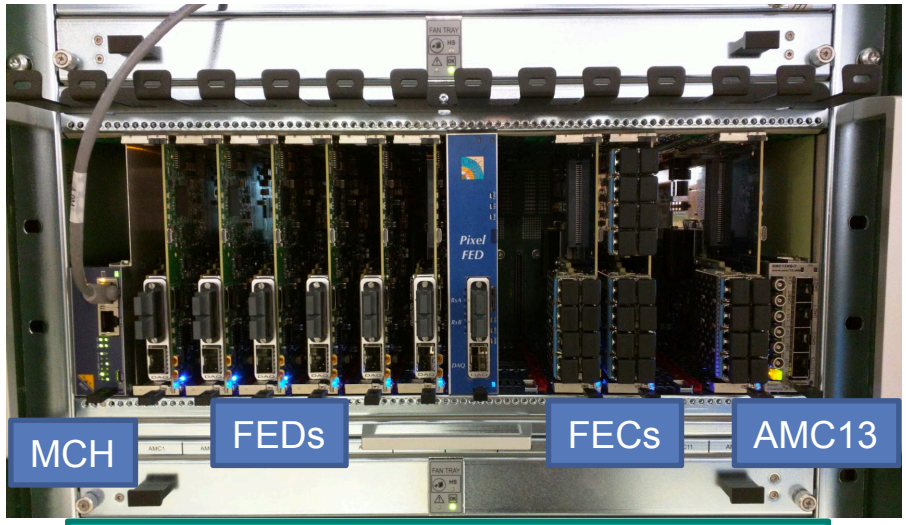
- Two FMCs equipped with low-speed (1Gb/s) optical transceivers
  - 8 SFPs per FMC
- Two flavors of FECs, but hardware fully identical
  Firmware defines FEC flavor
- Firmware:
  Receives configuration, program front-end (Pixel FEC) or service electronics (Tracker FEC), send control signals (clock, trigger, resets…)

A single µTCA crate

- Can hold up to 12 full size AMC cards
- Two redundant power supplies
- 1Gb/s Ethernet network access to all cards through MCH (MicroTCA Carrier Hub)
- Additional AMC13, custom made MCH like card, to distribute clock and trigger signals over crate backplane (CMS specific design)



µTCA crate layout

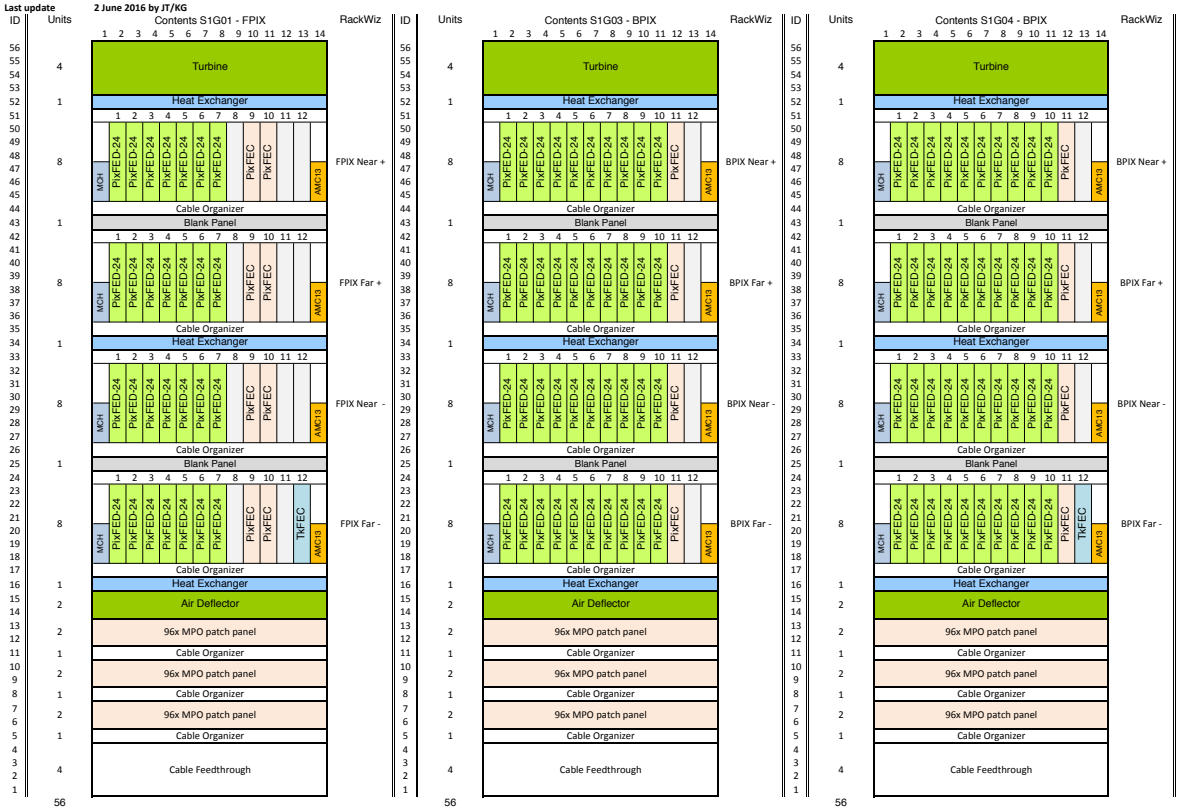


Example FPIX crate configuration

Full system layout

- 12 µTCA crates in 3 racks to hold all components of the DAQ backend.
  - 108 FEDs
  - 18 FECs

  + spares
- Separated into 1 rack for FPIX and 2 racks for BPIX
- Powered by AC/DC converters
- Patch panels for 12-fibre optical cables coming from the detector (MPO connectors)



Rack layout for CMS service cavern

System tests: In the laboratory

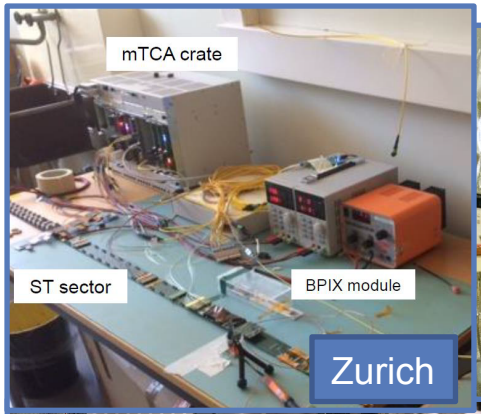
- Firmware and software development still ongoing
- Small scale systems used for development and testing of final detector parts
  → Advances development and helps finding bugs

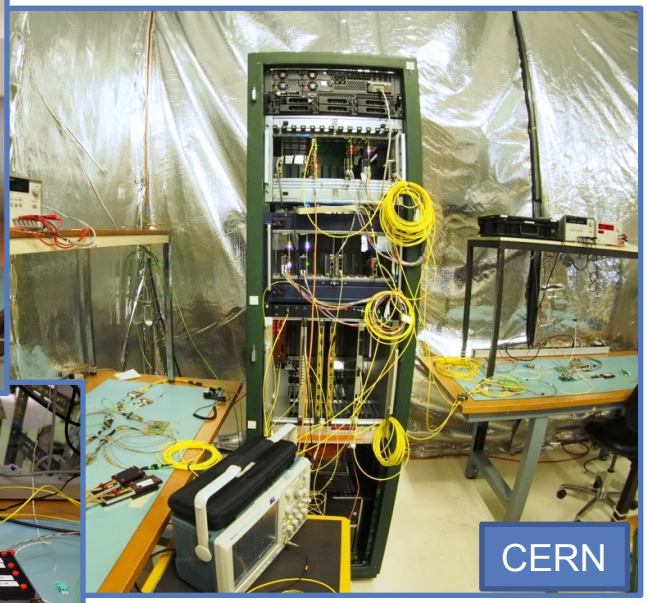
Integration centers using µTCA:

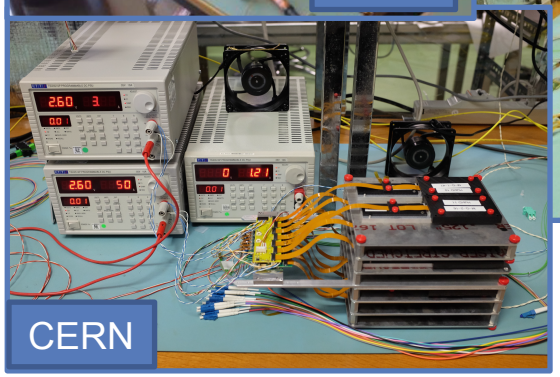
@CERN: Firmware development and general hardware tests, reception tests of arriving detector parts

@Fermilab: Final checkout of FPIX detector before being shipped to CERN for installation in CMS

@Zurich: Test of the optical components of the service cylinders, integration tests for BPIX

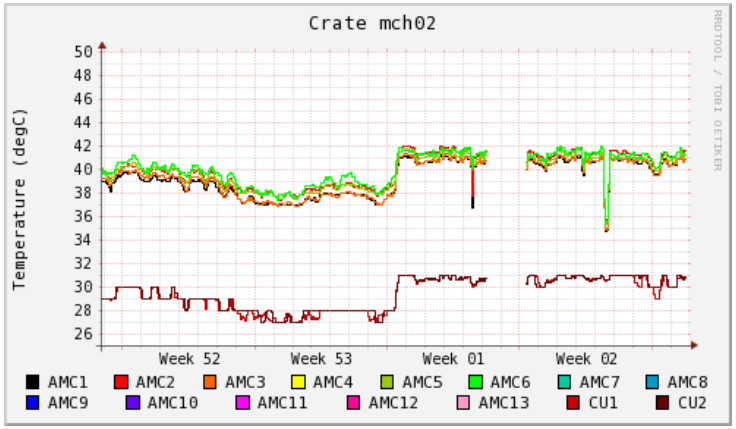


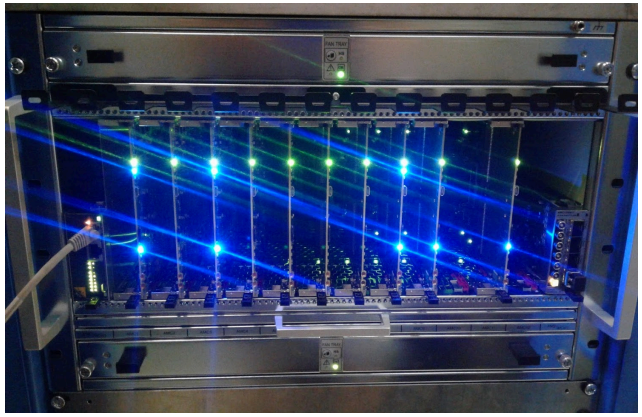




System tests: Getting a little bigger

- A soak test facility has been set up at CERN
- Rack layout identical to the final setup (3 racks with 4 crates each)
- Will be used to test all production parts before they are installed in the CMS service cavern
  - Soak test:
    Firmware load and power cycling of FEDs & FECs
    → Test for infant mortality while stressing the components
  - Measurement of optical receivers using the FED tester, a front-end emulator board
- Development stage for a crate monitoring system (temperatures, voltages, currents)

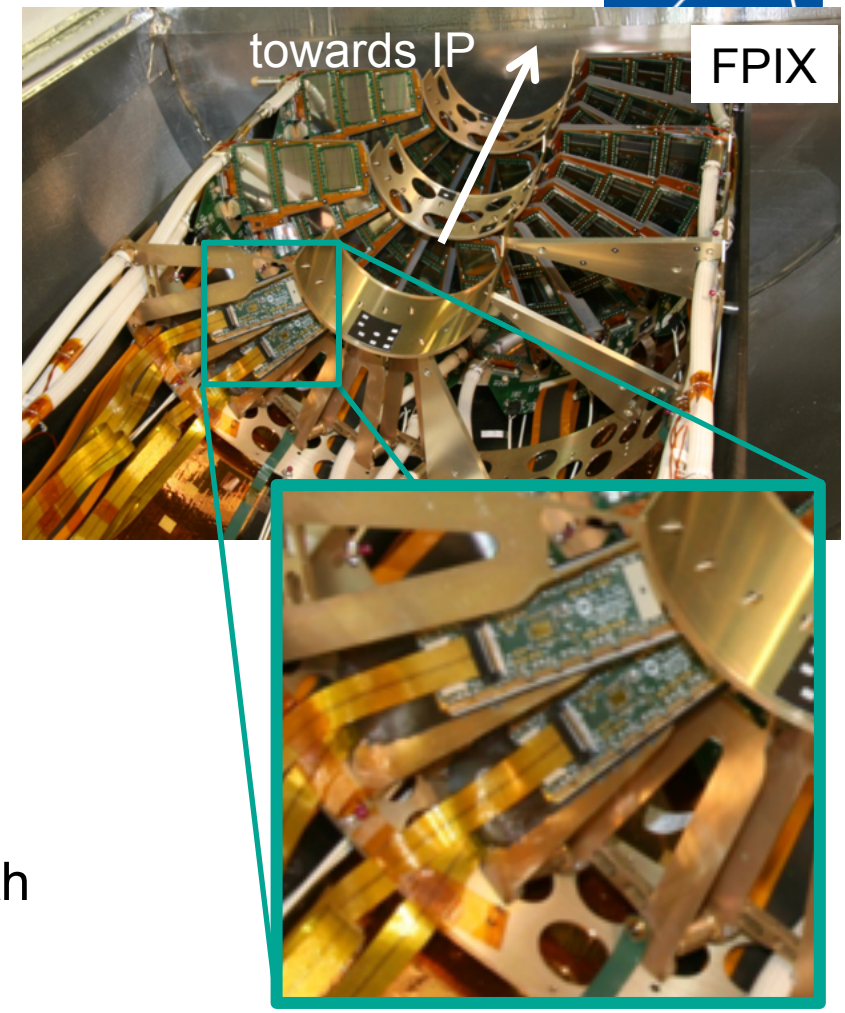




System tests: In the CMS detector

Phase 1 Pilot Blade

- 8 prototype pixel modules installed in CMS, right behind the two current FPIX disks
- Full readout chain as is intended for the upgraded detector
  - Readout chips & TBM chips
  - DC-DC power converters
  - Portcards and CCU cards
- Readout in legacy VME and µTCA possible
- All components can be tested under realistic conditions within CMS
- Test integration of new Pixel DAQ with central systems of CMS



Two upgrade pixel modules

System tests: In the (near) future

- Only small scale systems with low data throughput have been tested until now
- Before installation the system has to be fully qualified also for the highest expected data rates
- Stress test system:

→ Connect a fully loaded crate (10 FEDs), emulated data patterns are send to the central DAQ processor of CMS

→ Test that the new detector DAQ does work with all other sub systems of CMS to ensure a smooth start-up in 2017

→ Ensure and show the readiness of the upgrade DAQ

Summary and Outlook

- A new DAQ system based on the µTCA standard has been designed and is currently under development to accommodate for the new digital readout scheme and higher data rates coming from the front-end.
- FEDs and FECs based on the FC7 µTCA board have been produced.
- Several test stands for hardware and firmware development and final detector checkout have been setup.
- Integration tests of the system into the full CMS experiment are planned for this fall.
- Once the current run period has ended the old pixel detector and its corresponding VME based readout system will be fully replaced by the new Phase 1 Pixel detector and the presented DAQ system.