From LHC to HL-LHC ...
challenges and routes to solutions

M. Garcia-Sciveres
Lawrence Berkeley National Lab

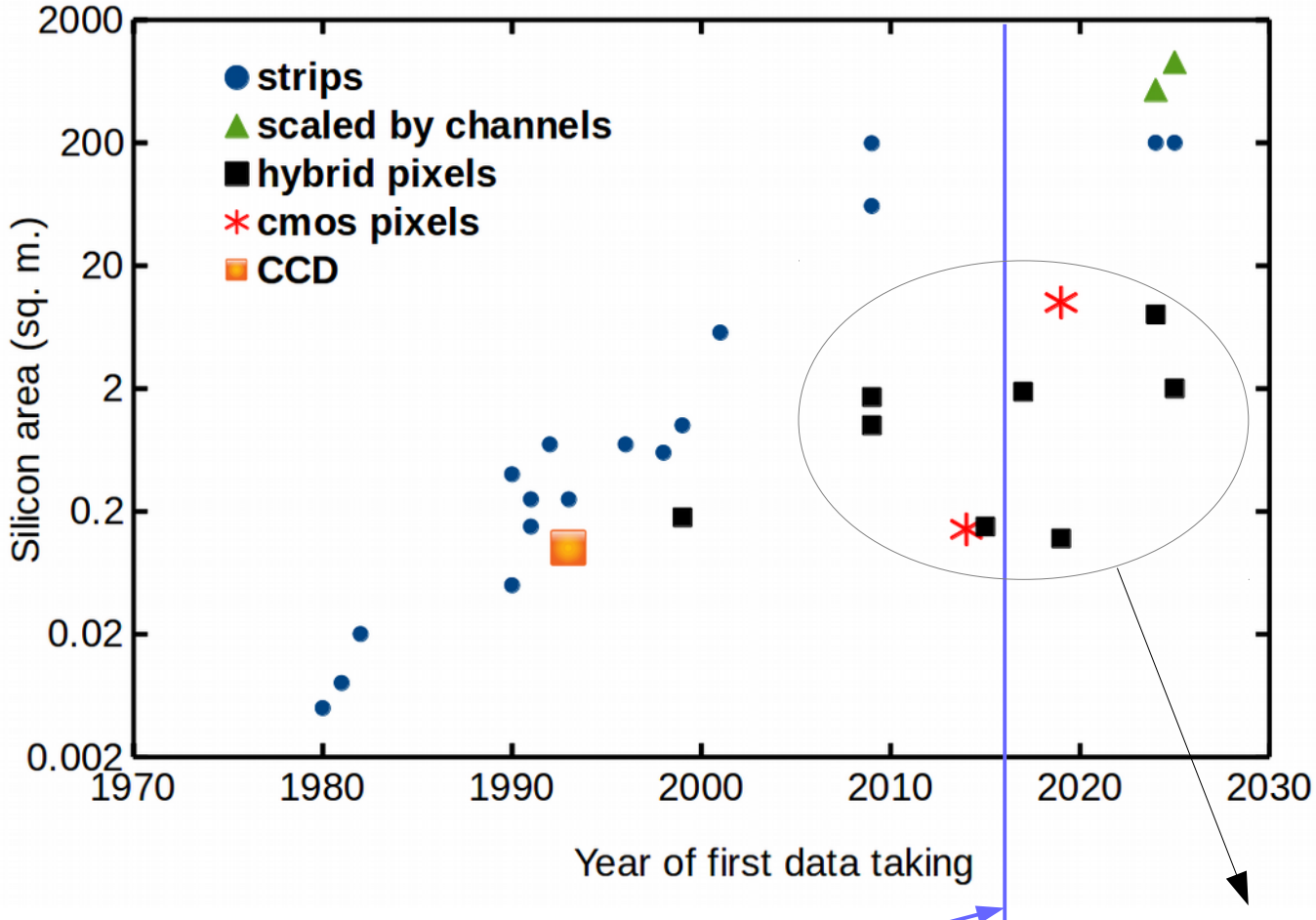
PIXEL 2016, Siestri Levanti

Challenges

- Scale
- Intensity
- Performance

This a overview/review talk in the middle of the conference.
Point to details in talks and posters throughout the conference

Scale



Strip Detectors		Hybrid Pixels	
1980	NA1	1999	Delphi
1981	NA11	2009	ATLAS
1982	NA14	2009	CMS
1990	MarkII	2015	ATLAS IBL
1990	DELPHI	2017	CMS
1991	ALEPH	2019	velopix
1991	OPAL	2025	ATLAS
1992	CDF SVX	2025	CMS
1993	L3		
1996	CDF SVX'	**CMOS Pixels**	
1998	CLEO III	2014	STAR
1999	BaBar	2019	ALICE
2001	CDF SVXII+ISL		
2009	ATLAS SCT	**CCDs**	
2009	CMS tracker	1993	VXD
2025	ATLAS ITK		
2025	CMS upgrade		

We have a dedicated talk or more for each point

Scale Solutions

- (There is no absolute right answer)
- Get more money
- Cheaper and faster construction
  - Multiple approaches explored in R&D

  - Reduce cost and increase volume of hybrid technology
  - Use different technology (eg. monolithic CMOS)
  - Combination (eg. passive sensor fabrication in CMOS foundry)
- Modular assembly
  - Different designs, but all are modular
- New Power Delivery Technology
  - Serial Power is baseline approach for both ATLAS and CMS

Reduce Hybrid Cost

- Larger chips, fewer chips per module
  - Long appreciated that flip-chip cost is per chip, not per bump
- Larger sensor wafers, n-on-p
  - 6” wafers are now standard. First 8” sensor wafers produced in 2015 (Unno, Fri. Wittig [P])
- Oh, but now we want to make everything thinner
  - This has complicated the use of large chips
  - Handle wafers and stress compensation layers successfully developed, but this eats into savings (Gaudiello, Bates, Fri. 11:15)
- Wafer-to-wafer integration
  - This would lead to dramatic cost reduction. Needs large format sensor wafers and thru silicon vias (Fritzsch [P])
- Increased competition among vendors
  - HL-LHC upgrades are not an irrelevant business opportunity for small scale companies

CMOS Sensors

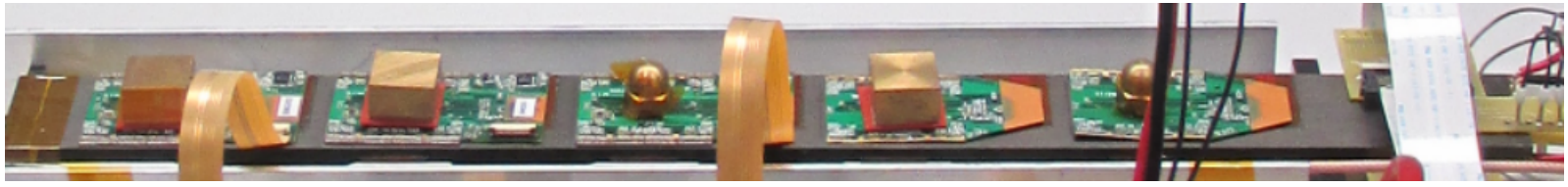
- Not all CMOS sensors are the same
  - Commercial sensors not fast enough or rad hard enough for ALICE
    (Reidt, Mon. 18:05, Sujic, Thu. 17:55)
  - ALICE sensors not fast enough or rad hard enough for ATLAS & CMS
    (Hemperek, Peric, Thu. 14:15; Calandri [P], Figueras [P], Hitesh [P])
- Monolithic CMOS is process-specific
  - Rad hard (collect by drift): HV-CMOS, HR-CMOS
- Not monolithic CMOS
  - Removes problem of sparsified readout from CMOS sensor.
    Needs a readout chip
  - Possible advantages: pixels size, thin collection region (2-hit separation)
- Good old diode sensors, but made in a CMOS foundry on large wafers
  - Advantages: cost and production speed
    (entire sensor production in a few weeks)

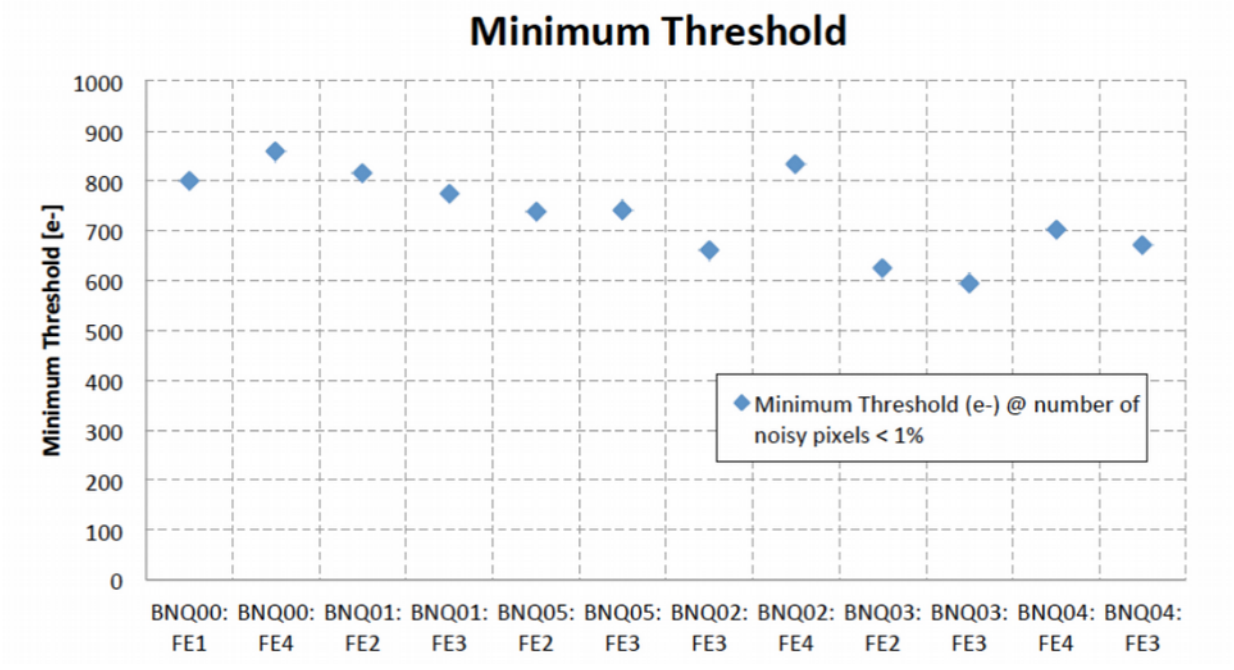
Power Delivery

- CMS Phase 1 upgrade off-chip DC-DC approach does not scale to larger, lower FE voltage HL-LHC detectors
  - (Tavolaro, Mon. 16:50)
- Fully on-chip DC-DC conversion did not have enough R&D effort to mature in time
  - Divide by 2 is easy and is being done in industry. But need to divide by 4 or more for efficient enough low mass distribution.
  - This needed a design and prototyping effort that did not materialize
    Got only as far as proof of concept in 65nm.
- Serial power is the only mature approach left standing
  - Basic regulation elements already used in IBL
  - RD53A chip will contain such regulation fully integrated (Demaria, Thu. 15:10)
  - Performance of modules in serial power chains well demonstrated
  - Full system (from counting room supplies down to modules) still under development. There are open questions (Lehmann [P])

Serial Powered Stave

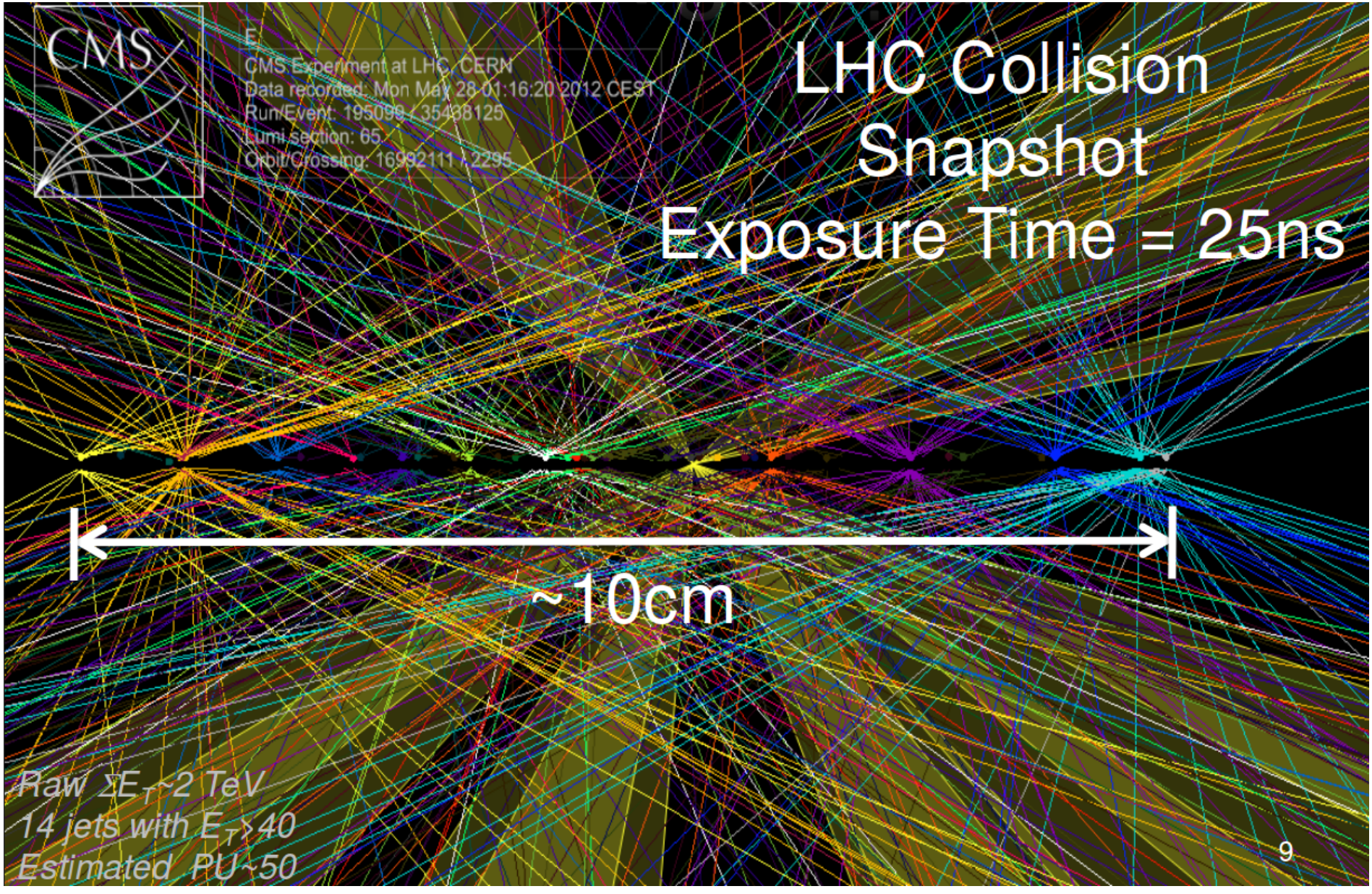
- Presented at ACES 2016
  Courtesy Bonn U. (L. Gonella)





This is
lower than for IBL

Intensity


CMS
CMS Experiment at LHC, CERN
Data recorded: Mon May 28 01:16:20 2012 CEST
Run/Event: 195099 / 35438125
Lumi section: 65
Orbit/Crossing: 16992111 / 2295
LHC Collision
Snapshot
Exposure Time = 25ns
~10cm
Raw ΣE_T~2 TeV
14 jets with E_T>40
Estimated PU~50
9

Intensity Solutions

- Smaller feature size CMOS readout chips
  - This is not because of smaller pixels (will explain)
  - RD53 is 3 years old
    (Demaria, Thu. 15:10, Monteil [P])
- Smaller pixels
  - To avoid In-pixel pileup
  - Also for performance

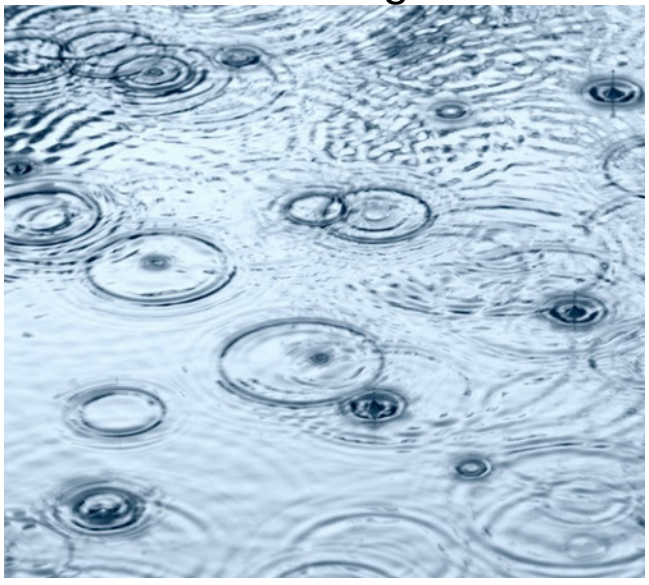
RD53 RAL meeting 2014

- Much higher bandwidth readout
  - Driven by high trigger rate for physics- consequence of high p/u
- More total dose radiation hard chips and sensors
  - Major progress in understanding of damage at high total dose
    (Lange, Macchiolo, Venturi, Linnik @ 16:40; Unno [P], Nakamura [P]; Demaria)
- New approaches to power delivery
  - Serial Power is baseline approach for both ATLAS and CMS
    (related: Lehmann [P])
- New approaches to system stability

Why Smaller Feature Size CMOS?

Particles / Hits

Raining

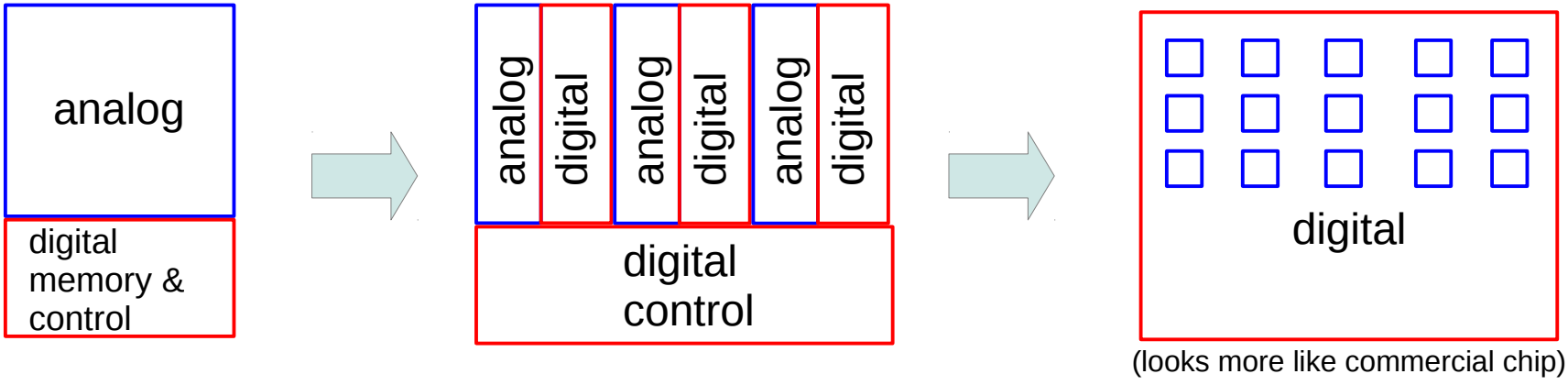


Pouring

Onto detector surface area

* Store full time sequence of drops until trigger (not collect in a bucket)
* Can quantify rate as memory bits / area / time
  (note: no mention of pixel size)

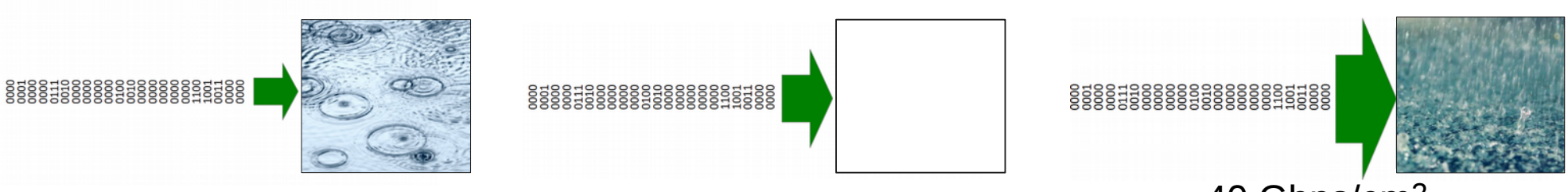
Readout Chip Evolution



10 yrs ago

today

HL-LHC



<1 Gbps/cm^2

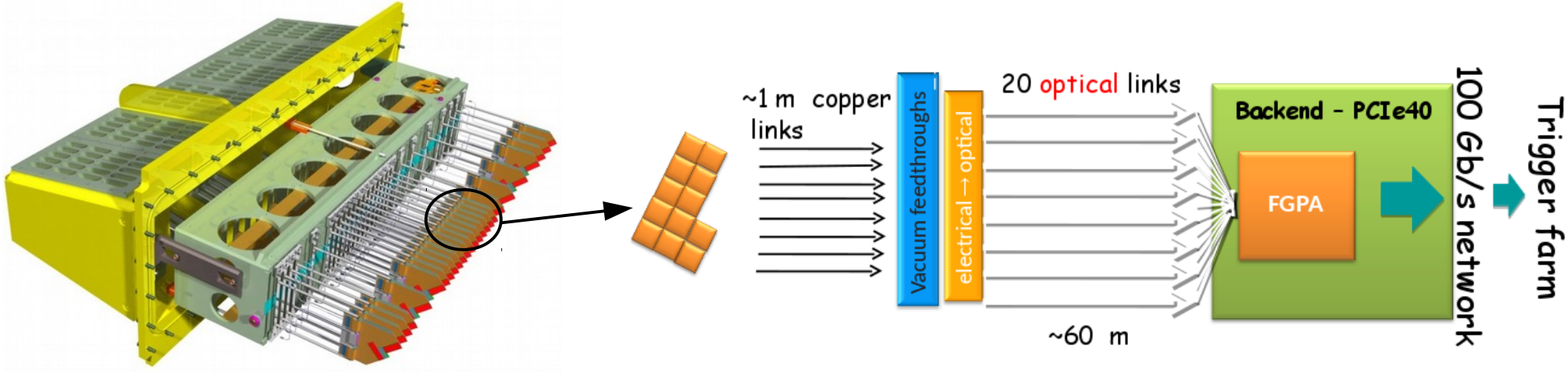
5 Gbps/cm^2

40 Gbps/cm^2

Another way to say memory per unit area: Logic Density.
We follow Moore's Law.

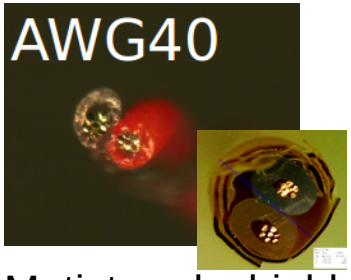
Digression

- If you simply read out all hits then don't need any memory and don't need smaller feature size
- 100% true. LHCb chip with 20Gbps output BW is in 130nm CMOS
  - (van Beuzekom [P])
- Why don't ATLAS and CMS do this?
  - Intensity is 10x higher. Would need 200 Gbps/chip
  - Cable mass is prohibitive in collider geometry
    - Velopix is a fixed target geometry- cables outside acceptance

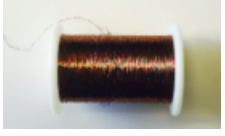


High Speed Readout for ATLAS/CMS

- 5Gbps transmission on long, low mass cables is not easy
  (Morettini, 11:05)
- Enabling technologies under development:
  - Custom cables

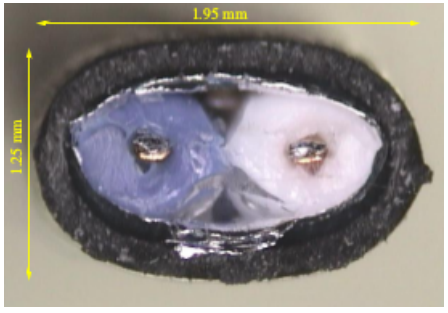


Mutistrand, shielded twisted pair, rad hard



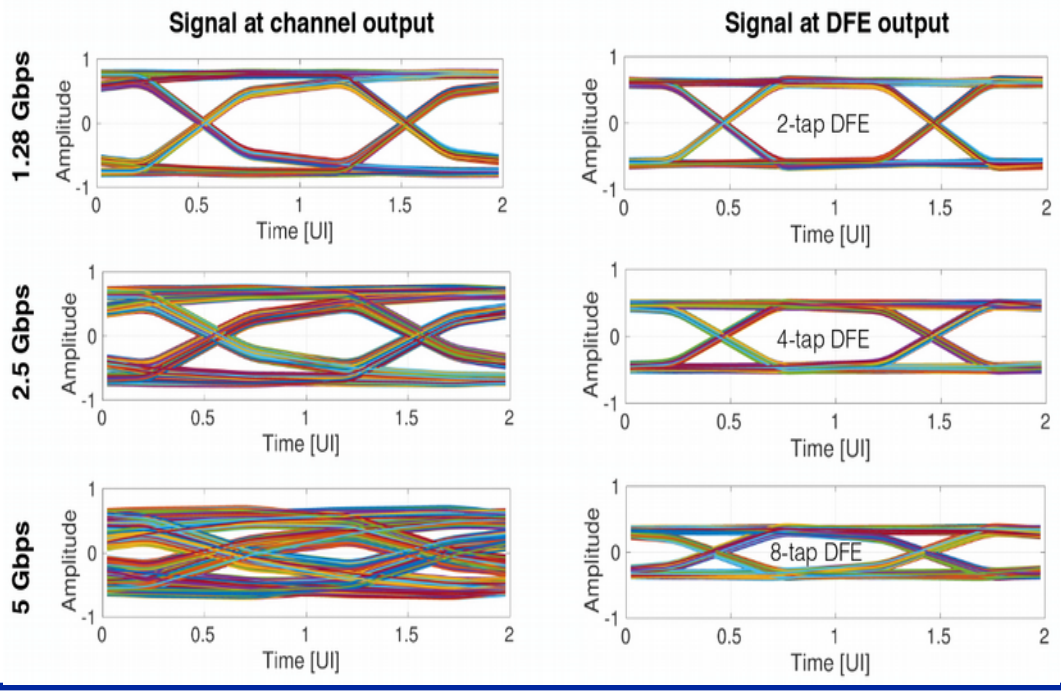
Multiple parallel lanes of unshielded twisted pair

2mm



AWG28 Cu/Al
6m Twinax
Rad hard

  - Adapting commercial techniques
    - Encoding 8b10b, 64b66b
    - Drivers and pre-emphasis
    - Receivers and equalization
    - Commonality with Velopix



Rad Hard Transistor Scaling

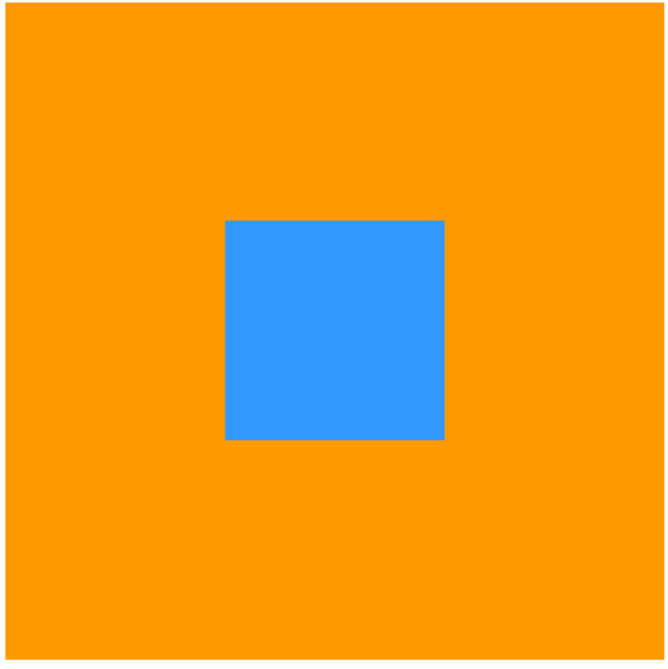
28nm ?maybe for HL-LHC inner layer replacement after 1ab^{-1}?

65nm

Not quite minimum size due to pesky radiation damage
logic density still << 130nm

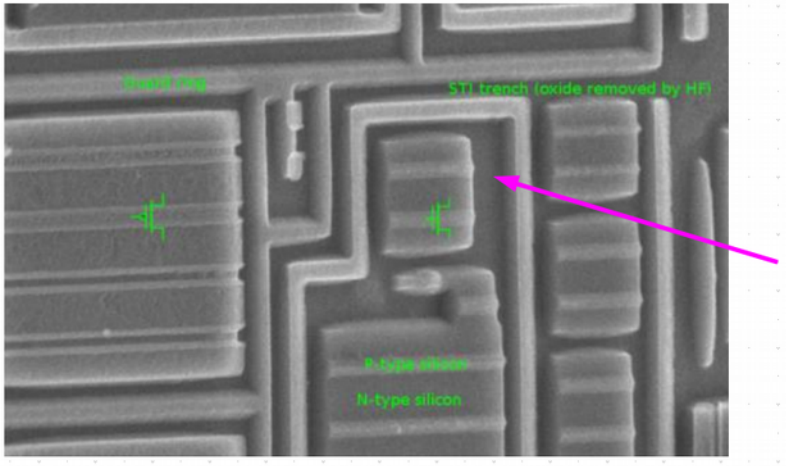
130nm

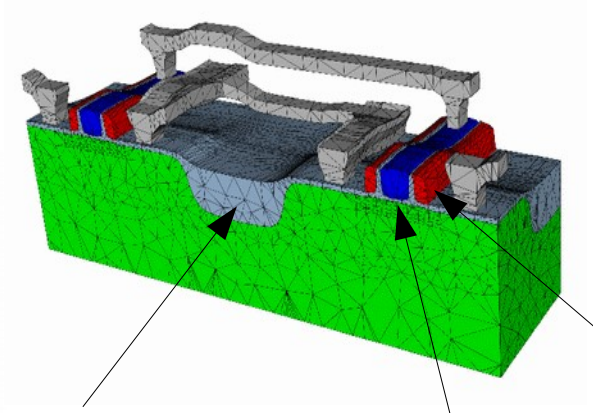
0.25um
ELT



- Huge amount of work done on CMOS radiation hardness
- Quite well understood by now
- Have quantitative simulation models for both analog and digital design
- **BUT, ultimate degradation at high dose depends on temperature and operation history**
  (sounds familiar from sensors?)
- (see Dette, Thu. 15:25 for example of damage evolution with operating conditions at low dose. Not same thing but related)

Meet the oxides: STI, Gate, Spacer

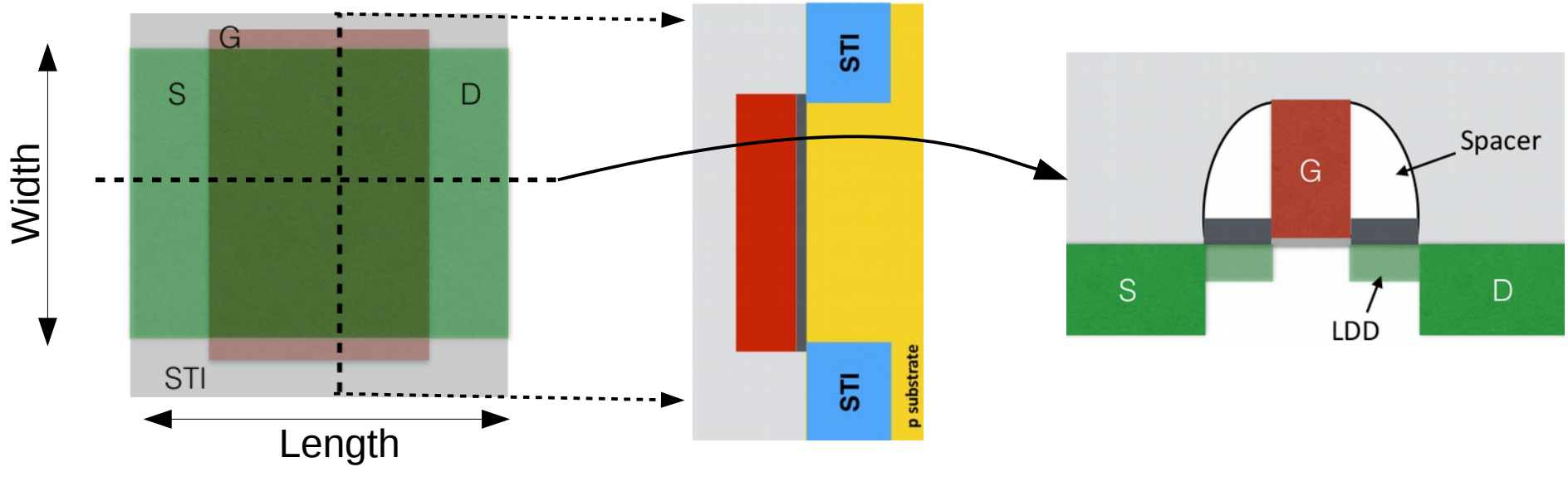




STI (thick)

Gate oxide (thin)

Spacer (thick)

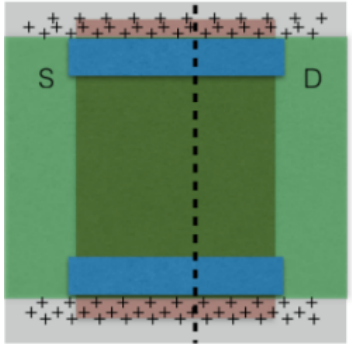


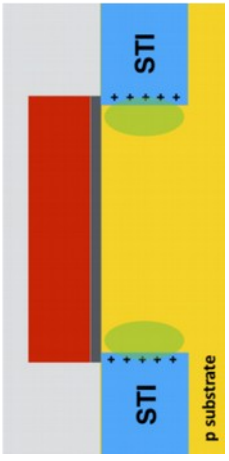
RINCE

Radiation Induced Narrow Channel Effect

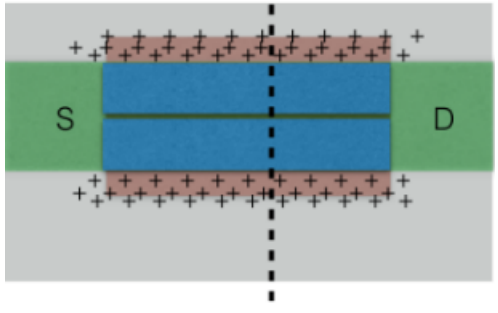
F. Faccio and G.Cervelli, "Radiation induced edge effects in deep submicron CMOS transistors", IEEE Trans. Nucl. Science, Vol.52, N.6 (2005) pp.2413-2420 http://dx.doi.org/10.1109/TNS.2005.860698

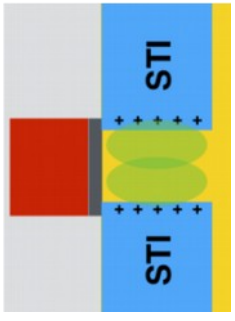
Wide Transistor

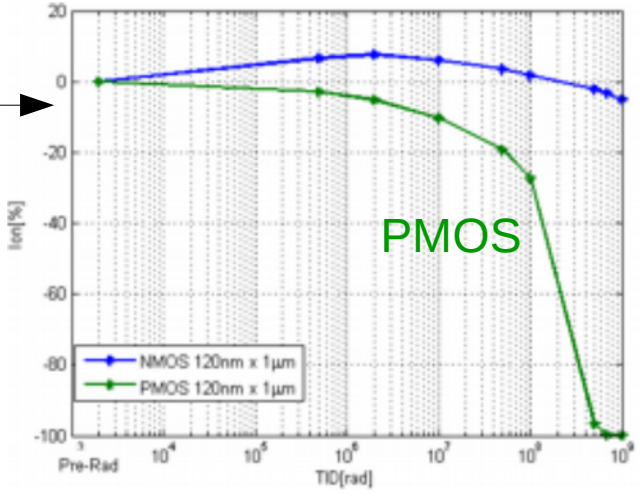




Narrowest Transistor







1Grad

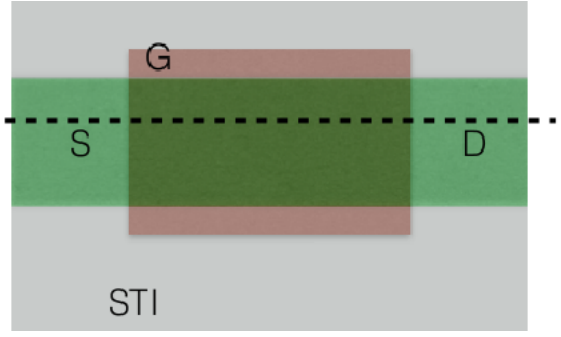
RISCE

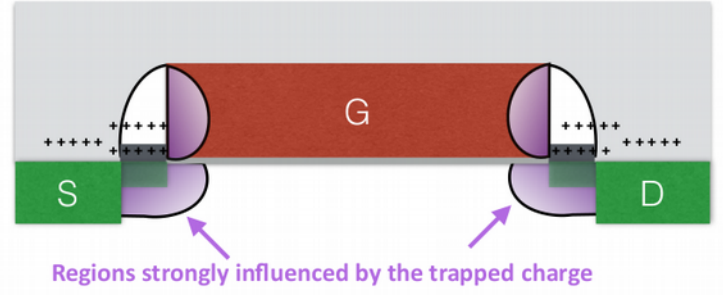
New!

Radiation Induced Short Channel Effect

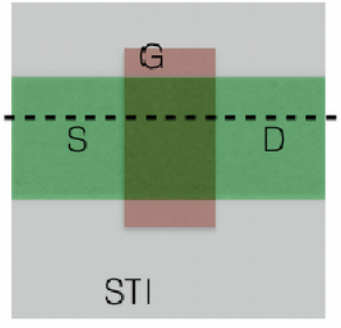
F. Faccio et al., "Radiation-Induced Short Channel (RISCE) and Narrow Channel (RINCE) Effects in 65 and 130 nm MOSFETs," IEEE Trans. Nucl. Science, Vol.62 , N.6 (2015) http://dx.doi.org/10.1109/TNS.2015.2492778

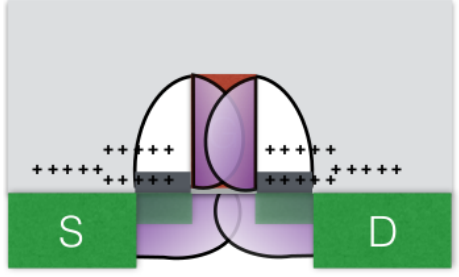
Long Transistor

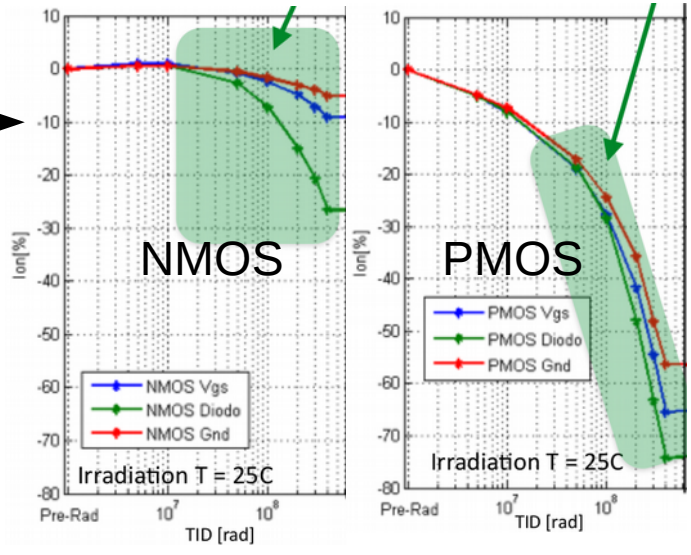




Shortest Transistor

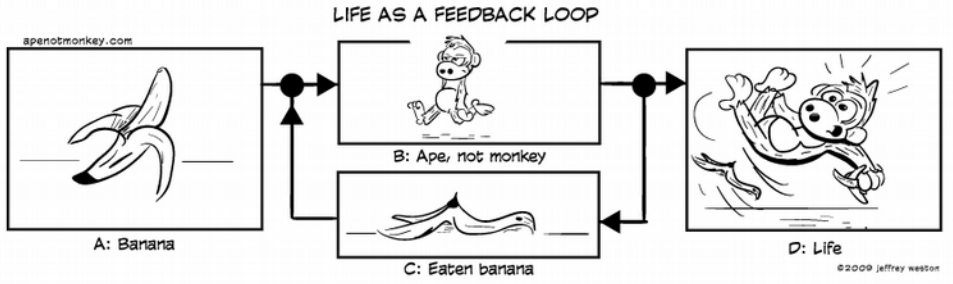


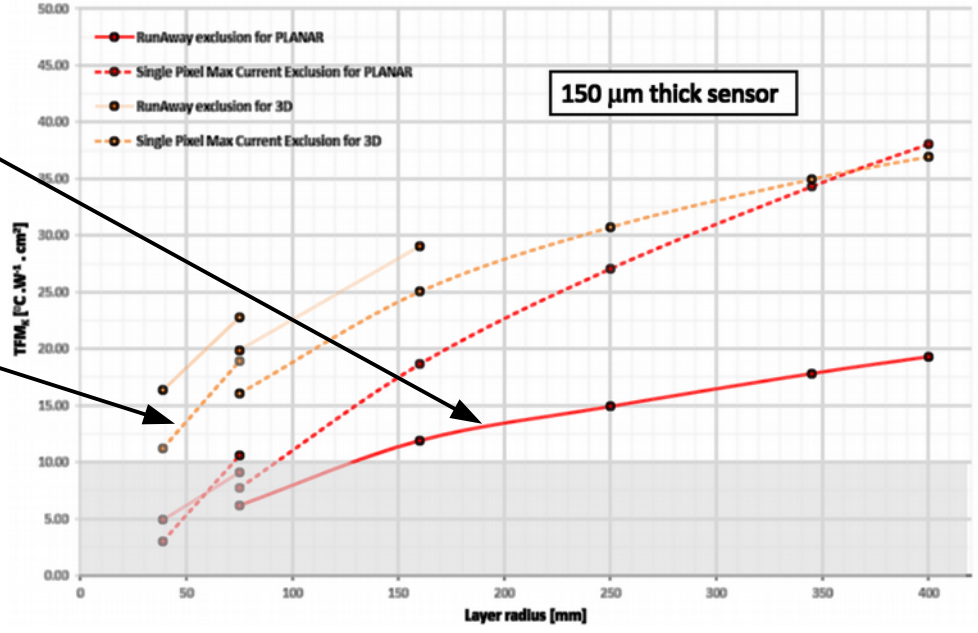




System ~~Sensor~~ Radiation Tolerance

- Sensor lifetime depends on cooling, Cooling is related to support mass, And to chip power.
- Study from ATLAS Scoping doc. thermal runaway vs. cooling performance. Limits planar
- Also shows a leakage current "bound". Limits 3D
- Design feedback, not as clean cut as thermal runaway
  - Charge collection can be sped up with more/bigger electrodes
  - More capacitance needs more chip power
  - More chip power degrades sensor cooling
- A rad hard system is a delicate compromise between sensor, electronics, and mechanics.



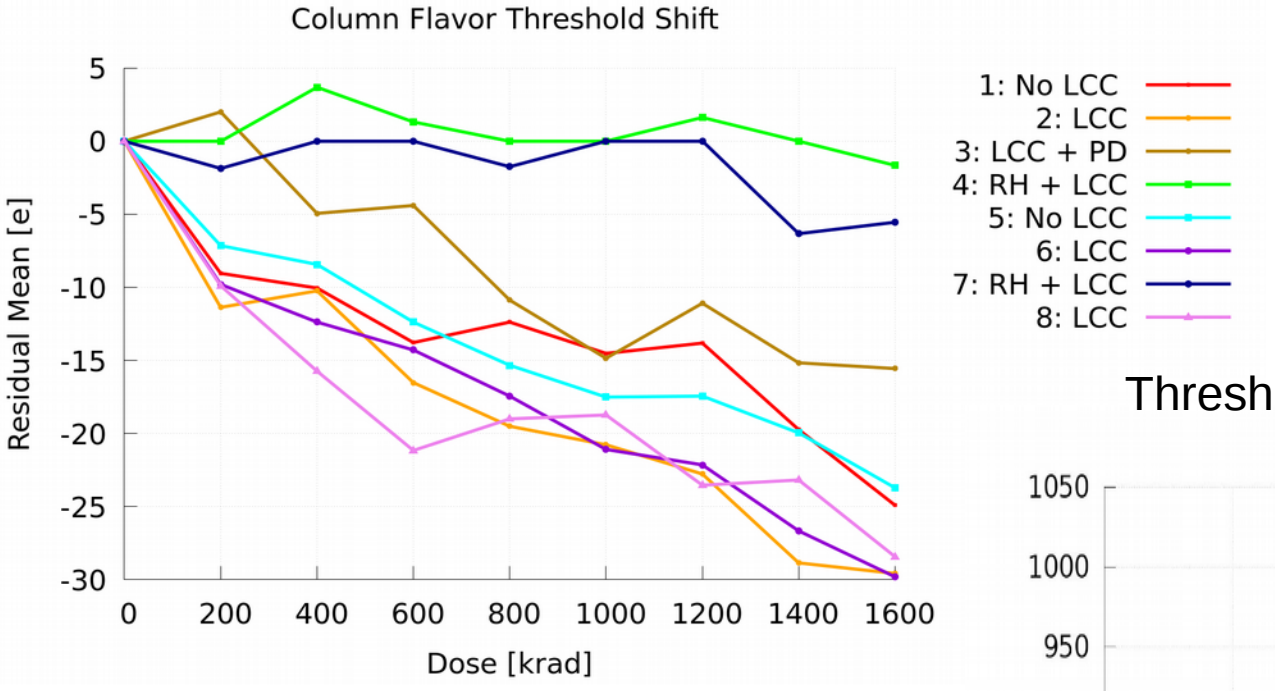


Stable Operation & New Concepts

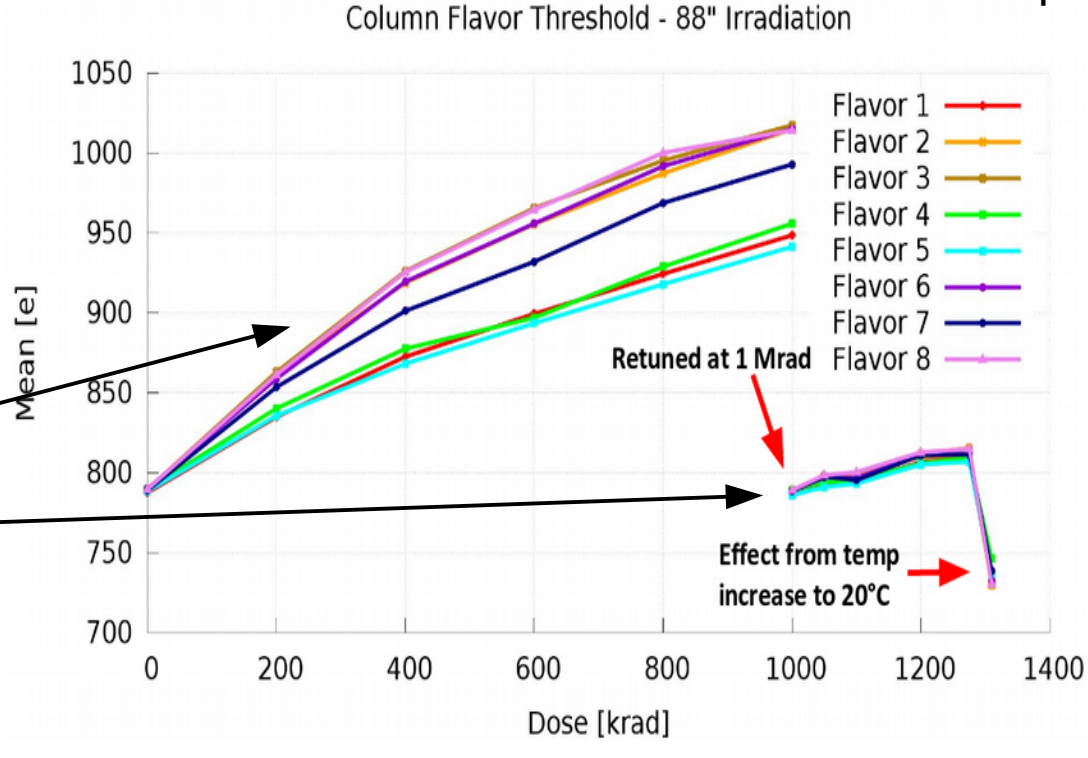
- Small pixel with thin, radiation damaged sensors demand low threshold operation (~600e)
  - This demands a threshold stability better than we have today
- The threats to stable operation are:
  - Temperature variation
  - Power supply fluctuations
  - Radiation (including transient effects and SEU)
- A single run at the HL-LHC will deliver a radiation dose of order 1Mrad to the inner pixel layer
- Power and temperature fluctuations can be reduced by running always at maximum power, rather than throttling with hit/trigger rate as now
  - Cooling must be designed for maximum anyway
- How SEU-hard can configuration memory be made within tiny pixels?
  - Why not just reconfigure all the time during running (trickle configuration) Move persistency off-detector. RD53A will support this mode.

FE65-P2 measured threshold stability

Threshold shift vs dose after 350Mrad



Threshold shift vs dose on brand new chip



10x HL-LHC dose rate

4x HL-LHC dose rate

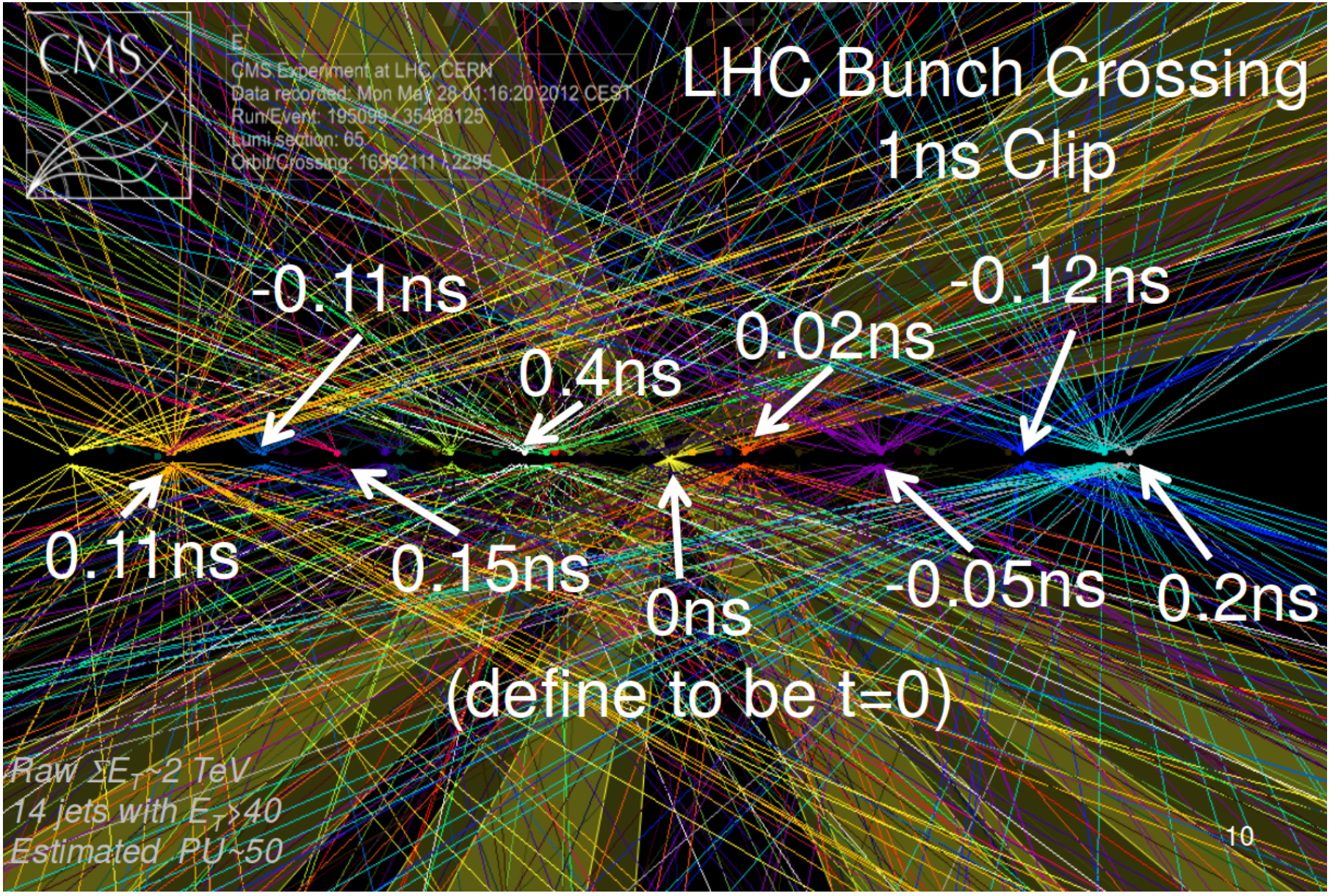
Performance

- Don’t just want to do the same job with larger scale and higher intensity, want to do better!
  - Separation of boosted objects
  - Suppression of pileup activity
  - Higher rapidity coverage
  - Much higher trigger rate
    (all events look the same at high p/u)
  - Lower mass
  - Faster pattern recognition
- Given signal, capacitance, transconductance: all is determined.
  - How to do better than what is possible?
  - Cheat. Measure new information in real time

Performance

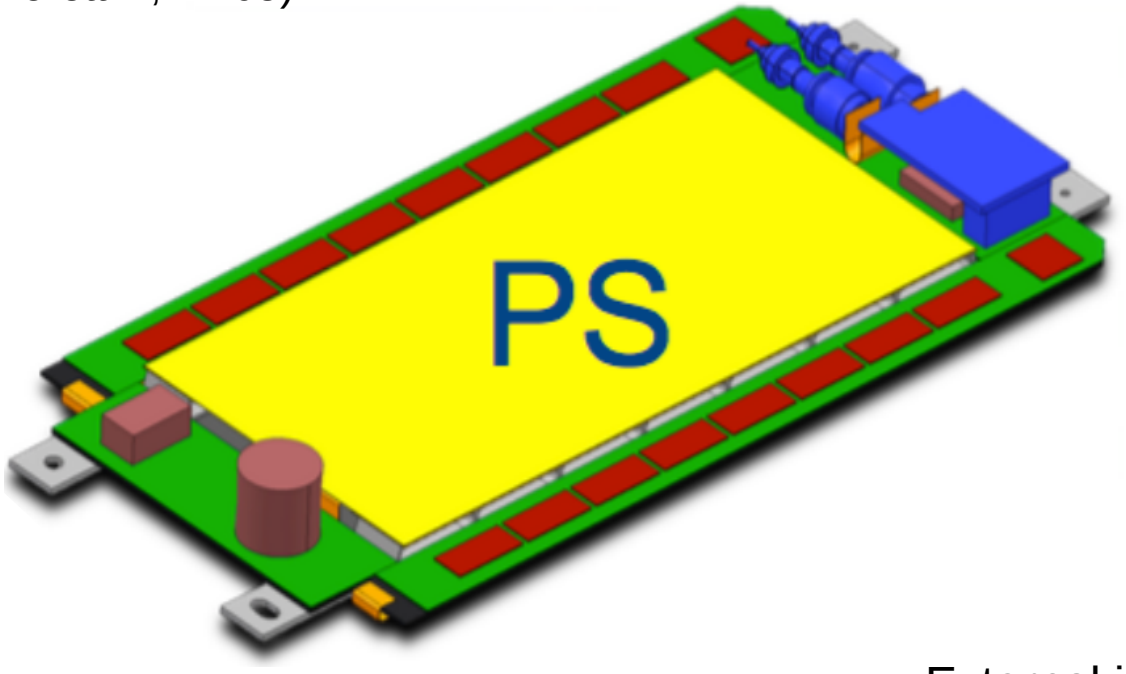
- Don't just want to do the same job with larger scale and higher intensity, want to do better!
  - Separation of boosted objects → Higher granularity yes, but can go further using clusters (Mansour, 9:15)
  - Suppression of pileup activity → Z-vertex separation (Smart, Migliore), timing (Seiden, Cartiglia; Mon., Neri, 12:10, Mulargua [P])
  - Higher rapidity coverage → Innovative layouts (Smart, Migliore) Which need lighter services!
  - Much higher trigger rate (all events look the same at high p/u) → Readout, track triggers Morettini, Kornmayer, Neri, 11:05)
  - Lower mass (also services) → Better cooling, new materials (Anderssen, Verlaat, Fri. 9, 10)
  - Faster pattern recognition → Dedicated hardware, Use more information (clusters shapes, timing)
- Given signal, capacitance, transconductance: all is determined.
  - How to do better than what is possible?
  - Cheat. Measure new information in real time

New Info: Fast Timing



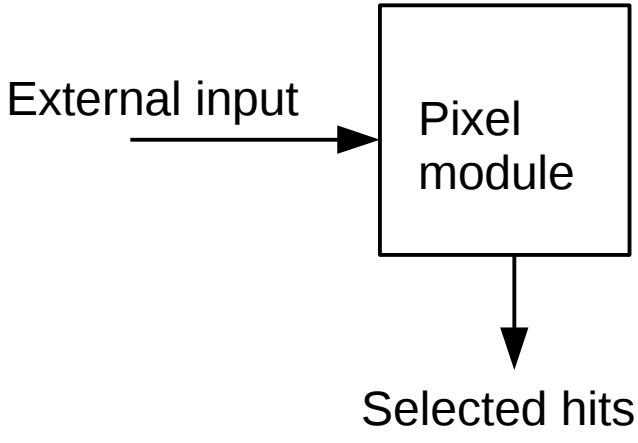
New Info: 2-Layer Correlations

(see Morettini, 11:05)



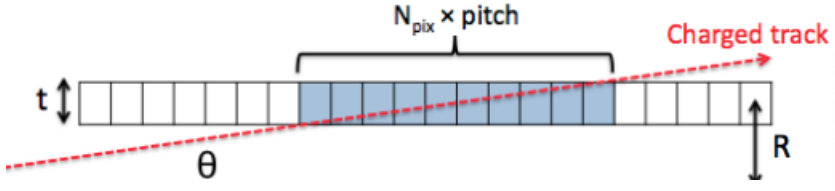
CMS track trigger
Pixel-Strip module

What is it really?

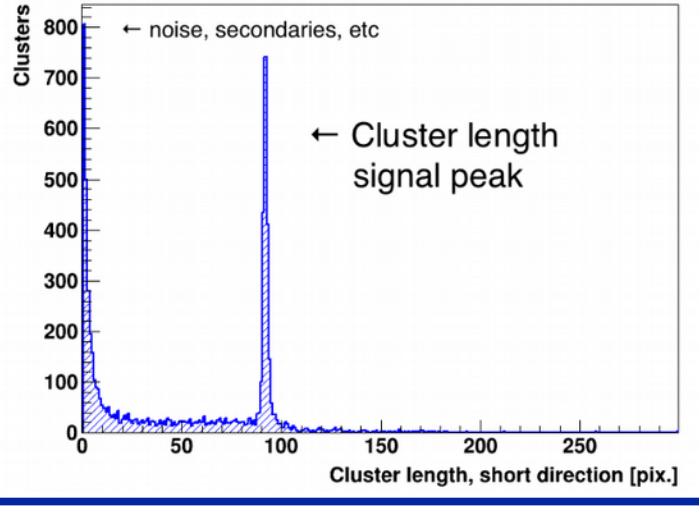


New Info: Cluster internal D.O.F.

- Pattern recognition is currently based on space points. Each space point is a priori equal => all combinations are equally valid
- Internal degrees of freedom, eg. if hits came in red, green, blue, reduce problem to combinations of like hits.
  - Timing we talked about
  - Direction (vectors not points) allows filtering for pT triggers
  - Cluster properties provide another handle, if clusters have enough structure (ie. are big enough) to allow meaningful classification



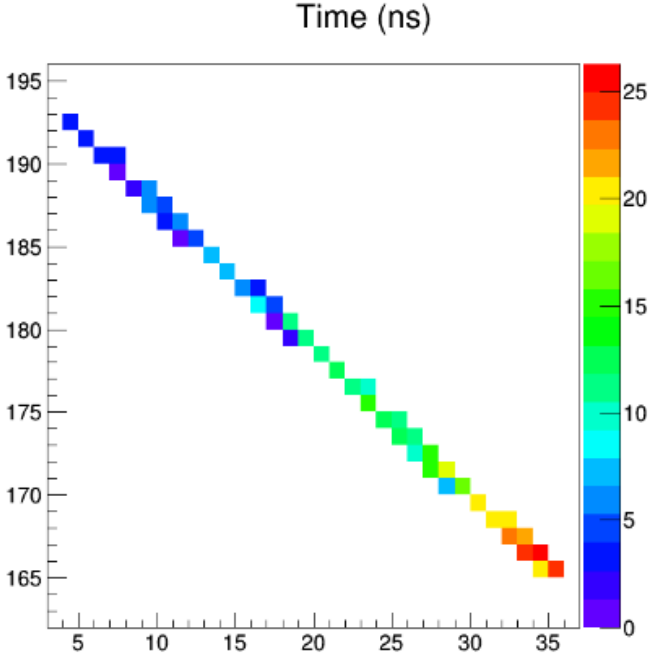
Test beam data



(S. Viel, Hiroshima 2015)

New Info: 3D clusters

- New developments may allow to cluster in 3D within a sensor, which would make for richer, more vector-like instead of point-like hits.
- Timepix 3 already can do this using drift time
- Natural in gaseous pixel detectors such as GOSSIP
- Can also do it geometrically? 3D, 3D sensors, for example with different depth columns



Track through Timepix 3 module w/300u sensor.
(M. Campbell, Imaging2016)

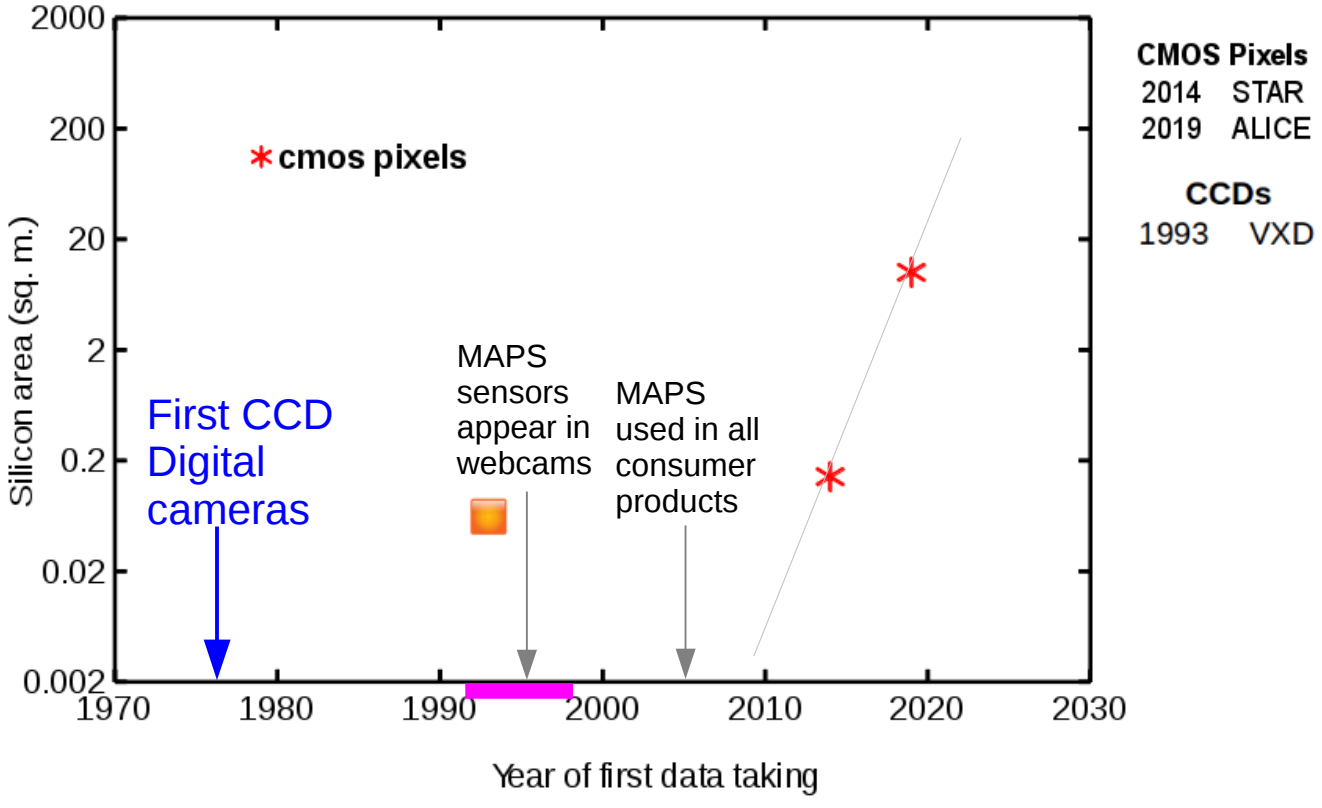
Low Mass Revolution

- Two main enabling technologies for HL-LHC:
  - CO_2 Evaporative Cooling
  - High thermal conductivity materials and adhesives
    - Critical for CO_2 cooling: need to concentrate heat onto tiny cooling tube to take advantage of CO_2
- Mass of meter-long CO_2 cooled supports starting to rival air cooled, short, STAR structures!
  - Don’t miss Friday AM session

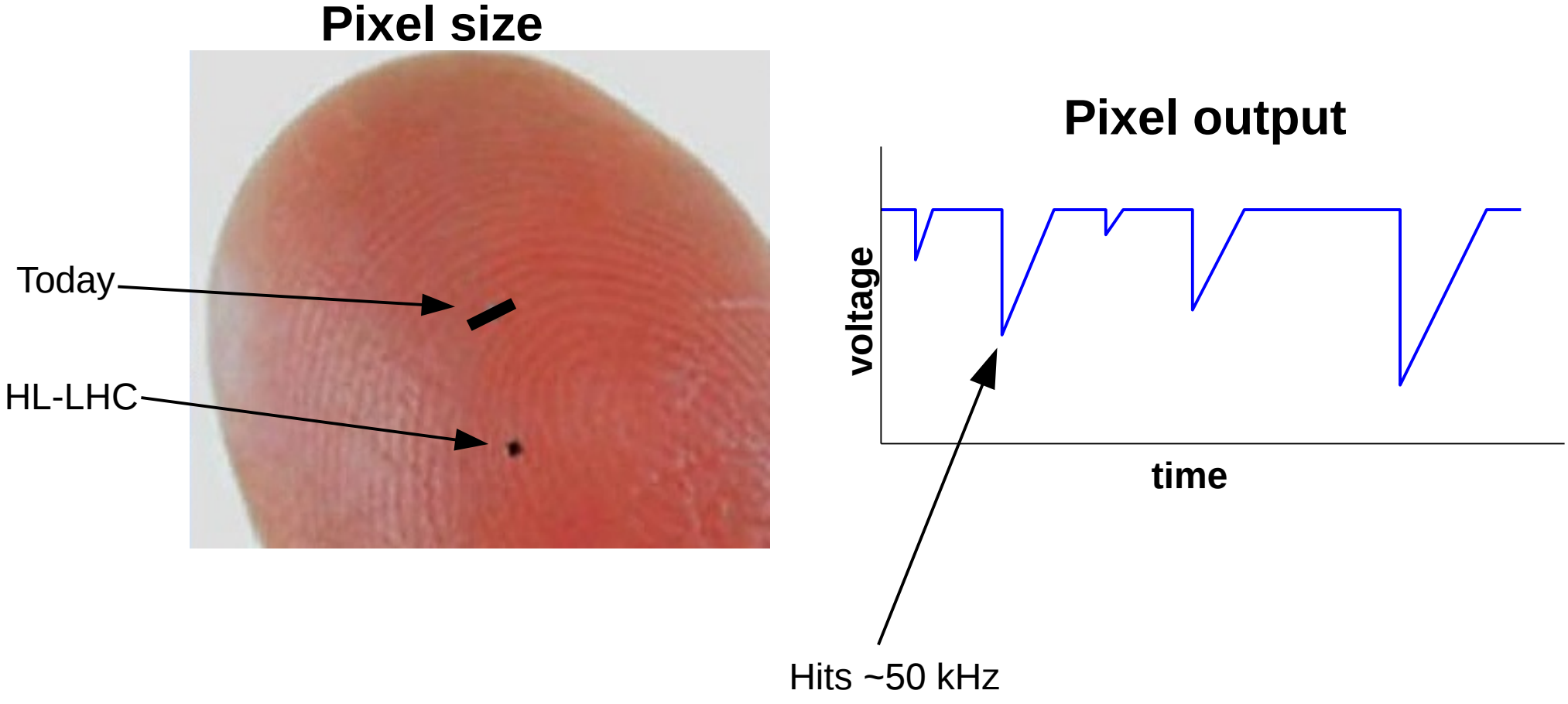
Conclusions

- Scale
  - Can build better hybrid detectors for lower cost, but not yet at the end
  - Watch list: larger sensor wafers, CMOS fabs, wafer scale integration
  - How can ATLAS, CMS take advantage of CMOS sensors?
- Intensity
  - Rad hard small pixel sensors and 65nm electronics maturing fast
  - Very active R&D on faster collection, fast timing
  - High speed readout and serial power distribution under development
- Performance
  - Low mass mechanics- wow!
  - Very active field looking for gains “outside the single pixel”
    Fueled by advances in scale and intensity work

B A C K U P


2000
200
20
2
0.2
0.02
0.002
Silicon area (sq. m.)
cmos pixels
First CCD
Digital
cameras
MAPS
sensors
appear in
webcams
MAPS
used in all
consumer
products
1970
1980
1990
2000
2010
2020
2030
Year of first data taking
CMOS Pixels
2014 STAR
2019 ALICE
CCDs
1993 VXD

Single Pixel Perspective



- For 50um x 50um HL-LHC pixels up to 3Ghz / sq. cm. In ATLAS / CMS
- Need to save these hits FOR ENTIRE TRIGGER LATENCY (12µs up from 6µs)