CMS Pixel Detector design for HL-LHC

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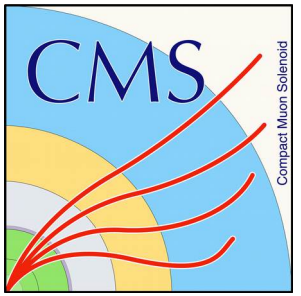
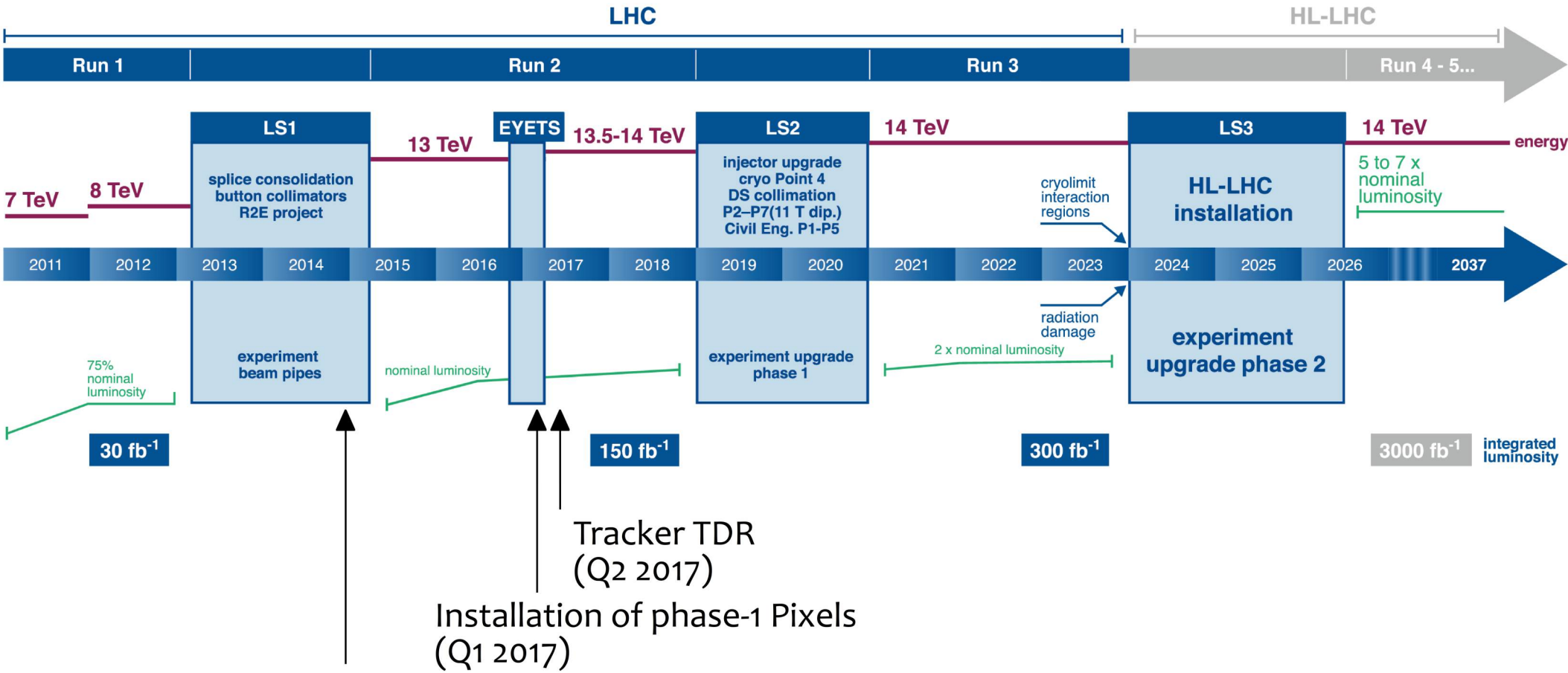
on behalf of the CMS Collaboration



The High-Luminosity LHC



Tracker TDR
(Q2 2017)

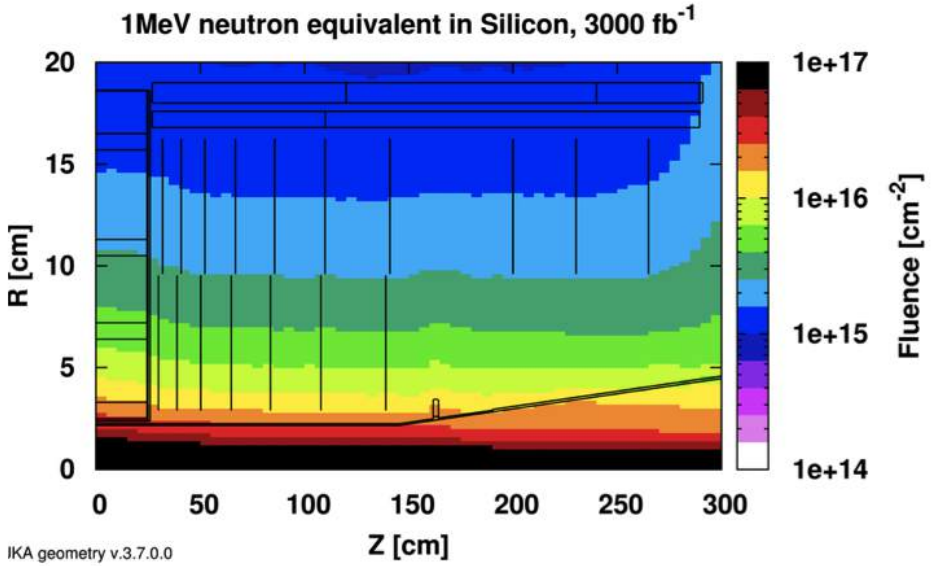
Installation of phase-1 Pixels
(Q1 2017)

CMS Technical Proposal
& Scope Document
(Q2/Q3 2015)

- In what follows I will recap the main design concepts of the Inner Pixel described in TP underlining new developments in view of the TDR.

The CMS Tracker in the HL-LHC scenario

- Higher luminosity → more harsh radiation environment:



  - integrated luminosity: 3000 fb^{-1}

    → radiation tolerance: up to $2x10^{16}$ n_{eq}/cm^2 in Si (→ sensors)

    up to in 10 MGy SiO_2 (→ electronics)

    current Tracker designed for 500 fb^{-1} and $1x10^{15}$ n_{eq}/cm^2

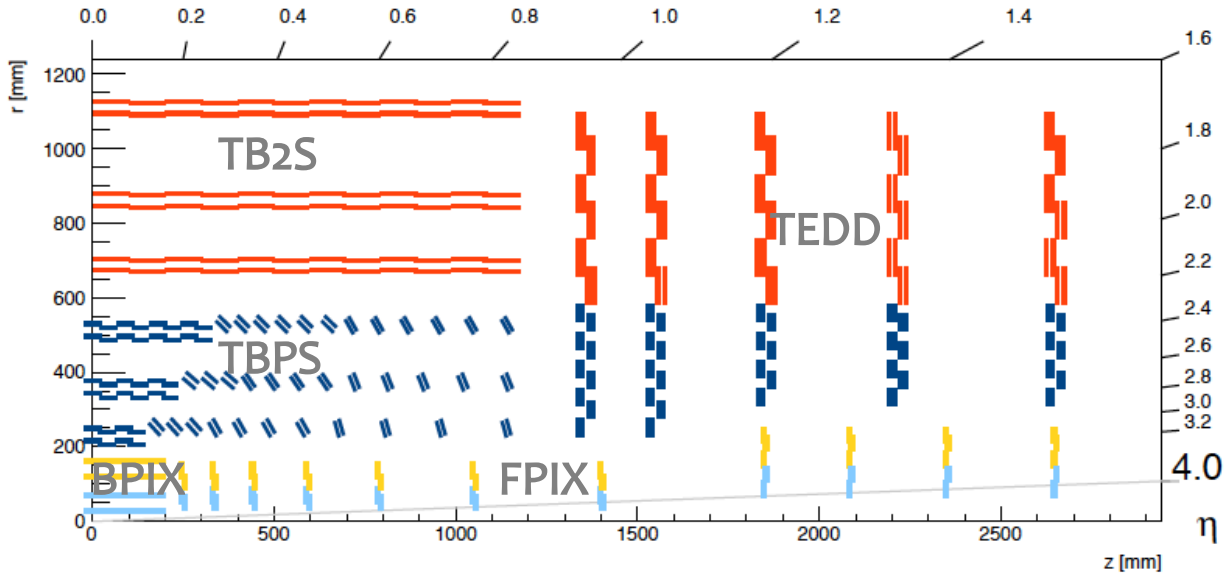
  - instantaneous luminosity: $7.5x10^{34}$ $cm^{-2}s^{-1}$ and <PU>≈200

    → charged particles rate up to 750 MHz/cm^2 (or hit rate up to 3 GHz/cm^2)

    current Tracker designed for <PU>≈50

    CMS foresees a complete replacement of the Tracker!

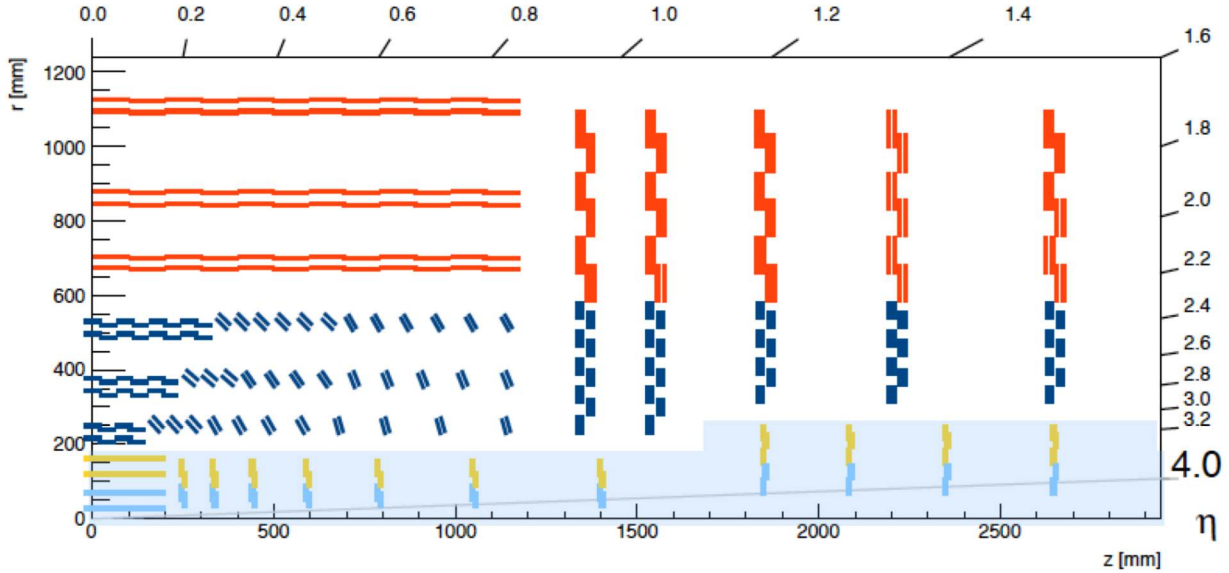
The CMS Tracker in the HL-LHC scenario



- Additional functional requirements for the overall Tracker:

REQUIREMENT	MOTIVATION
extended coverage	contribute to pileup mitigation (PF) up to |η|~4
high granularity	robust two track separation in high energy jet
low material budget	improve tracking performance/momentum resolution measurement
measure pT>2 GeV tracks at 40 MHz	contribute to L1 trigger
deep front end buffers and higher readout bandwidth	compatible with 12.5 μs L1A latency and 750 kHz L1A trigger rate

The CMS Tracker in the HL-LHC scenario



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measure pT>2 GeV tracks at 40 MHz	contribute to L1 trigger
deep front end buffers and higher readout bandwidth	compatible with 12.5 μs L1A latency and 750 kHz L1A trigger rate

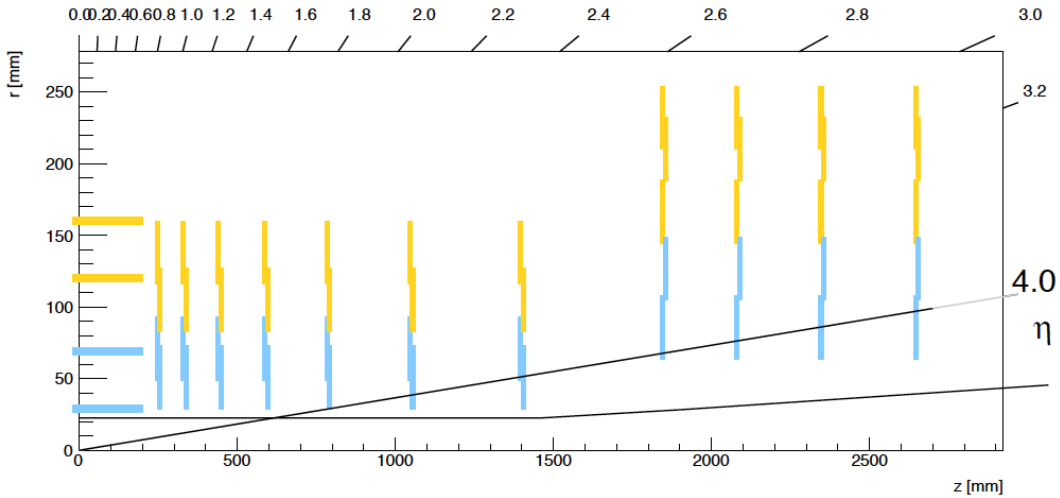
They all have implications on the design of the Inner Pixel!

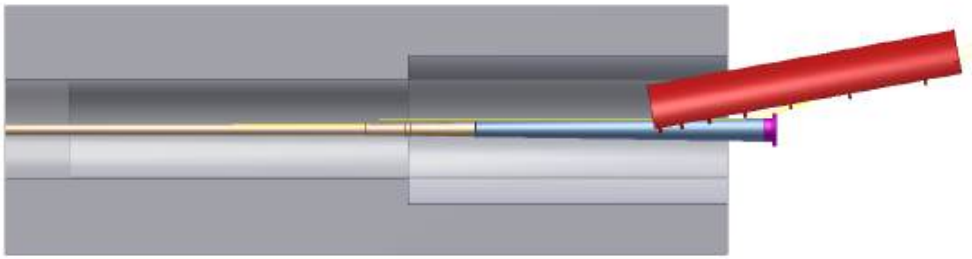
Extended coverage (Inner Pixel Layout)

Inner Pixel layout driving concepts

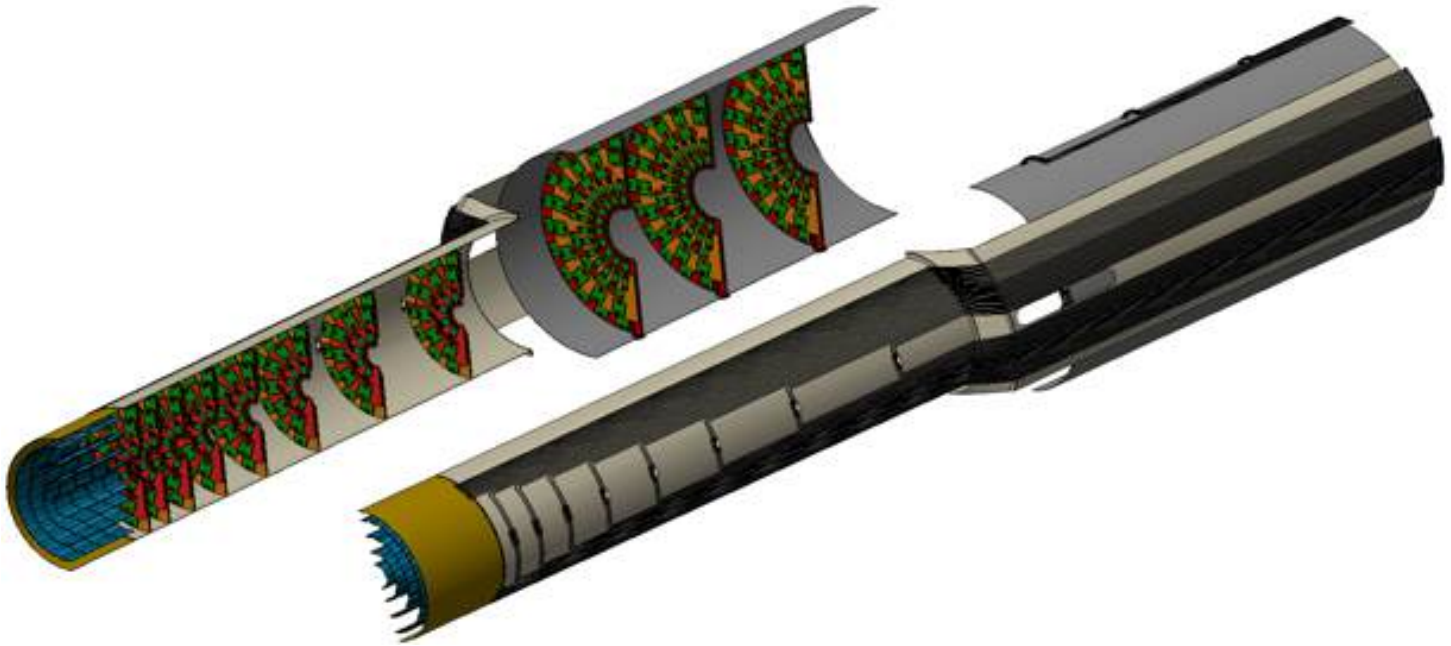
- Coverage of geometrical acceptance:
  - barrel: 4 layers a-la phase-1
    r_1=2.9 cm, r_4=16.0 cm
    but shorter
    z_{max}=±20 cm instead of z_{max}=±27 cm
  - forward: coverage at large |η| obtained by increasing the number of discs (11+11)
    z_1=±25 cm z_{11}=±265 cm

    Total: ~4.5 m^2 of Si
- Simple mechanics:
  - no turbines/blades in the FPIX discs
- Step in the pixel envelope (r=20 cm → r =30 cm at z=160 cm) to allow the installation of the central section with beam pipe in place.





Developments of the system mechanics



- Support tube(s) divided into half-cylinders consisting of two volumes each:
  - barrel + small discs
  - large discs
- Installation of the barrel+small discs section using temporary rails that will be removed before the insertion of the large discs.

High granularity
(Design of the sensors)

Sensors design driving concepts

- Current baseline: planar sensors
  - n-on-p substrate — current detector n-on-n
  - thin sensors (100 μm ≤d≤200 μm) — current detector 285 μm
  - small pitch pixel cell (2500 μm^2 area) — current detector 15000 μm^2 area

- Usage of 3D sensors is an option for the layers more exposed to radiation damage.

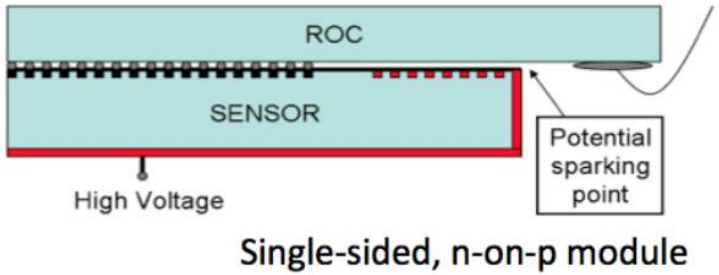
  Sensors with small pitch 3D pixels available (from CNM and FBK).

  Currently processed for bump-bonding of the readout chip.

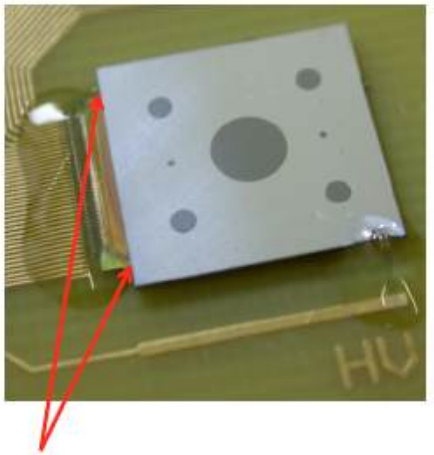
Sensors design driving concepts

- Current baseline: planar sensors
  - **n-on-p substrate**
    - compared to p-on-n: no excess noise after $1x10^{15}$ n_{eq}/cm^2
    - compared to n-on-n: more cost effective

    Challenge: protection against potential sparks between the ROC (at ground) and the sensor at the sensor edge.



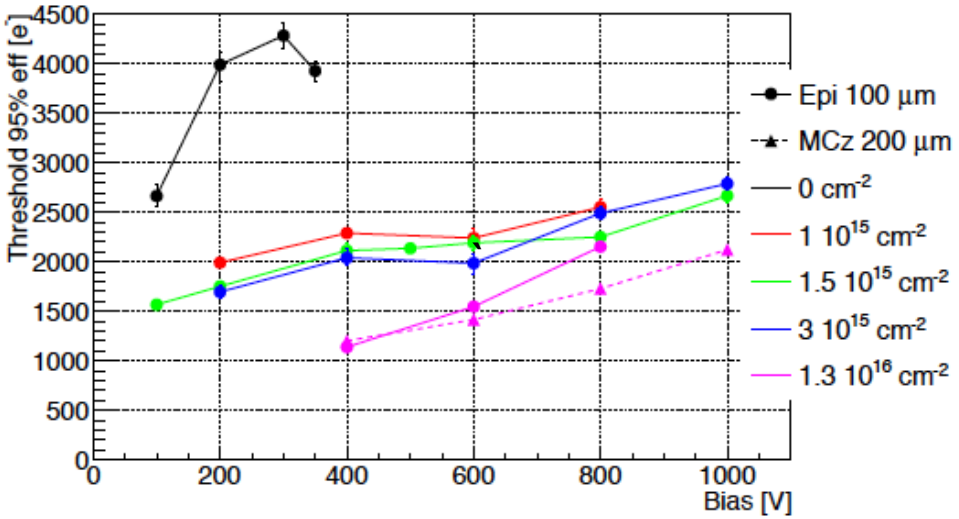
Single-sided, n-on-p module

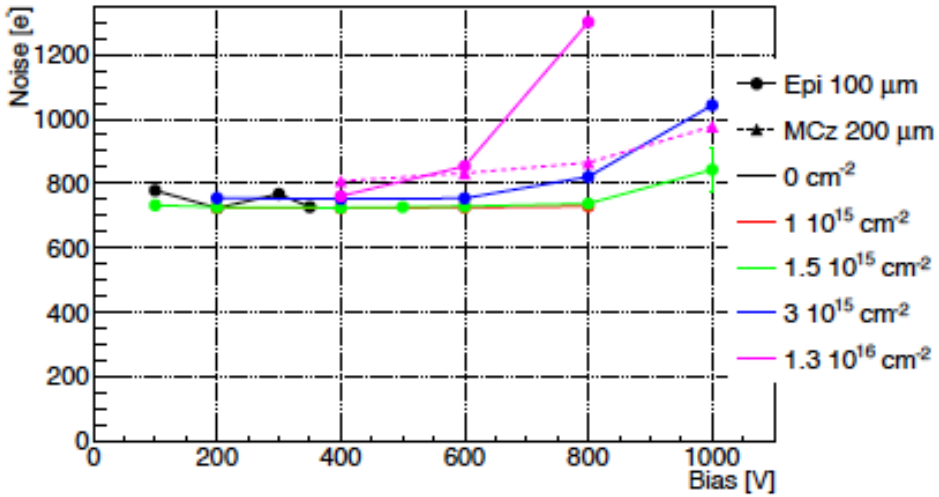

Critical sparking points for n-in-p planar pixels

    Two options: "in-process" benzo-cyclo-butene deposition before dicing or "post-process" parylene coating of the full module still open.
  - thin sensors (100 μm ≤d≤200 μm)
  - small pitch pixel cell (2500 μm^2 area)

Sensors design driving concepts

- Current baseline: planar sensors
  - n-on-p substrate
  - **thin sensors (100 µm ≤d≤200 µm)**





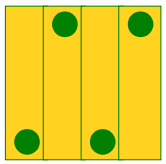
- 100 µm thick sensors after irradiation 1.3x10^{16} n_{eq}/cm^2 collect the same charge (~5000 e) as 200 µm thick sensors but at lower voltage

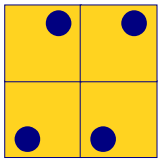
  Challenges: sensor bowing, small signal (~7500 e) already before irradiation, possible soft breakdown (need to find a good combination of sensor thickness & bias voltage).

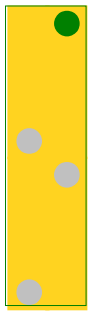
- small pitch pixel cell (2500 µm^2 area)

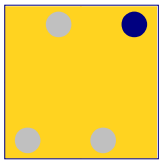
Sensors design driving concepts

- Current baseline: planar sensors
  - n-on-p substrate
  - thin sensors (100 µm ≤d≤200 µm)
  - **small pitch pixel cell (2500 µm² area)**
    - It allows several aspect ratios (small: 25x100 µm², 50x50 µm²; large: 50x200 µm², 100x100 µm²) to be read out by the same ROC.
      Power saving if channels not read out are properly configured.

25x100 µm² rectangular 

50x50 µm² square 

50x200 µm² rectangular 

100x100 µm² square 

  - **Challenges:**
    - not enough room for p-stop for individual pixels
    - not enough room for conventional biasing scheme for testing the sensor before assembly

Sensors developments

- Intense R&D program (measurements before/after irradiation) in next two years also thanks to the ROCs (PSI46digi, ROC4Sens*, RD53A*) that will be available for the tests.

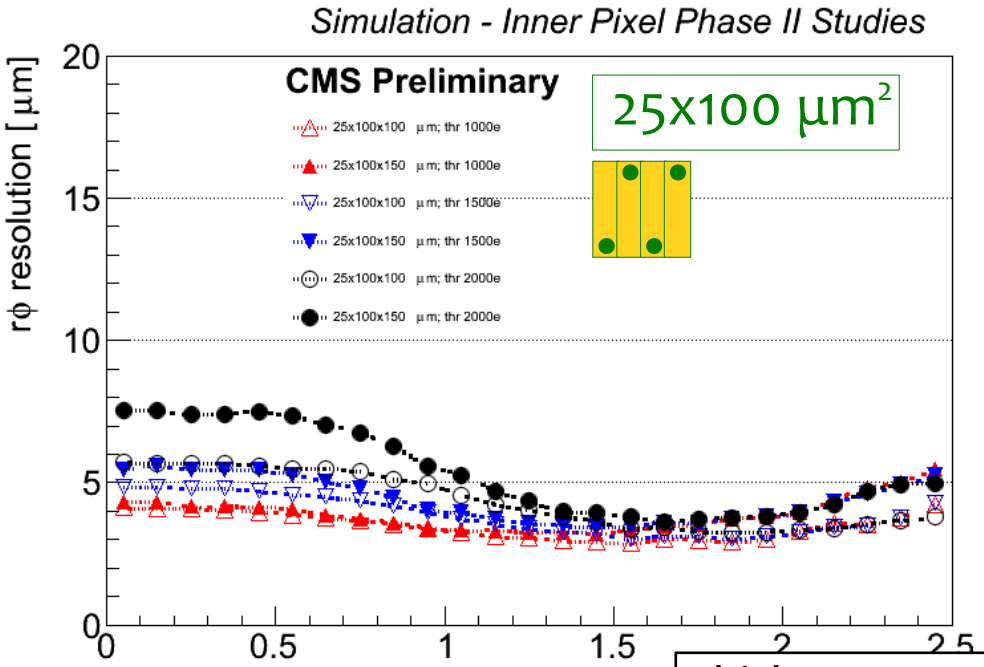
  * specific for 2500 μm^2 pixels

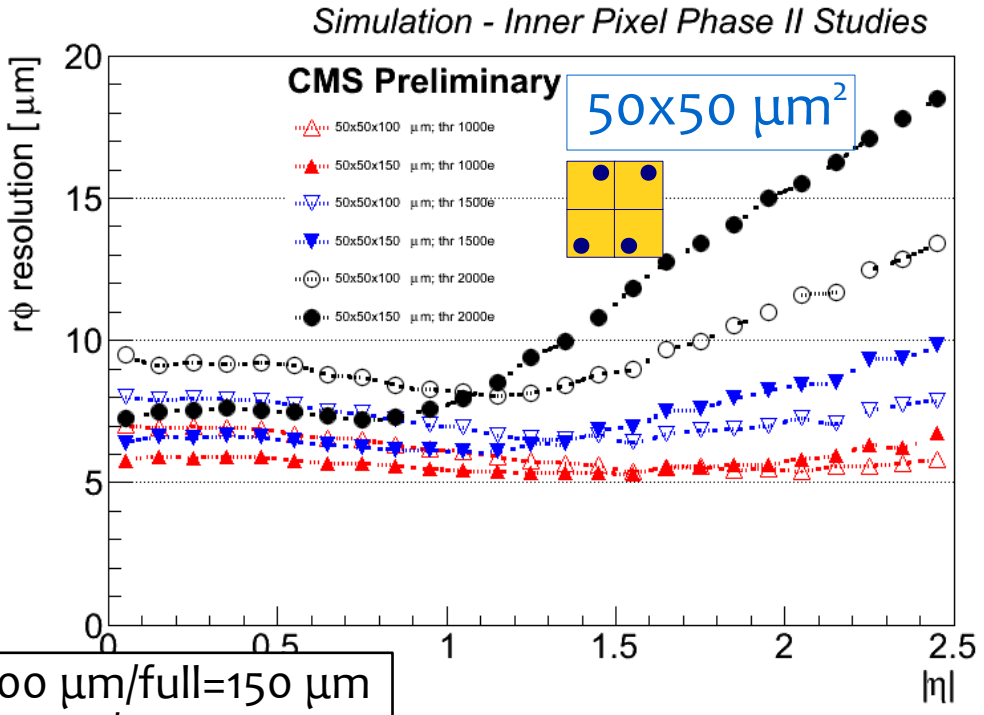
  - HPK submission:
    6" wafers, n-on-p, 150 µm thick, ρ=1-5 kΩ·cm, [O] = $1x10^{16}$-$6x10^{17}cm^{-3}$
    - effect of metal overhang on IV stability
    - common p-stop vs. p-spray pixel isolation
    - spacial resolution of 50x50 μm^2, 25x100 μm^2 and 25x100 μm^2 (bricked) cells

    } minimal program for TDR
  - INFN-FBK submission(s):
    6" wafers, n-on-p, 100-130 µm active thickness, ρ>3 kΩ·cm
    - biasing scheme (punch-through vs. no punch-through)
    - spark protection (BCB) studies
    - test different post-processing thinning procedures
    - bump bonding: SnAg (IZM Berlin) and Indium (SELEX Rome)
  - SINTEF submission:
    n-on-n, 300 µm active thickness
    - slim edge (active area 210 µm from diced edge)
    - slim pixels 25x600 μm^2

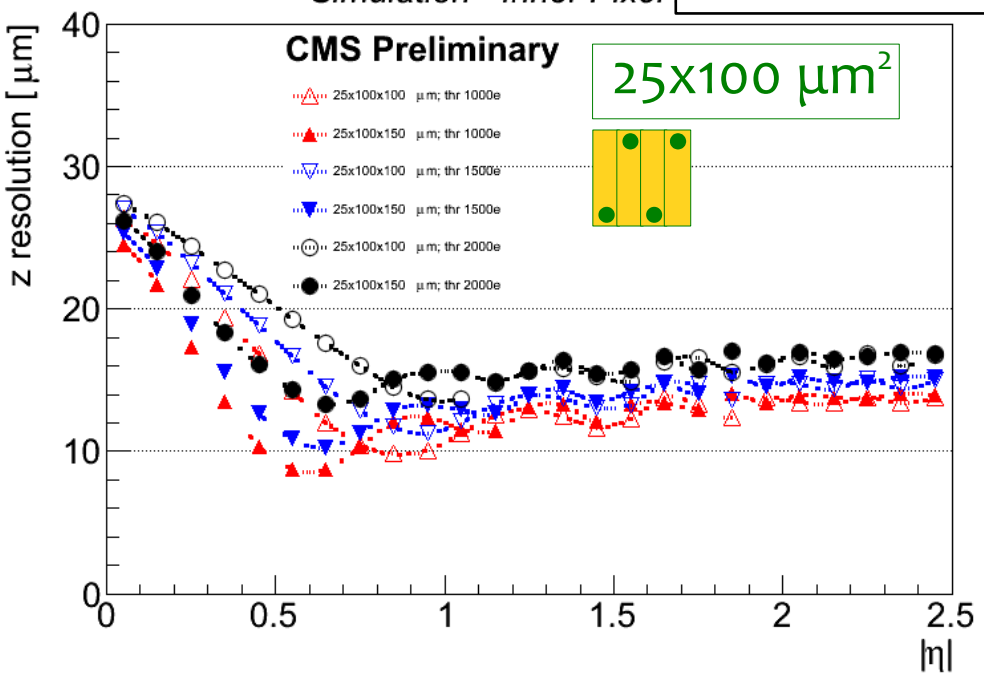
Sensors developments

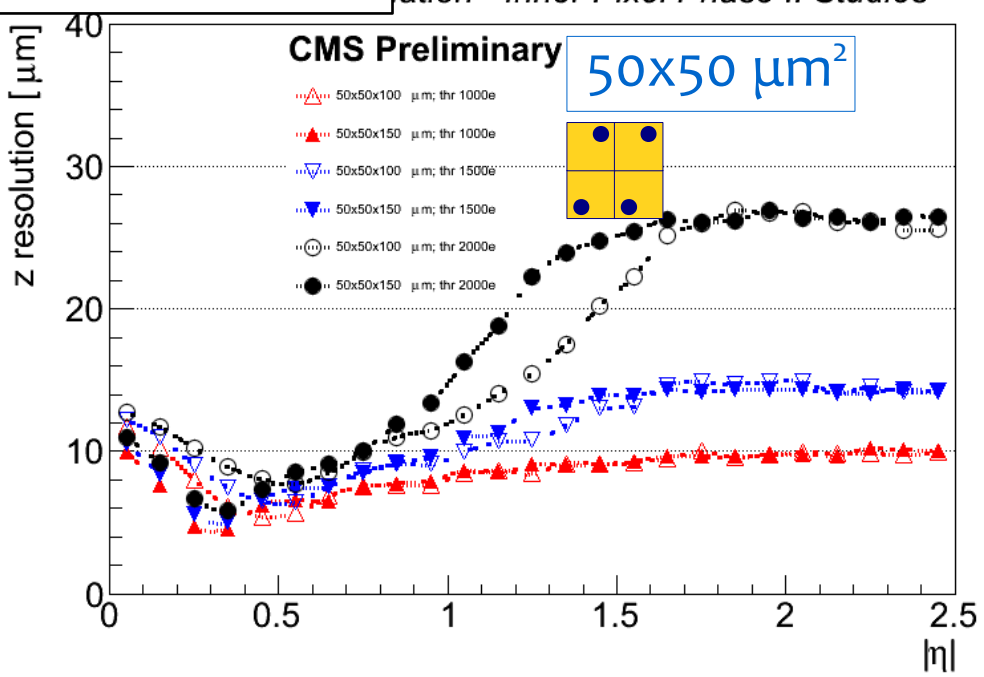
- Preliminary indications from full-simulation studies on the aspect ratio:
  in BPIX better performance of rectangular pixels compared to square pixels:





thickness open=100 µm/full=150 µm
threshold 1000e/1500e/2000e





Sensors developments

- Preliminary indications from full-simulation studies on the aspect ratio:
  in BPIX better performance of rectangular pixels compared to square pixels:
  - square pixels more prone to cluster breakage if thresholds not low enough (25x100 μm^2 better/comparable resolution than 50x50 μm^2 almost everywhere)
  - square pixels aggravate bandwidth requirement (+30%) at the edge of the barrel

Low material budget
(Readout electronics and services)

Readout electronics driving concepts

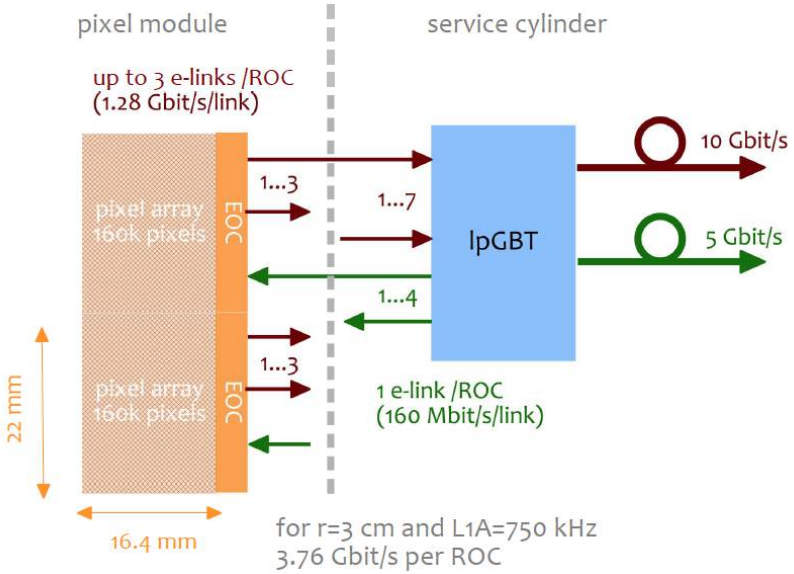
- Requirements on the pixel readout chip (ROC)
  - radiation tolerance (5+5 MGy)
  - driven by the design of the sensor:
    - small cells (2500 μm^2) in a large (4 cm^2) chip → high density of transistors
    - small cells (2500 μm^2) and thin sensors giving small signals → low noise (<1200e)
  - driven by CMS trigger & DAQ:
    - deeper buffer to accommodate 12.5 μs latency
    - faster readout to withstand 750 kHz L1A trigger rate

  Baseline: ROC in 65 nm technology based on common ATLAS+CMS RD53 developments. (see N.Demaria's talk on Thursday)

- Aspects of the overall Inner Pixel system:
  - modularity and modules
  - services

Modularity and modules

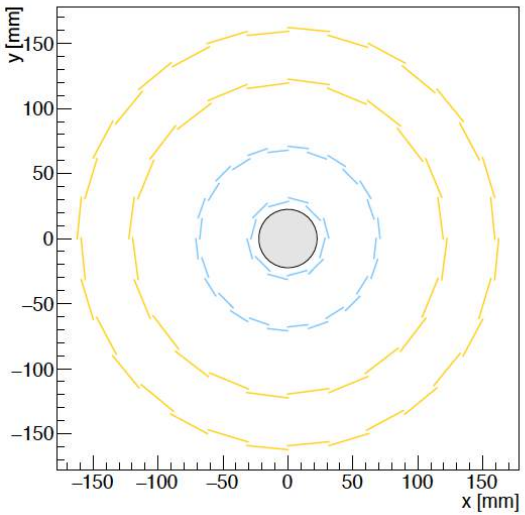
- Modularity of the readout chain

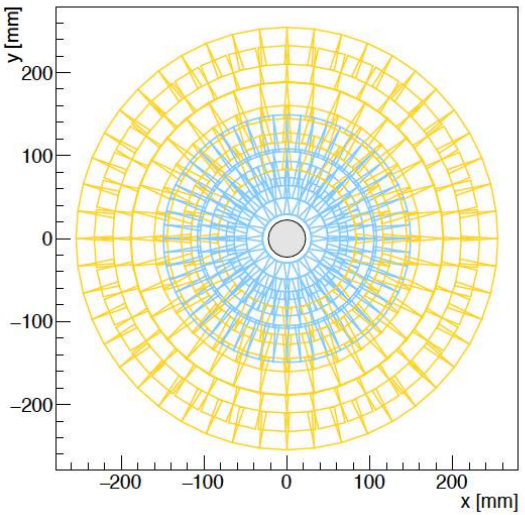


- No opto-electronic device able to survive in the radiation environment of the inner layers.

  Solution: "remote" lpGBT placed on the pixel service cylinder and connected to the module (readout and control signals) via e-link cables.

- Modularity defined by matching input specs of lpGBT (10 Gbit/s → 7 e-links at 1.28 Gbit/s) with the output rate of the module (which depends on the position and on the physical dimensions of the ROC).





- Minimal number of module types e.g. 2x1 or 2x2 ROCs per module with typical size of a ROC 2x2 cm^2.

  No wedge shaped modules.

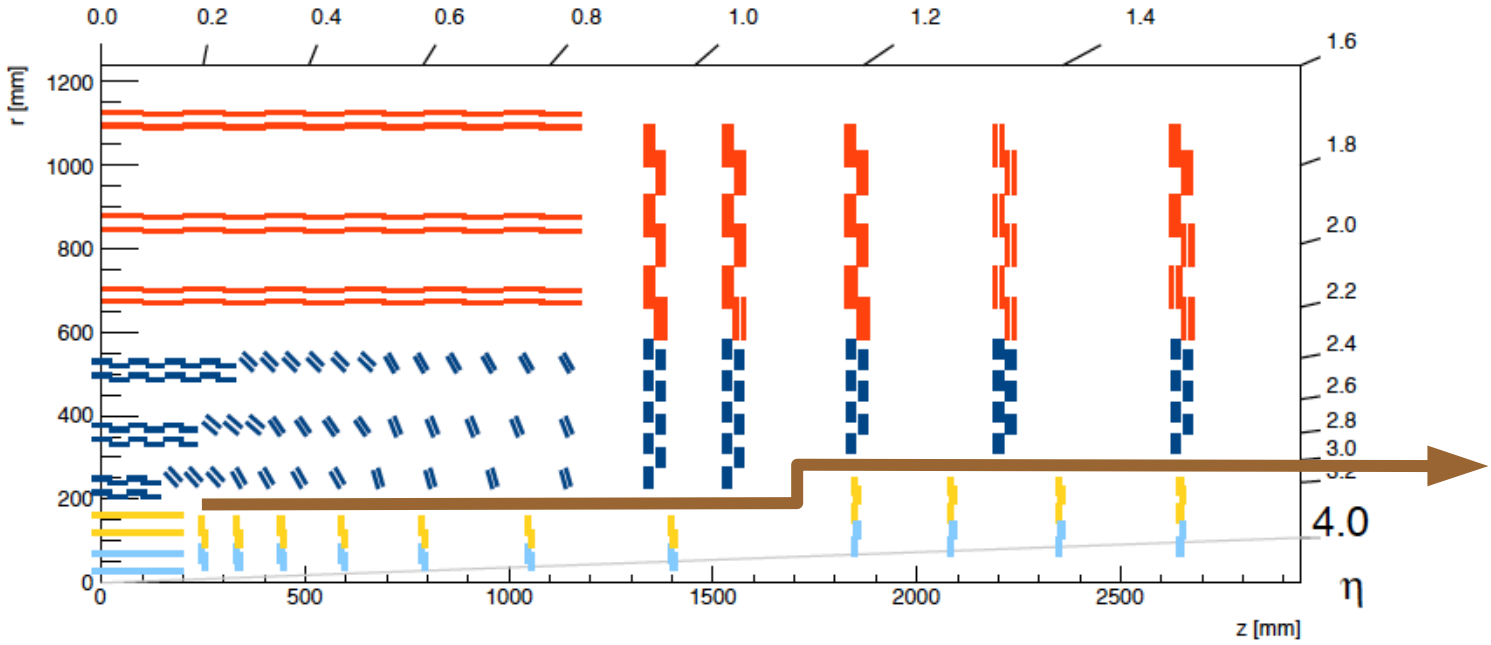
- Possibly use small/large pitch pixels in different layers/discs.

Services

- Usage of service cylinder(s) similar to phase-0/phase-1:
  - housing opto-conversion module (lpGBT+VCSEL)
  - routing signal/ctrl e-links from module to lpGBT
  - routing power cables
  - cooling pipes

service cylinder in the tracking acceptance

→ keep material as low as possible



Services developments

- **e-links**

  5500 signal cables + 2000 ctrl cables with length varying from 0.1 m to 1 m.

  Two options under investigation: Al+kapton flex and twisted pairs with different configurations of shielding and insulation.

  Total mass for reference scenario (9000 cables x 0.5 m):
  - Al+kapton flex: 0.6-1.3 kg
  - Cu twisted pair: 1.1-3.7 kg

  grounding/shielding driving the total mass → need lab measurement of cable cross-talk

- **power distribution**

  Required power for pixel ROCs (65 nm): 20 kW on 4.5 m^2.

  Powering schemes used for phase-0 (direct from PS) and for phase-1 (DC-DC converter) cannot be used → investigate across modules serial powering.

  First estimate: 1/3 power loss in the cables (0.5-0.9 kW), 1/3 material in power cables (1.0-1.8 kg)

  Start with a setup based on ATLAS FEI4 to gain experience on system test.

- **cooling**

  2-phase Co_2 system.

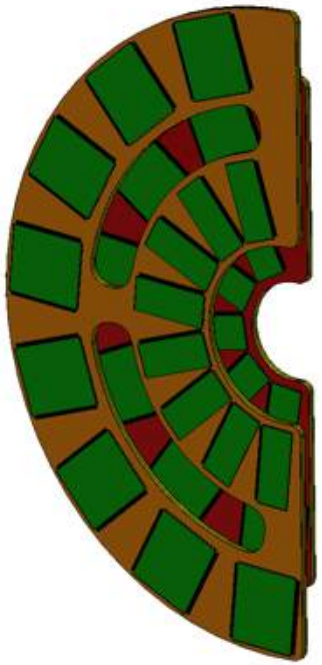
  Investigating titanium pipes (instead of stainless steel) to further reduce the material budget.

Summary

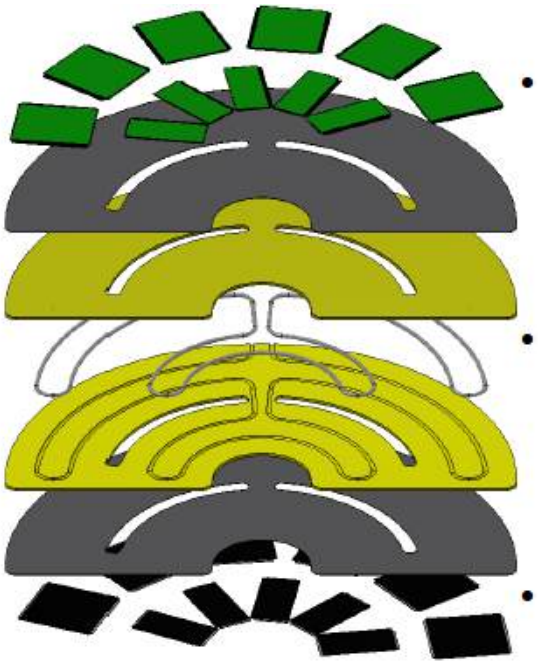
- Last year has seen a focused but considerable effort to converge toward a realistic design of the CMS Inner Pixel for the TDR.
- Key points which will be clarified by R&D activities in the next months:
  - performance of small pitch pixels before/after irradiation
  - performance of 65 nm ROC
  - performance of serial powering

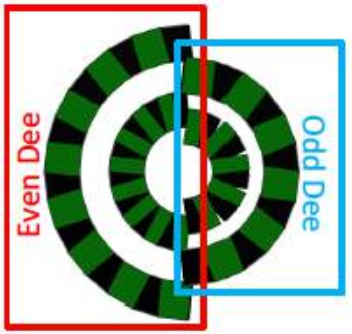
EXTRA SLIDES

Design concept of FPIX discs



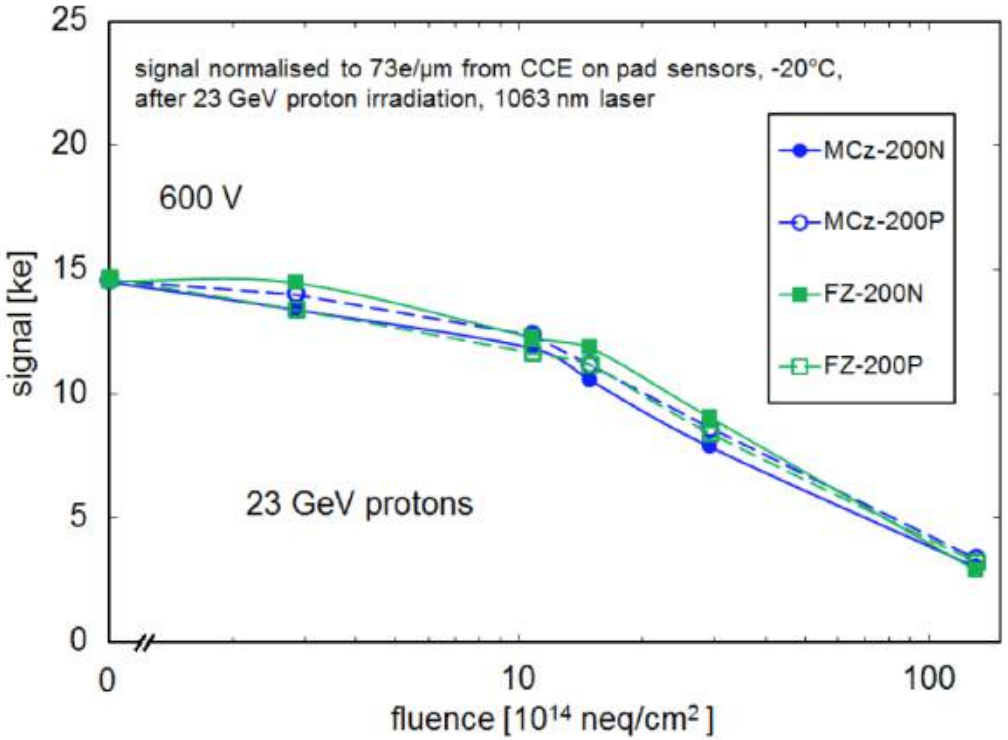
- Each FPIX disc consists of two "Dees":
  - Odd Dee: with modules of 1st and 3rd ring
  - Even Dee: with modules of 2nd and 4th ring
- Dees are CF sandwich structures with CO_2 cooling tubes embedded in thermally conducting foam.
- Dees will also host the lpGBT (at the periphery) and other electrical components.
- 1 (small discs) or 2 (large discs) cooling loop for each Dee with ~200 W/loop

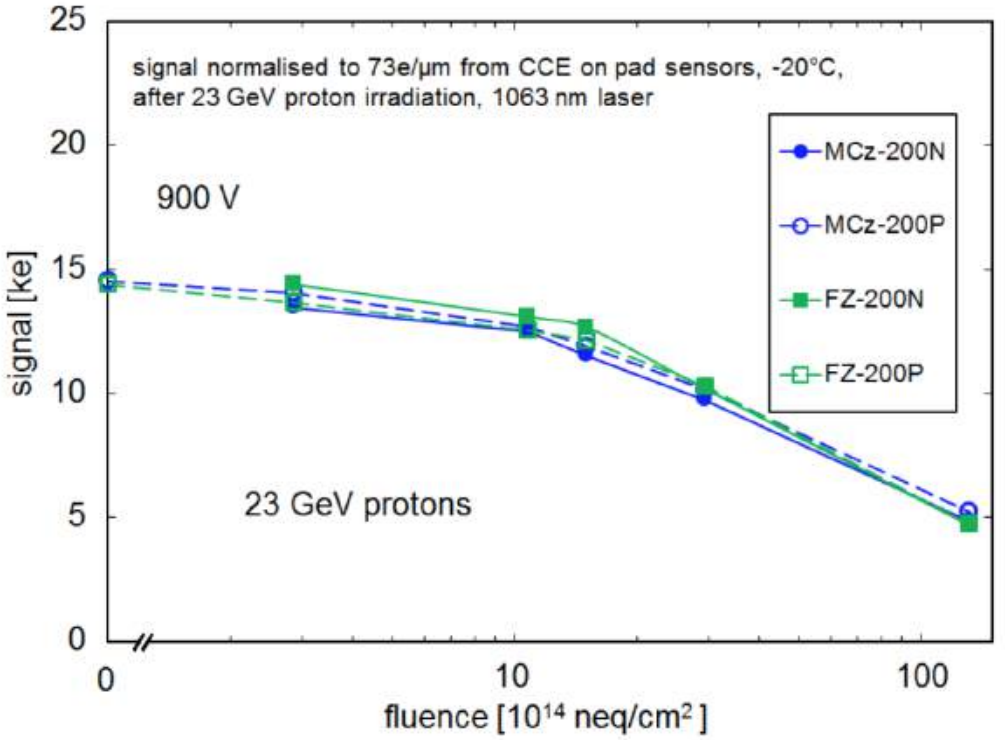




Sensor radiation hardness

- Charge collection efficiency as a function of fluence in 200 μm thick n-on-p pad diodes
  - collected signal after 1.3x10^{16} n_{eq}/cm^2: ~5000 e with V_{bias}=900 V
  - measurements to be repeated on irradiated pixel sensors from HPK and FBK submissions

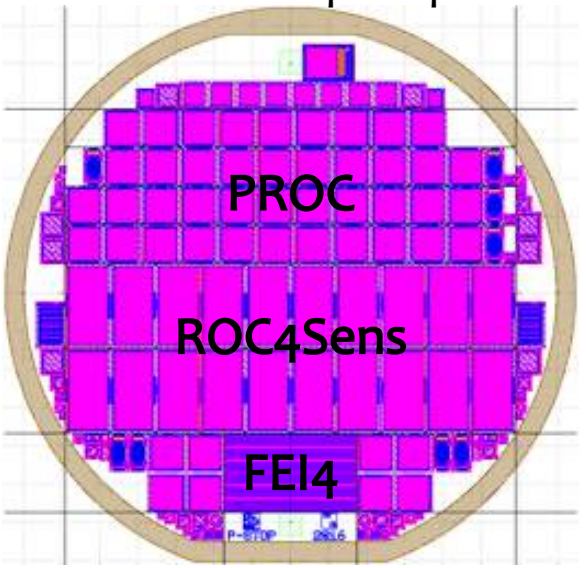




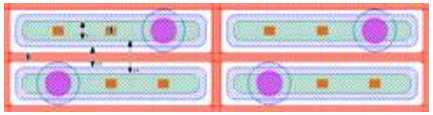
HPK submission details

- Small pitch (2500 µm²) on thin (150 µm) n-on-p wafers (6”).
- 2 isolation schemes/2 independent mask sets:
  - common p-stop
  - p-spray
- 3 aspect ratios matching the same readout pattern.

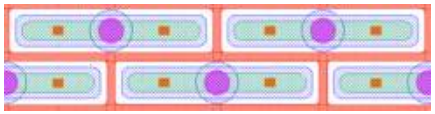
p-stop wafer



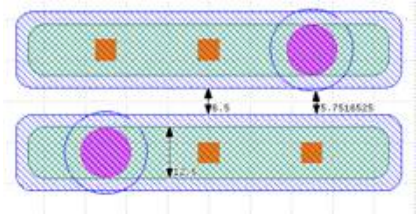
25x100 µm² (implant 9 µm)



common p-stop

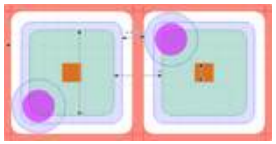


”bricked” common p-stop

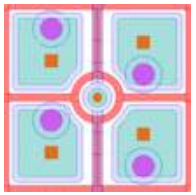


p-spray

50x50 µm² (implant 32 µm)



common p-stop



p-spray, PT bias

metal overhang 3 µm, 12 µm passivation opening for bump-bonding

FBK-INFN developments

- 2014 batch: planar pixels, n-on-p, 6" wafer, 100 μm and 130 μm thickness Direct-Wafer-Bonding (DWB) and Silicon-On-Insulator (SOI) handle wafer, standard picth 100x150 μm^2.
- several options for pixel design:
  - guard-ring (from 1 to 4), punch-through/no punch-through, p-stop/no p-stop
  - neutron irradiation up to 10^{16} n_{eq}/cm^2
- results from sensors qualification:
  - overall excellent quality
  - CV curves showing full depletion of sensor with punch through
  - sensors stand high V_{bias} after irradiation and annealing
- results from testbeam (FNAL):
  - hit efficiency > 99%
  - charge collection:
    - observed correct scaling from 100 μm to 130 μm thick sensors
    - in p-stop pixels found slightly less (~8%) than in no p-stop pixels
    - charge profile along pixel sides uniform when the neighbour pixel is included

3D sensors developments

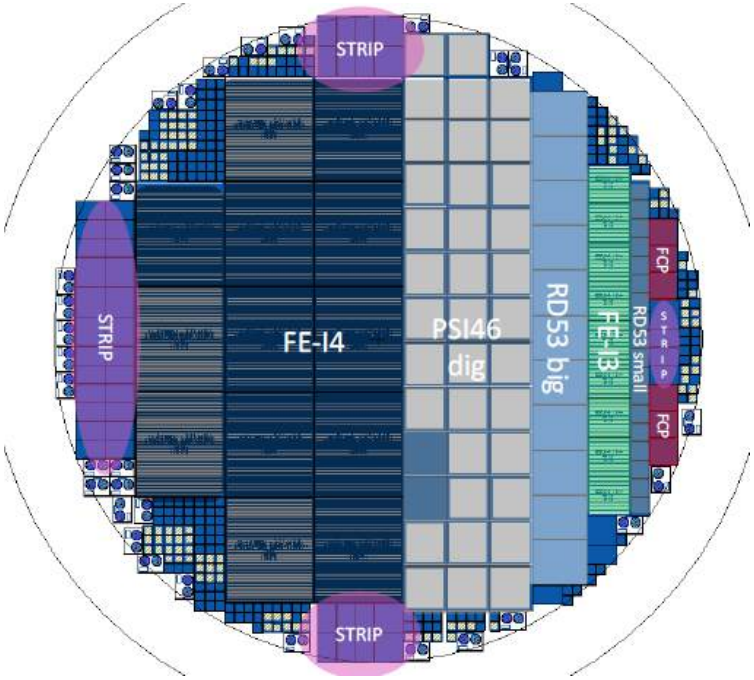
- Two submissions of small pitch pixels:

– CNM/RD50 (with ATLAS and LHCb)

- small pitch: 50x50 µm² (ROC4Sens) and 30x100 µm² (FCP130)
- double side columns
- 230 µm thickness n-on-p
- small aspect ratio (8 µm columns e.g. 1:25)
- production completed in December 2015, preparing for bump bonding (FE-I4)

– FBK/INFN

- small pitch: 50x50 µm² and 25x100 µm²
- single side columns
- 100 µm and 130 µm thickness (on 500 µm handle wafer)
- production completed in March 2016, preparing for bump bonding (FE-I4 and PSI46dig)



ReadOut Chip (ROC)

- Requirements:
  - high hit rate (up to 3 GHz/cm^2)
  - demanding readout (750 kHz L1A trigger rate) and buffering (12.5 µs latency)
  - small pitch pixels (2500 µm^2) and large chips (2x2 cm^2) → 1 billion transistors
  - harsh radiation environment (10 MGy, 2x10^{16} n_{eq}/cm^2)
- Baseline technology: 65 nm developed by RD53 collaboration:
  - radiation damage (already after 10^{15} n_{eq}/cm^2) affecting transconductance and V_{thr}
  - effects largely depending on temperature and geometry of the transistors
    - ROC should be kept cold (-20 °C when switched off, <20 °C when switched on)
    - analog: small degradation if large transistors are used
    - digital: mainly affecting speed. Most of the digital components operates "only" at 40MHz; design faster circuits with larger transistors (ad-hoc library required)
  - Full scale RD53 ROC demonstrator (400x200 pixels) expected in 2017 to check if 10 MGy may be accomplished.
  - Option to replace the inner layers after 5 MGy.