8th International Workshop on Semiconductor Pixel Detectors for Particles and Imaging.



ID contributo: 81

Tipo: invited talk

Physics benchmarks with the VELO pixel

The upgrade of the LHCb experiment, planned to start data taking in LHC Run 3 in 2021, will transform the experiment to a trigger-less system reading out the full detector at 40 MHz event rate. The electronics of all systems will be changed and the tracking detectors completely replaced. For the Vertex detector this will see a move from the currently installed strip detectors to a fully pixel based system.

At the upgrade all data reduction algorithms will be executed in a high-level software farm with access to the complete event information. The pixel detector will play a central role in the event selection, with fast and efficient tracking algorithms being central to the ability of the computing farm to process full events at 30 MHz rate. Online alignment and calibration procedures will be mandatory as well as event reduction to optimise the bandwidth to storage. In addition, the resolution and tracking performance offered by the pixel detector is required to be at least as good - at higher occupancies and rates - than the current strip detector, in order to maintain the excellent performance of the LHCb detector in the areas of heavy flavour physics.

The pixel detector has been studied in detail and the enhancement in tracking and pattern recognition performance has been quantified. The impact of the material budget and the pixel resolution has been assessed, and performance parameters of the ASIC such as pile up and spillover have been related to the expected physics performance. The way in which the pixel detector enhances the speed and efficiency of the detector, as well as the physics performance, will be presented.

LHCb is also looking beyond the current upgrade, and considering in particular what the new technological possibilities for hybrid pixel detectors can contribute towards enabling LHCb to run at even higher luminosity. This includes concepts such as a move to 65 nm CMOS technology, improving the time stamping in pixels to improve pattern recognition and distinguish pile up vertices at high luminosity running, or the use of TSVs to improve the material budget, detector packaging and high speed signal routing. The possible impact of such applications on the future LHCb physics programme will be discussed.

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