8th International Workshop on Semiconductor Pixel Detectors for Particles and Imaging.

Contribution ID: **83** Type: **contributed paper**

4D fast tracking for experiments at HL-LHC

Several efforts have been recently devoted to develop high-resolution timing detectors for tracking at the High Luminosity LHC experiments while track triggers, implemented with dedicated hardware, have been used at hadron colliders to select heavy-flavour decays. In this R&D project we propose to combine the two methods to develop an innovative detector, based on accurate time and position particle hit measurements, for 4D tracking and fast track trigger. The precise measurement of the hits'time is the key feature to operate an effective pattern recognition that guarantees a high tracking efficiency while enhancing the ghost track rejection, and to perform selective track triggering. We ultimately aim to exploit this detector in flavour physics experiments, in conditions of a high event pile-up, where sensors and front-end electronics are required to provide a hit time resolution of the order of 20 ps and a hit position resolution better than 40 μm, and are able to continuously operate in a harsh radiation environment (up to a total flux of 10E17 1-MeV neutrons equivalent per cm^2).

Summary

State of the art tracking pixel detectors with precise time-tagging show a time resolution of about 200 ps [1], and we aim to reduce this by one order of magnitude. Crucial aspects to achieve this ultimate time resolution are the optimization of pixel sensor geometries (in both 3D and planar technologies) to achieve the most uniform electric field, and the design of fast and low noise dedicated front-end ASIC. This front-end will incorporate a fast current amplifier followed by a discriminator and a time-to-digital converter, and will be developed in 65 nm CMOS technology with fault tolerant architecture which matches the radiation hardness requirements.

Feasibility studies of a 4D fast track finding system, using hits'space and time information, has been recently presented [2] as a possible solution for the low level track trigger of the HL-LHC experiments. The system is based on a massively parallel algorithm implemented in commercial FPGAs using a pipelined architecture and allows a precise real-time determination of the track parameters (including time) while maintaining a low fraction of reconstructed fake tracks.

The proposed detector will allow to perform flavour physics at LHC while operating at instantaneous luminosities more than one order of magnitude larger than the current ones, while guaranteeing large tracking efficiencies and a negligible ghost tracks rate.

Primary authors: CARDINI, Alessandro (CA); LUPPI, Eleonora (FE); FIORINI, Massimiliano (FE); Dr NERI, Nicola (MI); CALABRESE, Roberto (FE); Dr MARCONI, Umberto (BO)

Presenter: Dr NERI, Nicola (MI)