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Tracking and flavour-tagging performance for HV-CMOS sensors in the context of the ATLAS ITK pixel simulation program

The HV-CMOS pixel technology has recently risen interest in the ATLAS community in view of its possible usage for the ATLAS pixel detector upgrade towards the High Luminosity LHC phase. HV-CMOS sensors can be employed in the pixel outer layers given the reduced radiation hardness at high radius and their cheap technology. However, the largest impact on physics performance, vertexing, tracking and flavour tagging, could be achieved if exploited in the innermost layers due to their very fine granularity and small depletion depth that can result in improved tracking resolution and better characterisation of the cluster size for tracks in the large pseudorapidity region.

Summary

An overview of the studies on the tracking performance resulting from the usage of HV-CMOS sensors in the Innermost Pixel Layer will be presented. Full simulations based on Geant4 and ATLAS reconstruction are used to assess the typical gain of the various detector designs. Different pixel granularities and depletion depths are explored and the typical resolution of the tracking residuals and impact parameters is compared to the present pixel technology in the Innermost Pixel Layer (IBL). In addition, the expected impact of this technology is also verified on tt events in order to disentangle pure resolution effects from pattern recognition issues, with a particular emphasis on b-tagging performance gauged by the improvement of the light-flavour and c-jet rejection for a given b-jet efficiency. A detailed study on the specific pixel clustering algorithm to be used in the simulation will be discussed as well.

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