Thin n-in-p planar pixel modules for the ATLAS upgrade at HL-LHC

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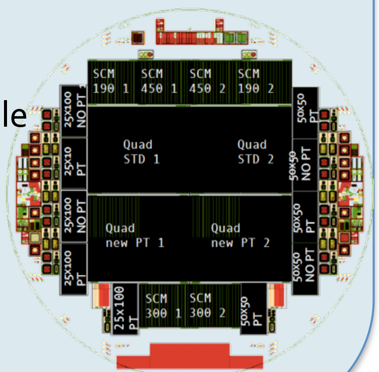
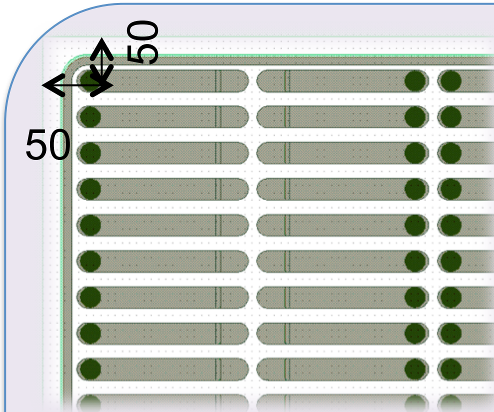
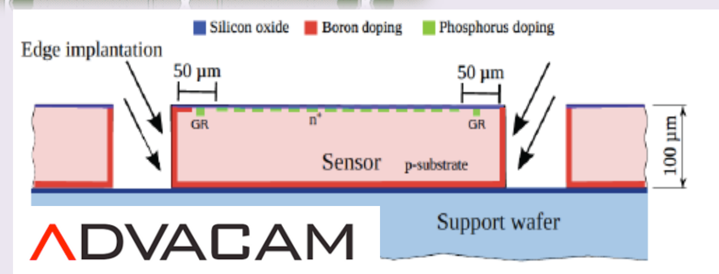
Technologies for thin planar pixel sensor productions

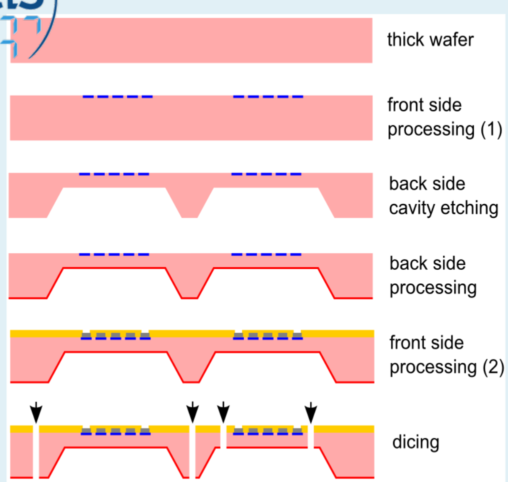
- SOI technology as a reliable method to obtain thin sensors
- Ongoing productions with RD53A compatible sensors and sensors for quad prototyping

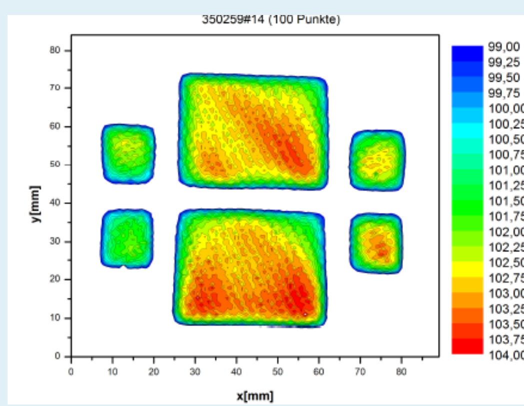




- SOI wafers with active edge processing:
  - Trench etching
  - Inclined ion beam implantation on the side





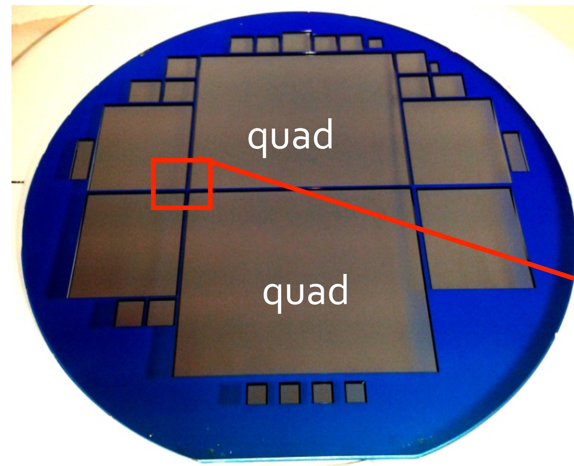


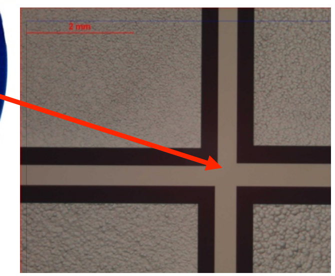
- Backside cavities etching → no need of handle wafer

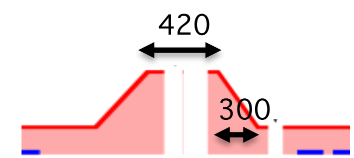
- Results of thin planar sensors will be shown before and after medium and high irradiation fluences

Thin planar pixel sensors with backside cavities

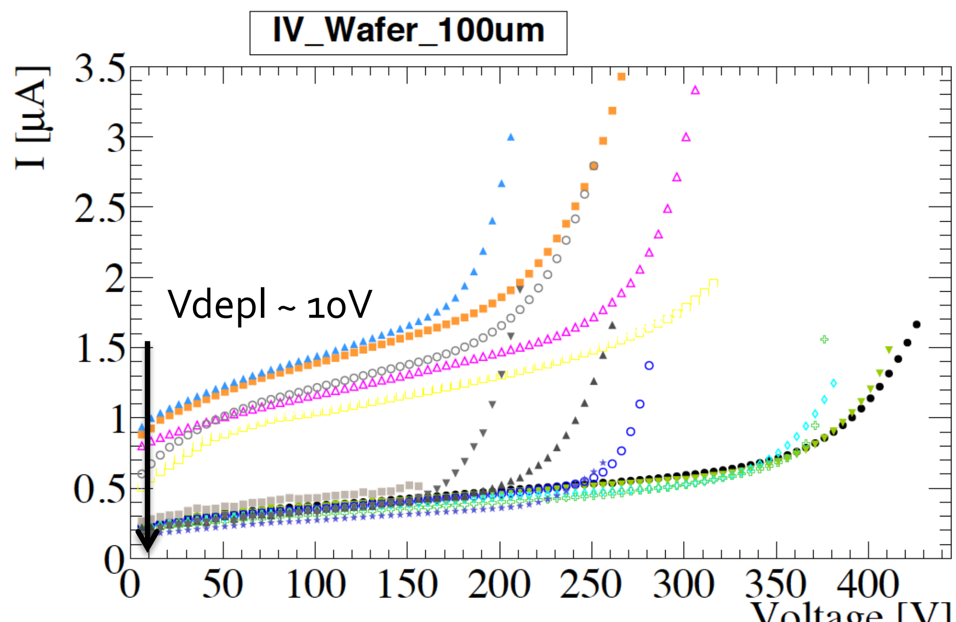
- Starting thickness 525µm,
- Target thicknesses 150/100µm
- Anisotropic etching by KOH
- Two sets of dicing lines:
  - On the 420 µm wide frame between the structures
  - Dicing along the sensor perimeter on the thinned substrate



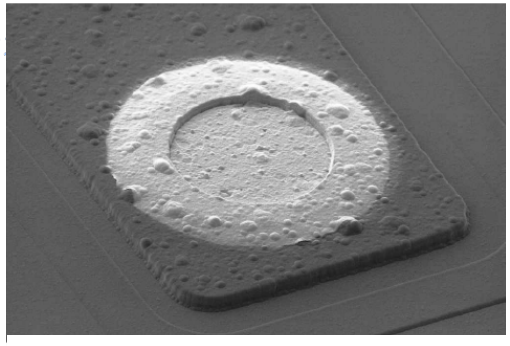




- Two batches:
  - 8 wafers with 150µm membrane
  - 7 wafers with 100µm membrane
- Depletion voltages as expected
  - ~15V for 150µm membrane
  - ~10V for 100µm membrane
- Very good electrical yield in the order of 70…95% for pixel sensors



UBM processing at CIS



Nickel UBM

Mask-based electroless Ni-UBM

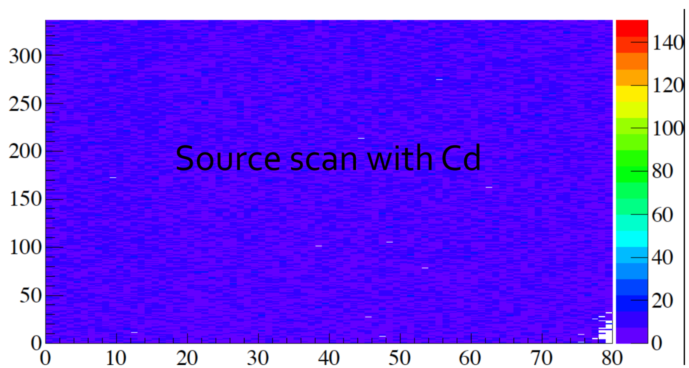
- applied for CMS-Pixel production, in combination with In-bumps
- relatively thin film on sensor surface
- already tested with (IZM) solder bumps

Mask-based electroless Pt-UBM

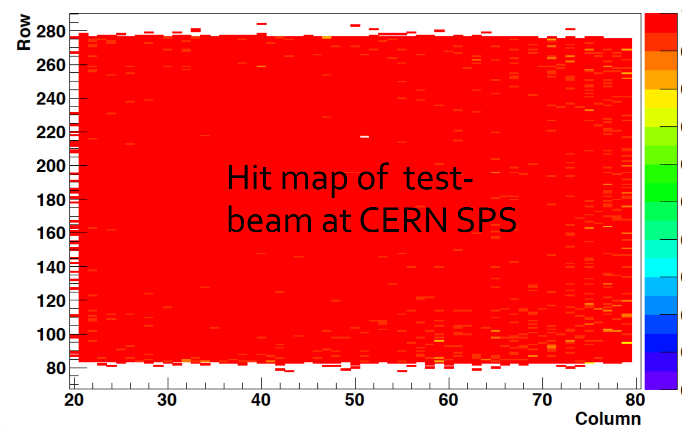
- First experience at CIS
- Some deposition steps are outsourced

- Single chip and quad sensors with Ni and Pt UBM have been flip-chipped at IZM

Ni UBM and 150 um thickness: only a few disconnected corners, stability after thermal cycling (20 to -50°C)



100 µm thin sensor with Pt UBM



See poster of T. Wittig (CIS)

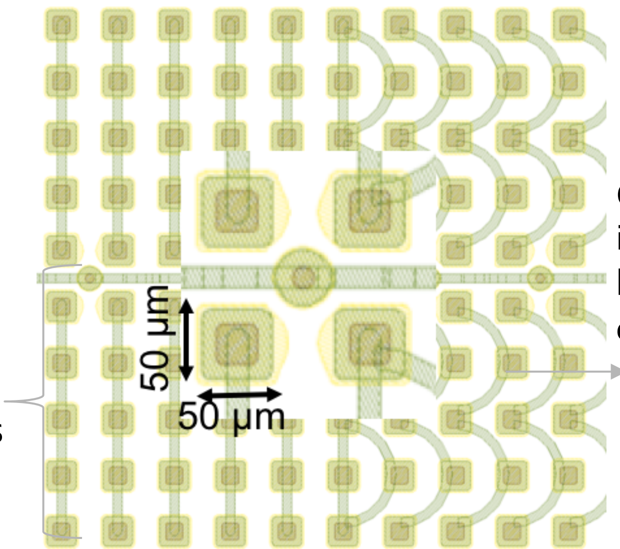
" Large Area Thinned Planar Sensors for Future High-Luminosity-LHC Upgrades "

Investigation of charge sharing effects on 50x50 μm² pixels

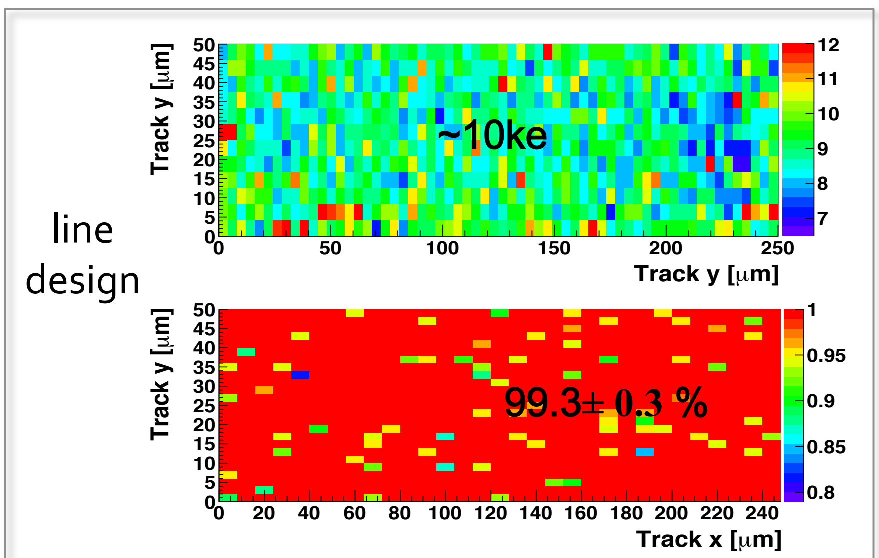
- Investigate the effect of charge sharing with 50x50 μm² pixels by using FE-I4 compatible sensors
  - no significant charge sharing effects between neighbouring pixels with 150 μm thick sensors
  - plan to repeat measurements after irradiation when charge sharing can induce charge loss

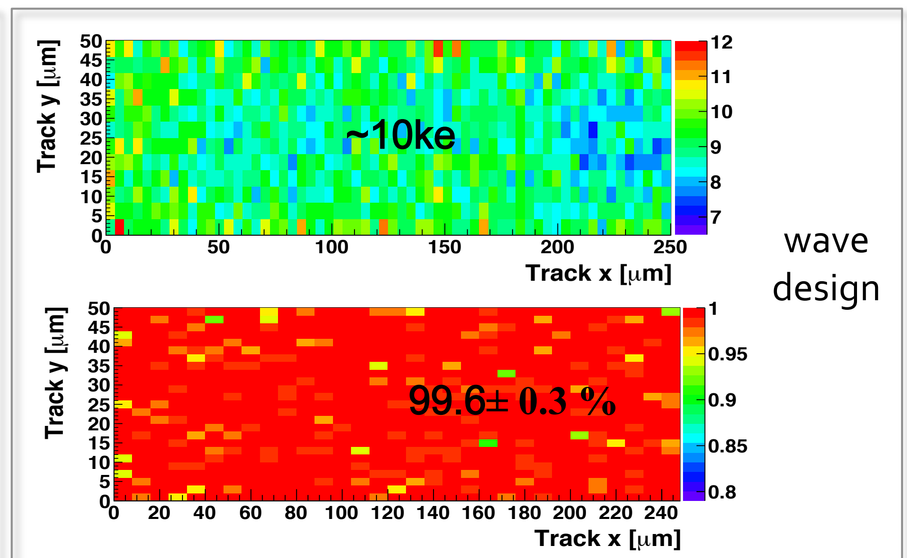
Sensor with modified implants in the CIS production with backside cavities

250 μm= five 50 μm long pixels connected by Al line



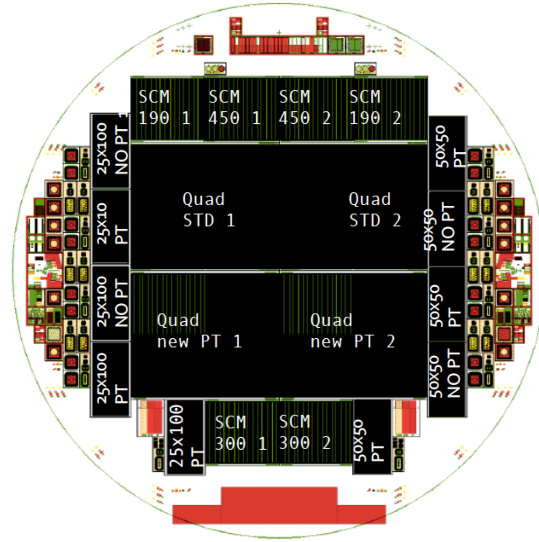
Only every other implant is read-out by same FE-I4 channel.

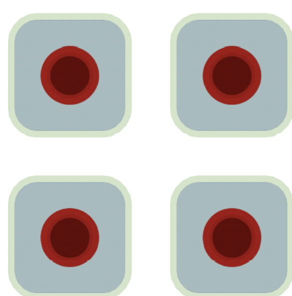




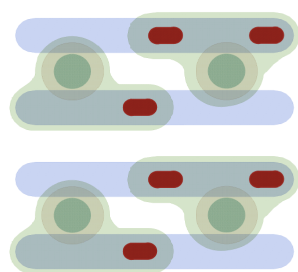
RD53A sensors in new SOI production at MPG-HLL

- High resistivity SOI 6" wafers
  - 6 wafers 100 µm thick
  - 4 wafers 150 µm thick
- Wafers at IZM for
  - BCB and UBM processing
  - complete etching of the handle wafer

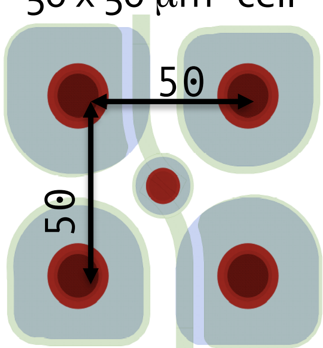


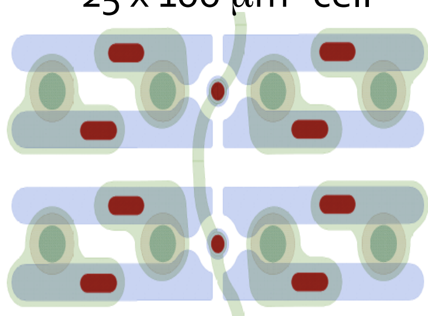


50 x 50 µm² cell

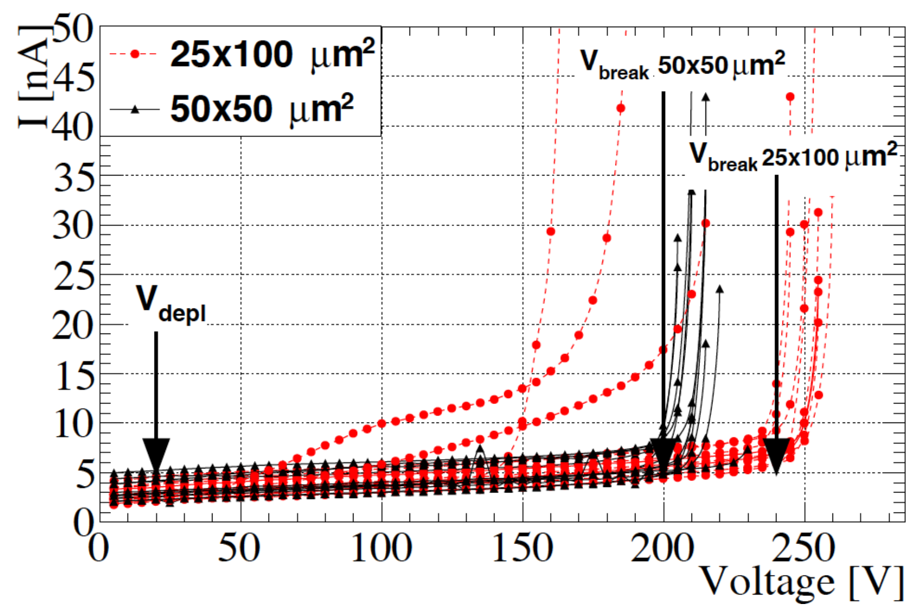


25 x 100 µm² cell

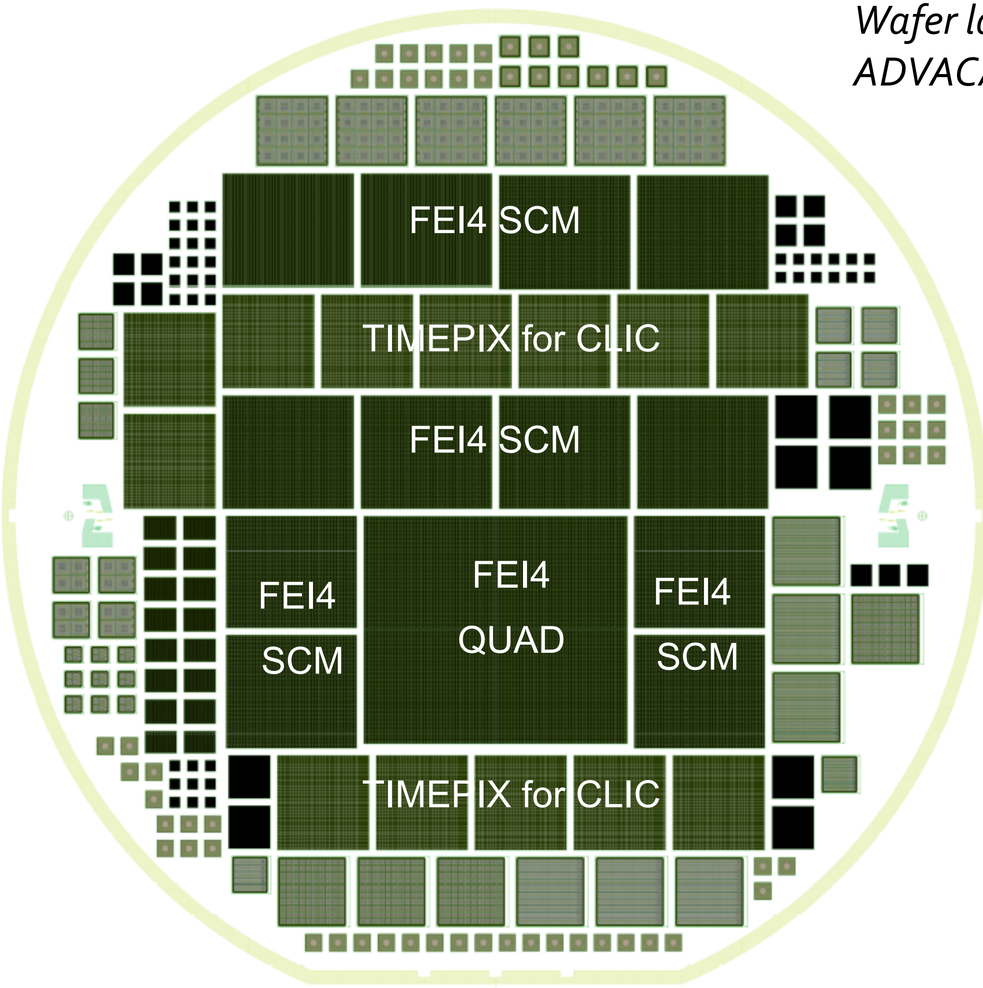




IV curves of RD53 compatible sensors



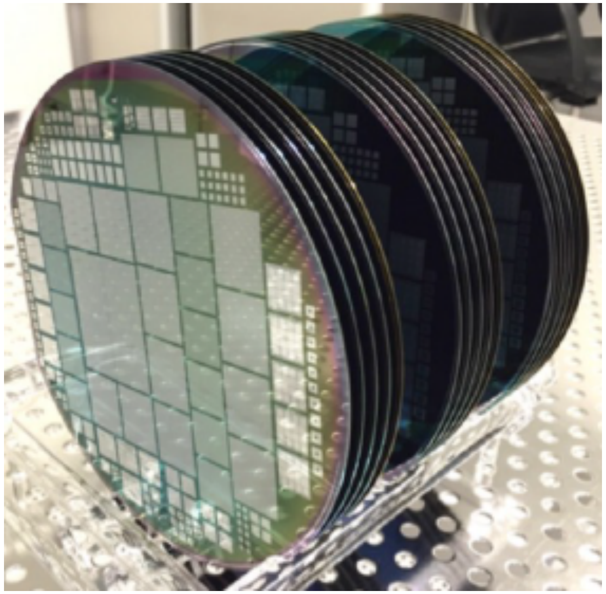
Second production of active edge pixels at ADVACAM



Wafer layout of the new production at ADVACAM (spin-off VTT)

- In collaboration with Glasgow, Göttingen, LAL, CLIC CERN-LCD,
- Geneva University for medical applications

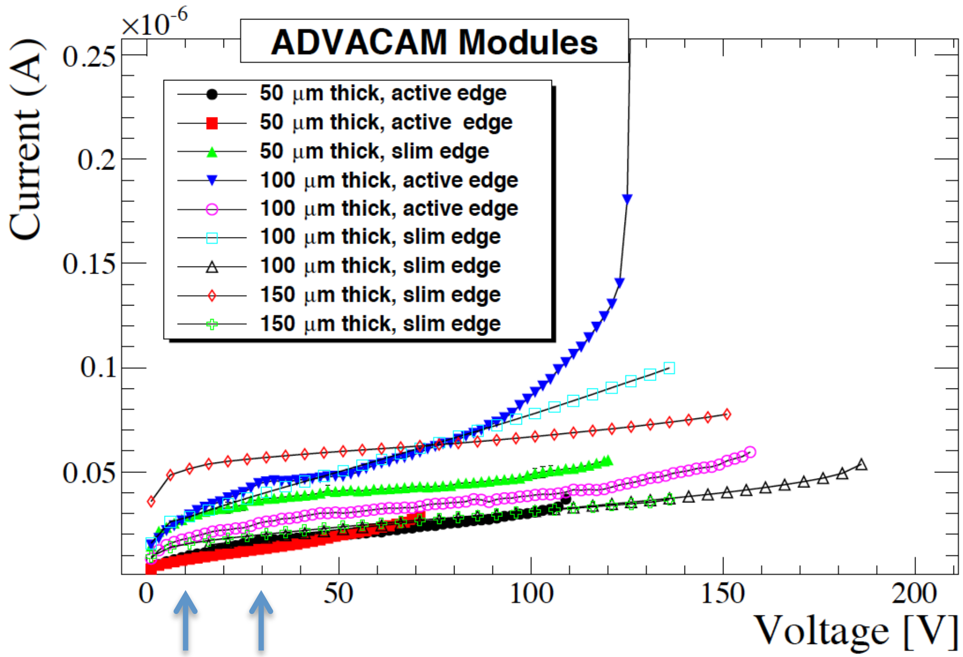
50, 100, 150 μm sensor thickness: 5 FZ p-type wafers for each thickness



Active edge process for all the structures

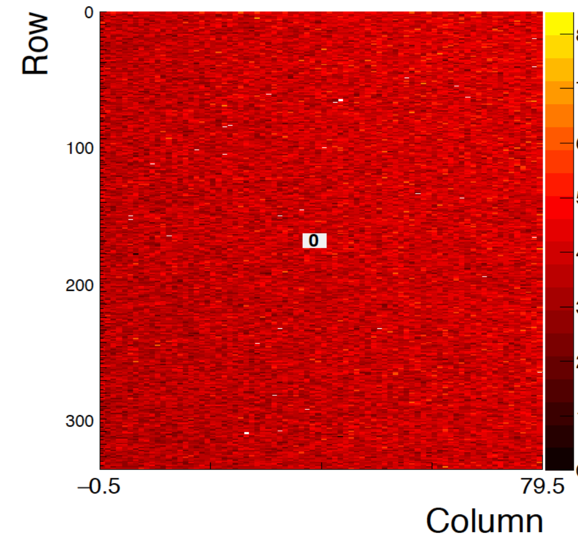
ADVACAM: a first look at 50 μm thick sensors

- Modules with 50 μm thin sensors and Cu-Au UBM show a perfect interconnection efficiency

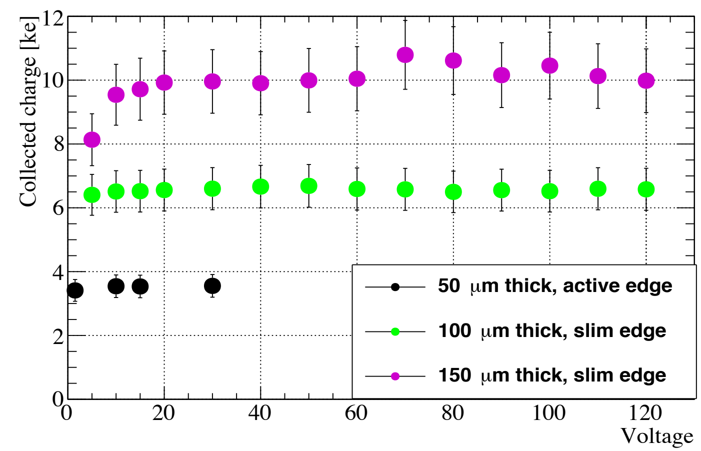


Range of depletion voltage for (50-150) μm thick sensors

Occupancy map from Cd scan of a module with a 50 μm sensor

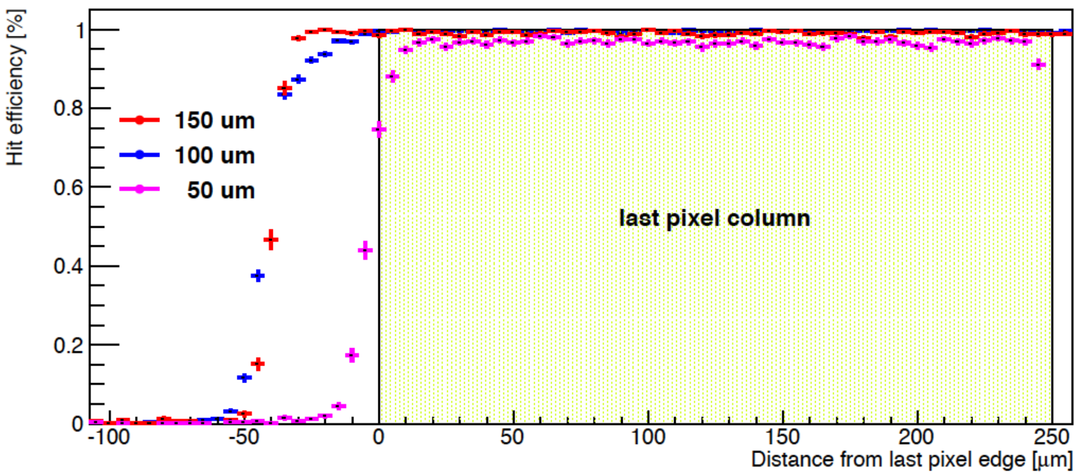


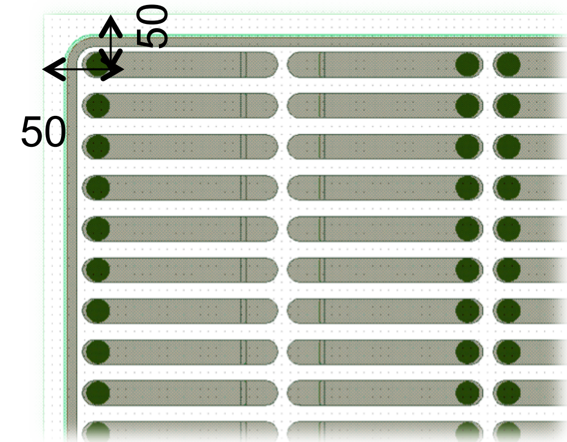
- Collected charge by ^{90}Sr scans agrees with expectations for the three thickness
- 50 μm thin sensors needs a special tuning to very low thresholds ≤ 1000 e



Test beam results of active / slim edge modules

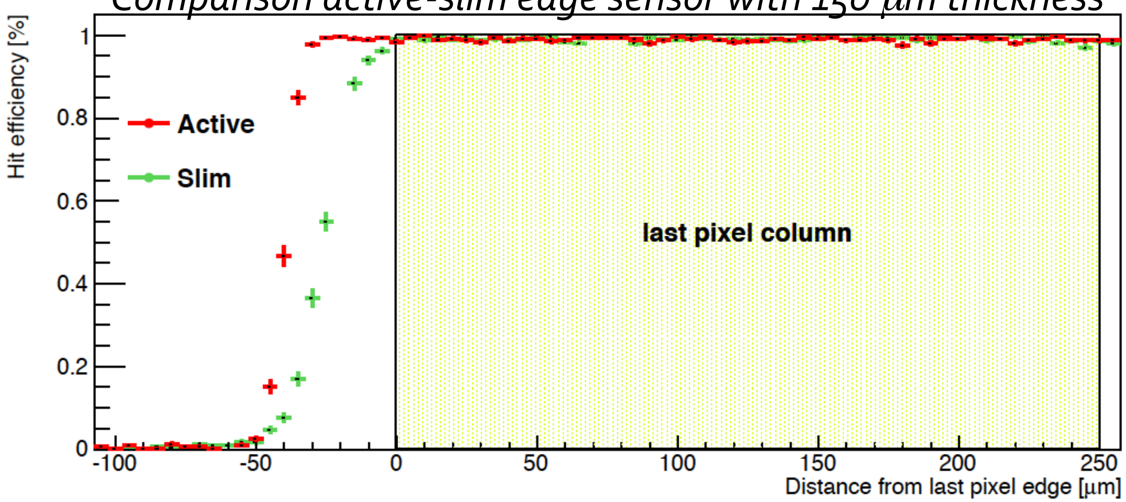
- August test-beam at CERN: systematic comparison of different sensor thicknesses

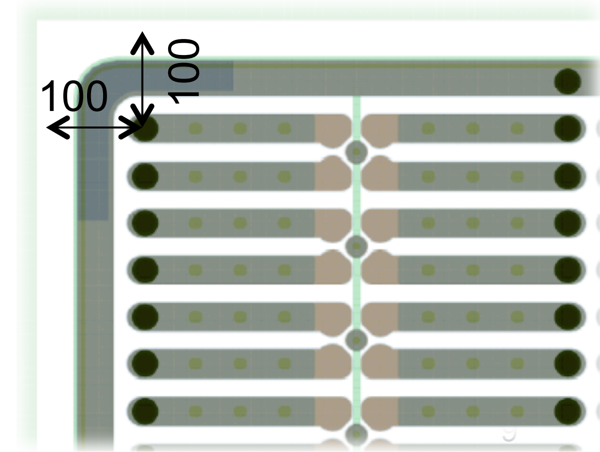




- Very good performance up to the edge of 100-150 µm thick sensors
- Lower efficiency (~97%) of 50 µm sensors even with a tuning to 800 e threshold

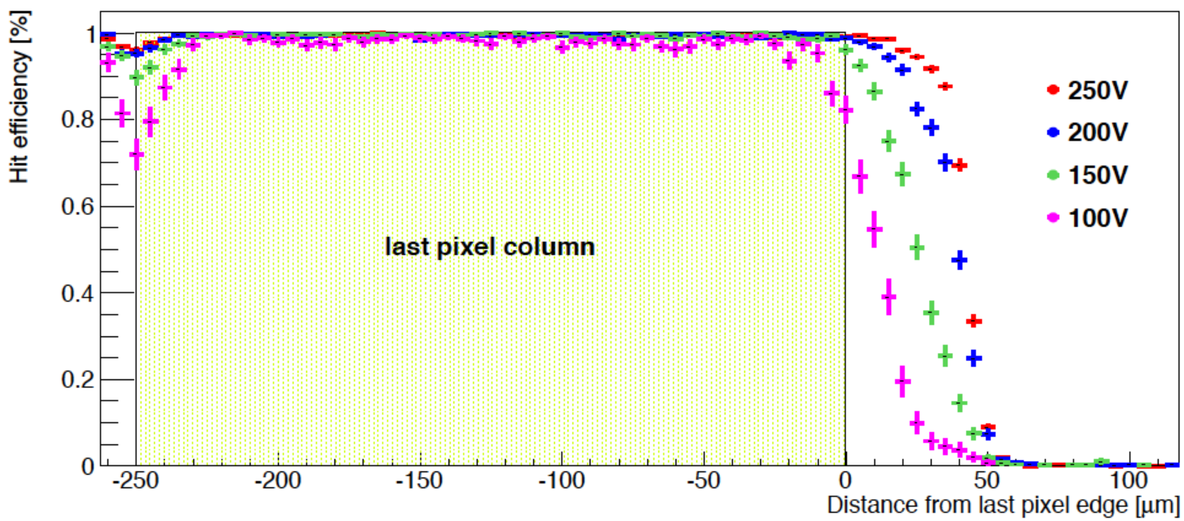
Comparison active-slim edge sensor with 150 µm thickness



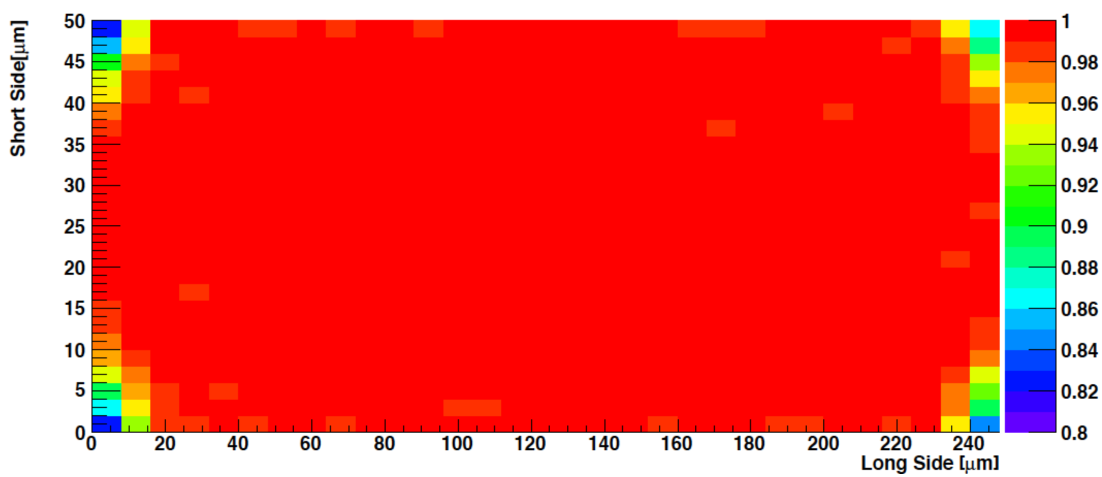


Slim edge module after irradiation

- 150 μm thick sensor, slim edge (BR), Fluence = 10^{15} n_{eq} cm^{-2}



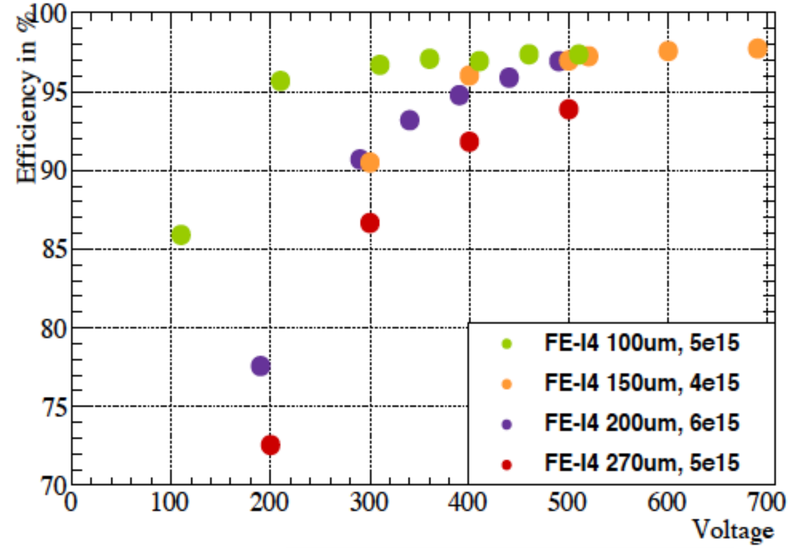
- At 250V very good edge efficiency and small eff. loss due to charge sharing



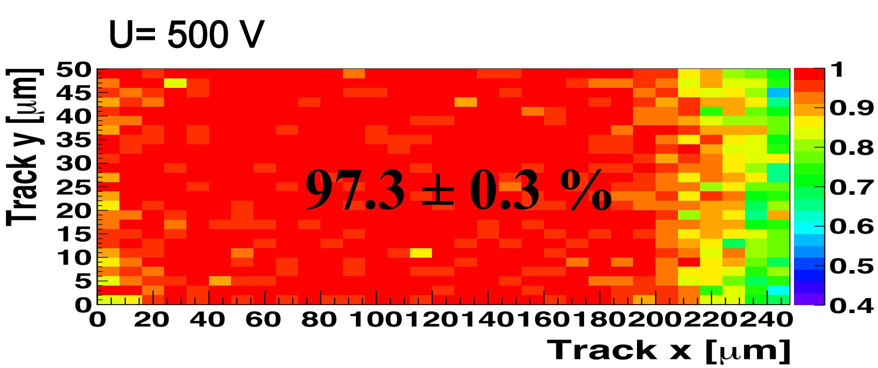
Thinner active/slim edge sensors are being or will be irradiated after parylene coating for spark prevention

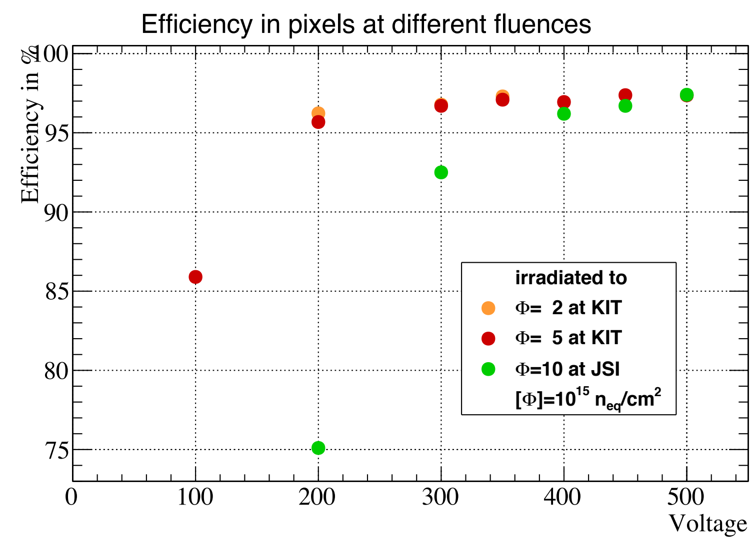
Thin sensors performance at high fluences

- 100 μm thin sensors yield the best hit eff. at 5×10^{15} n_{eq}/cm^2
- VTT FE-I4 module with 100 μm thin sensor irradiated at JSI at 1×10^{16} n_{eq}/cm^2
- Tested at DESY with 5 GeV electrons, threshold tuning to 1300 e

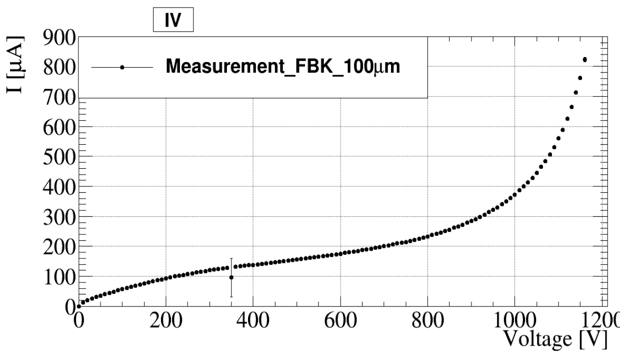


- significantly lower efficiencies at 200 and 300 V at $\Phi=1\times10^{16}$ n_{eq}/cm^2
- efficiencies at different fluences have similar saturation values (~97%)

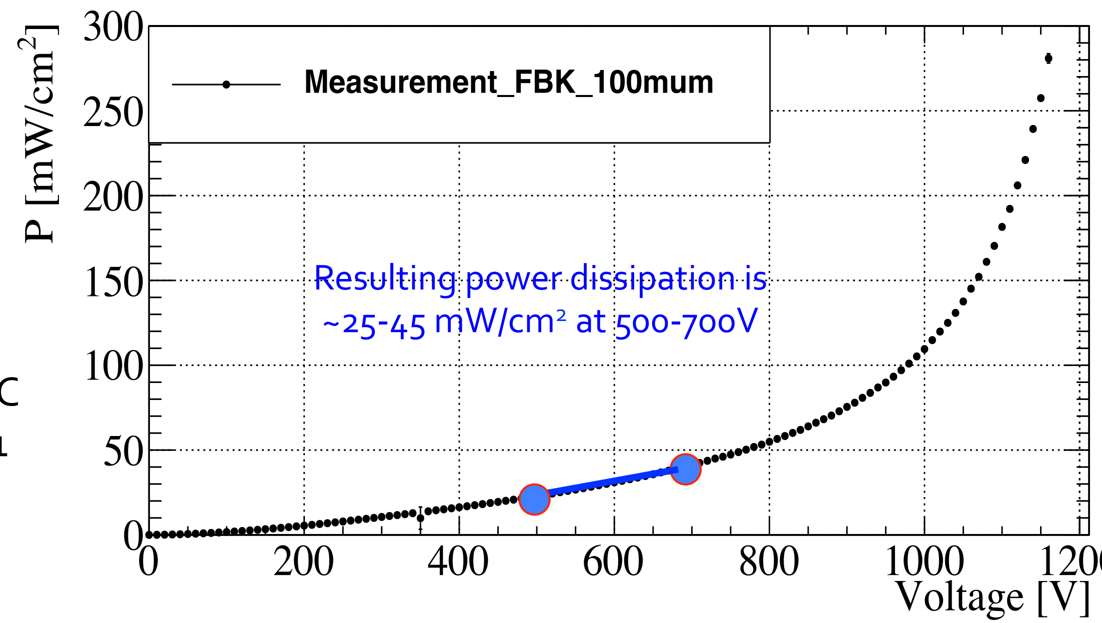




Power dissipation for thin planar sensors at high fluences



IV curve of bare FE-I4 sensor at -25˚C irradiated to **1×10^{16} n_{eq}/cm^2** after 11 days of annealing, as measured in direct thermal contact in a probe-station



Estimated power dissipation per cm² at -25˚C for a 100 µm thin sensor irradiated to **1×10^{16} n_{eq}/cm^2**

- The possible range of operation bias voltage for a pixel module with a 100 µm thick sensor is **500-700 V**
- The resulting power dissipation at 500-700 V is **~25-50 mW/cm²** at 1×10^{16} n_{eq}/cm^2 irradiation

Conclusions and Outlook

- Different production and interconnection technologies for thin planar pixel sensors investigated in a thickness range (50-150) μm.

- Good hit efficiencies up to the physical perimeter of the devices obtained with (100-150) μm thin active edge sensors

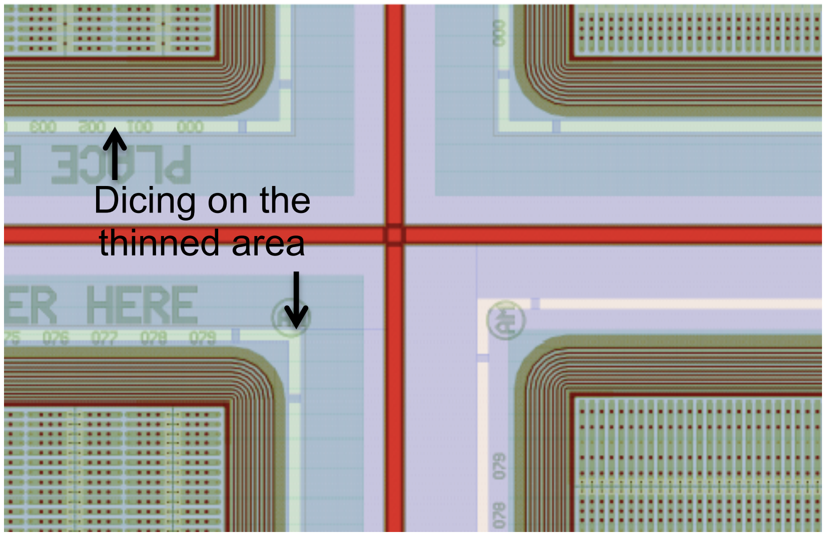
- Modules with 50 μm thin sensors show perfect interconnection yield and electrical characteristics. They are at the limit when interconnected to the FE-I4 read-out chip for what concerns collected charge and hit efficiency

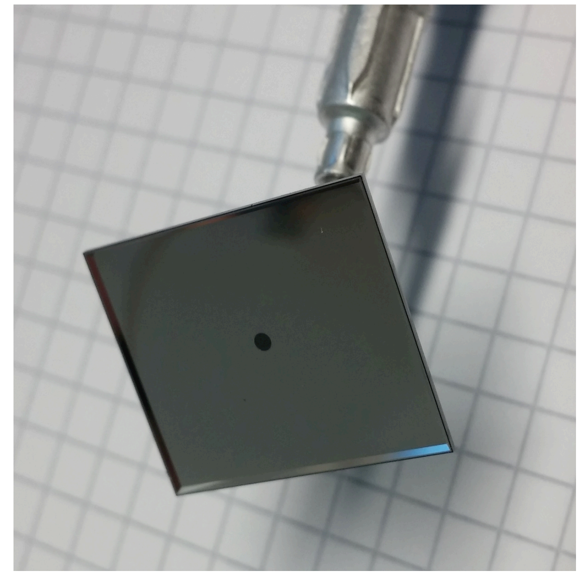
- FE-I4 modules with 100 μm thin sensors found to deliver 97% hit efficiency at a fluence of at $\Phi=1\times10^{16}\ n_{eq}/cm^2$ for a moderate bias voltage of 500V. It is so possible to estimate a lower power dissipation with respect to previous predictions obtained on the base of thicker sensors

- RD53A compatible sensors with SOI technology already produced with / without biasing structures and at the moment are being post-processed at IZM

Additional slides

Thick frame on the sensor perimeter

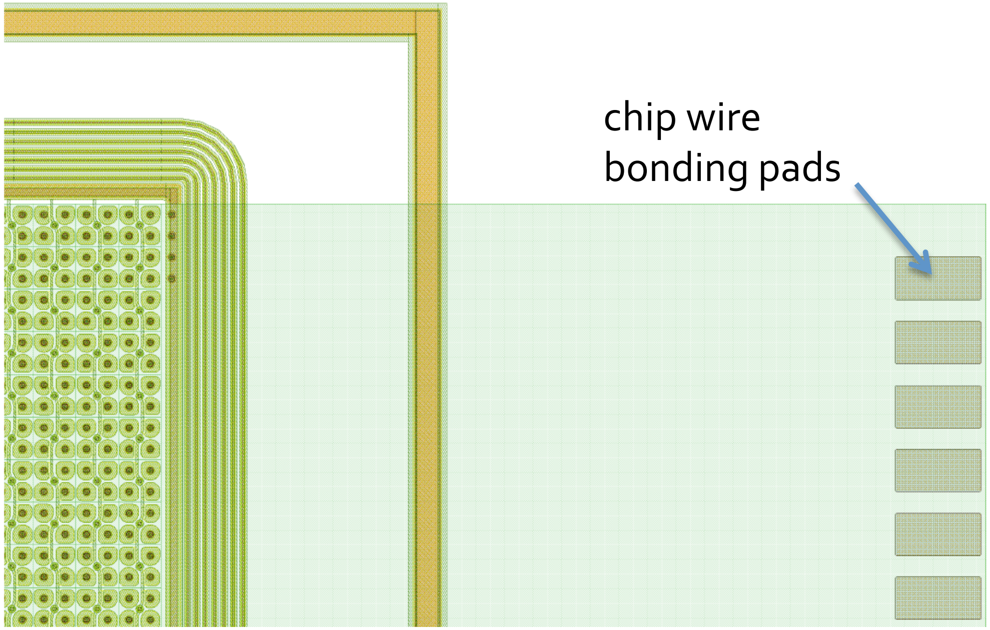


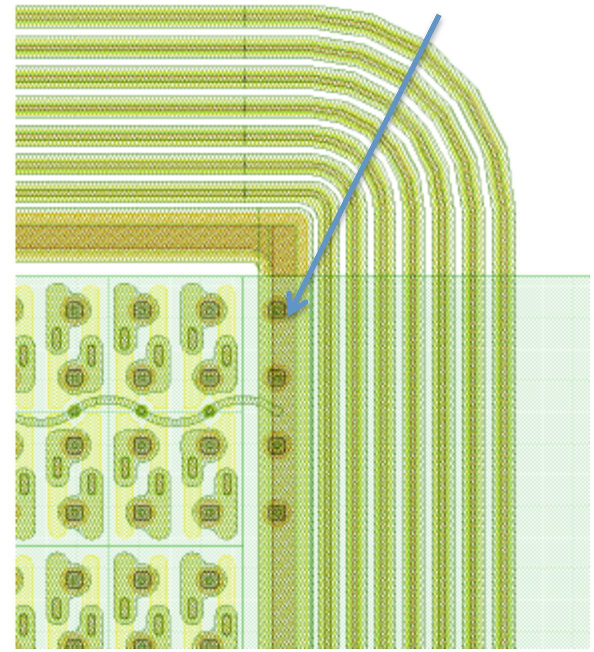


Only one module in the wafer has implemented dicing lines such that it is singularized with the thicker frame around

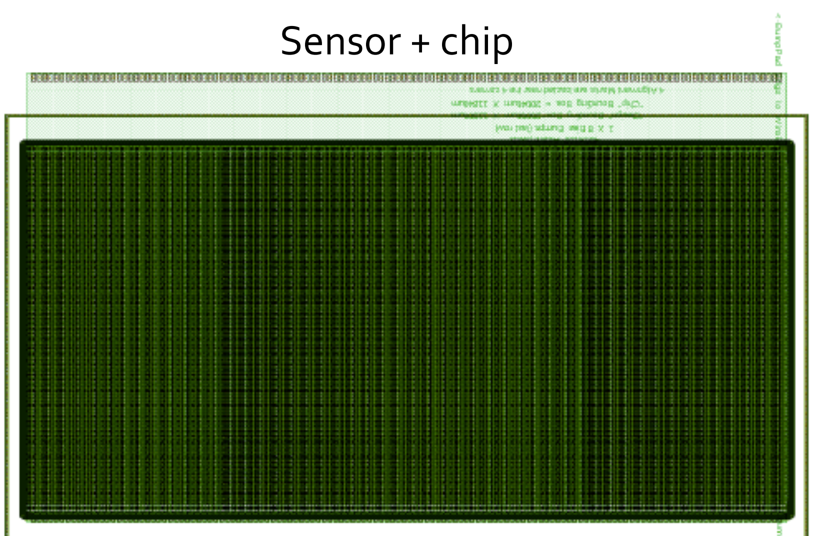
... but probably the aplanarity on the sensor backside poses problems at the system level (flex glueing, etc).

SOI3 production: RD53 sensor design



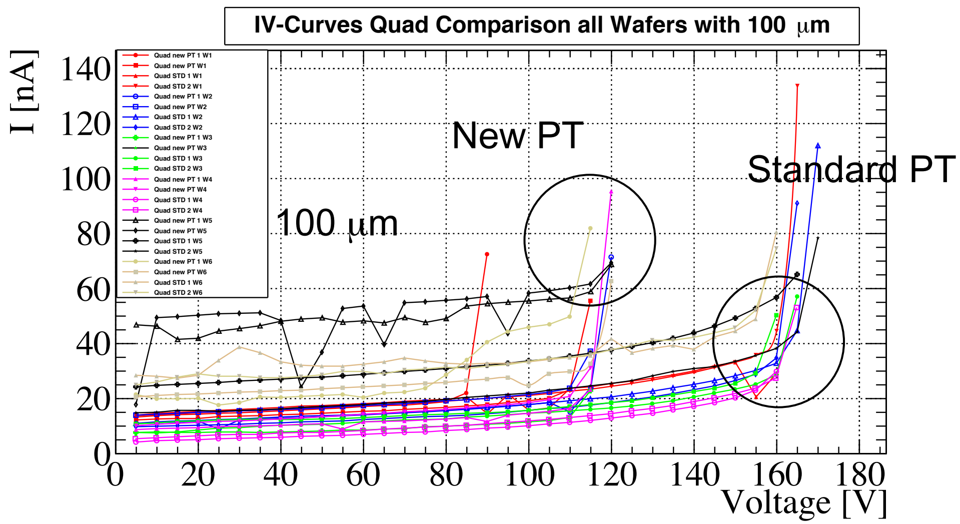


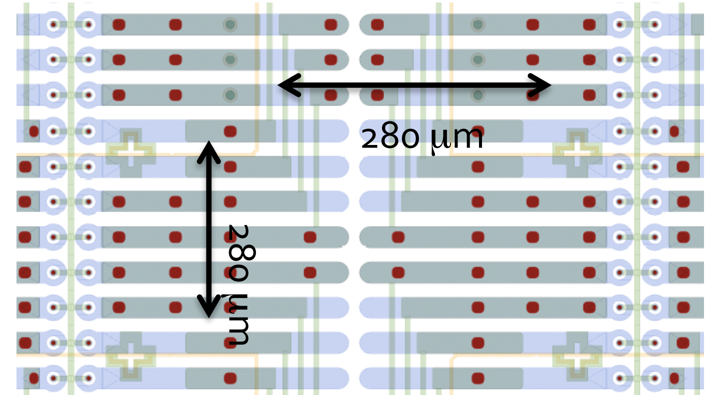
Sensor + chip



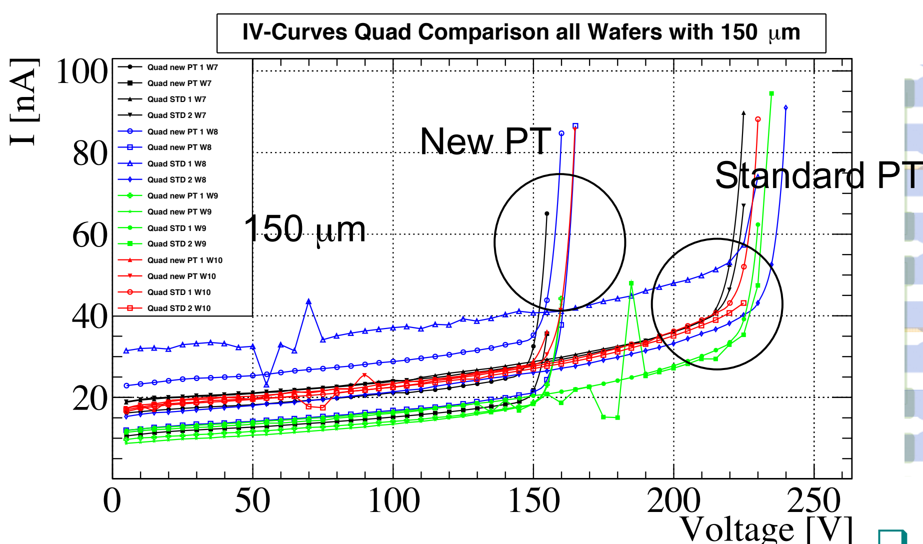
- 4 sensors geometries implemented:
  - 50x50 μm² with PT
  - 50x50 μm² NO PT
  - 25x100 μm² with PT
  - 25x100 μm² no PT

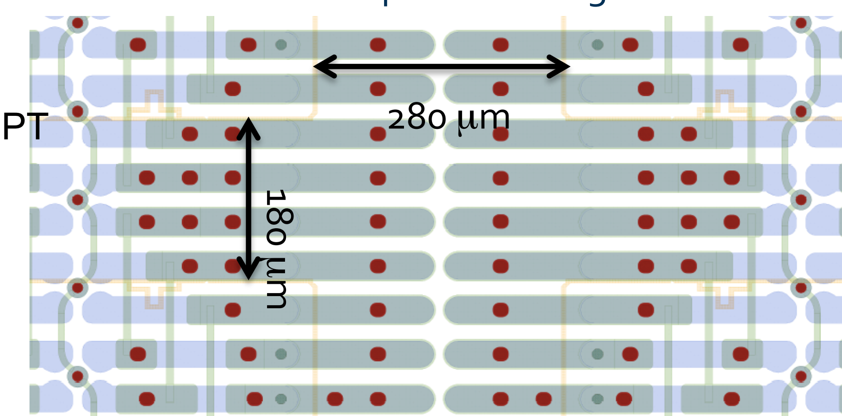
SOI3 production: FE-I4 quad sensors





- 4 rows of ganged pixels
- Standard punch-through structures





- 3 rows of ganged pixels
- Common punch-through structures for 4 pixels

Tuning of a 50 um thin sensor to a 600 e threshold