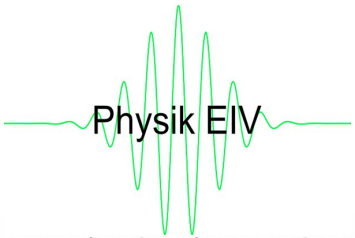
Total Ionization Dose effects in the FE-I4 front-end chip of the ATLAS Pixel IBL detector

Karola Dette[1,2] on behalf of the ATLAS Pixel Collaboration
[1]TU Dortmund, Germany; [2]CERN, Geneva, Schwitzerland

GEFÖRDERT VOM

Bundesministerium
für Bildung
und Forschung



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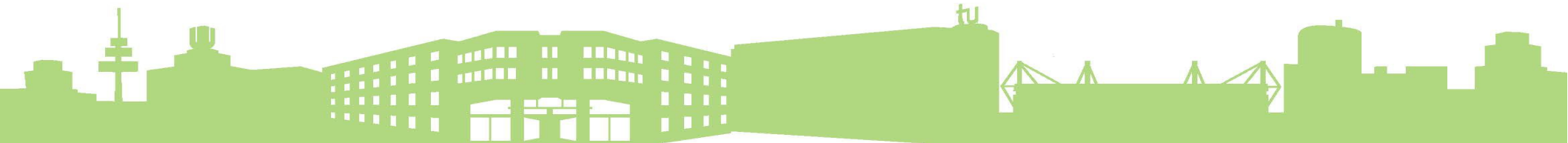
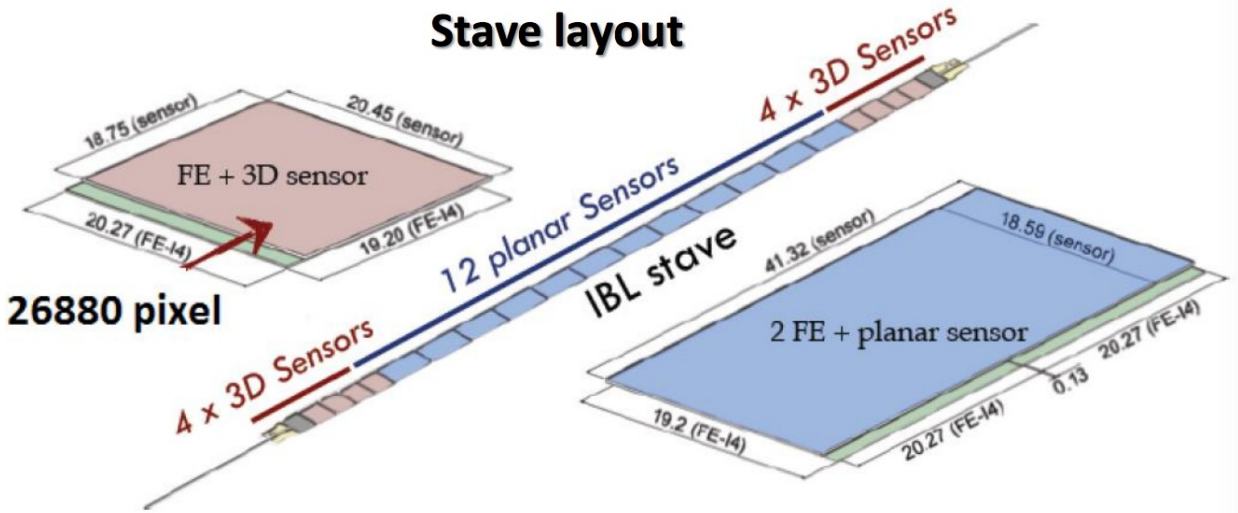


The IBL (Insertable B-Layer)

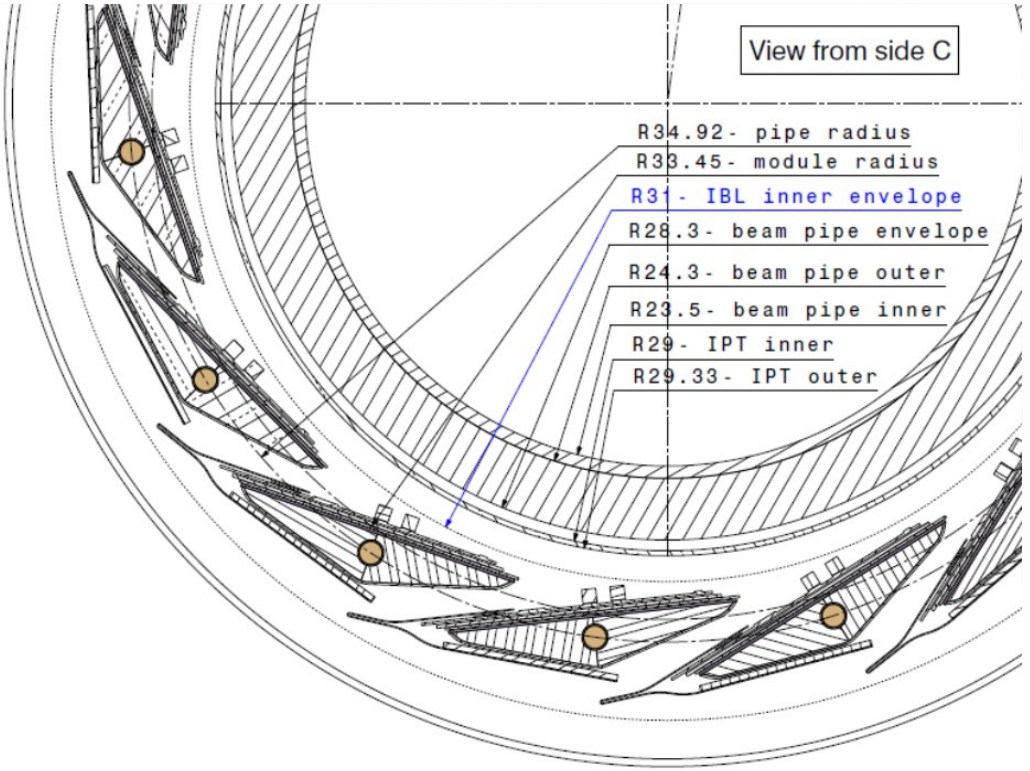


Detector overview:

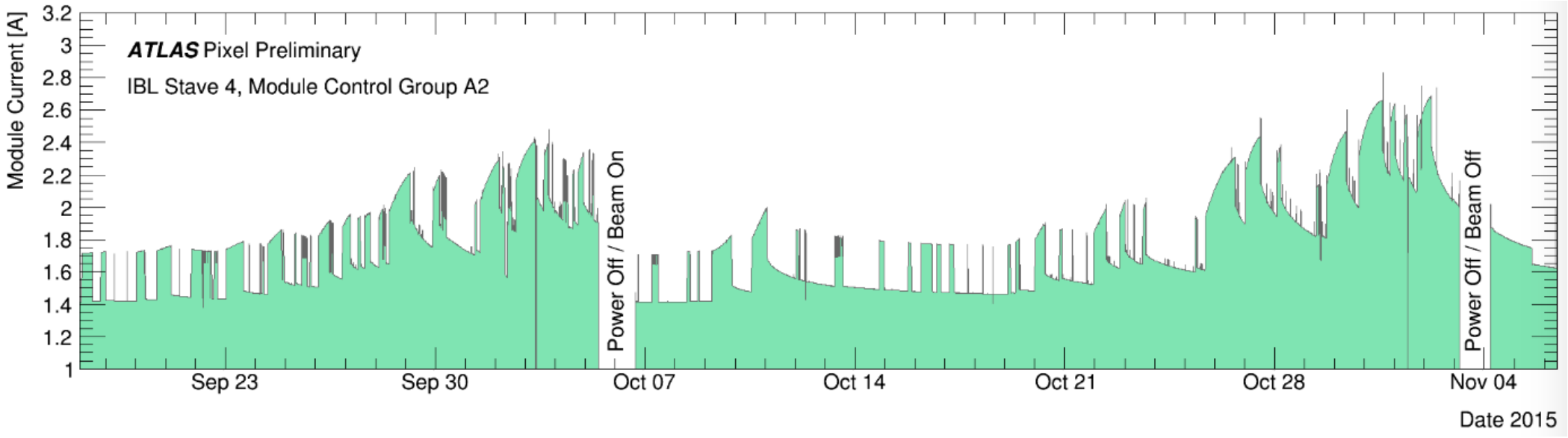
- 14 local support structures (staves) at r = 3.3 cm (Former B-Layer at 5.5 cm)
- 32 readout chips per stave

New readout chip FE-I4

- Smaller pixel size (50X250μm^2)
- Lower threshold and noise operation



Observations during operation



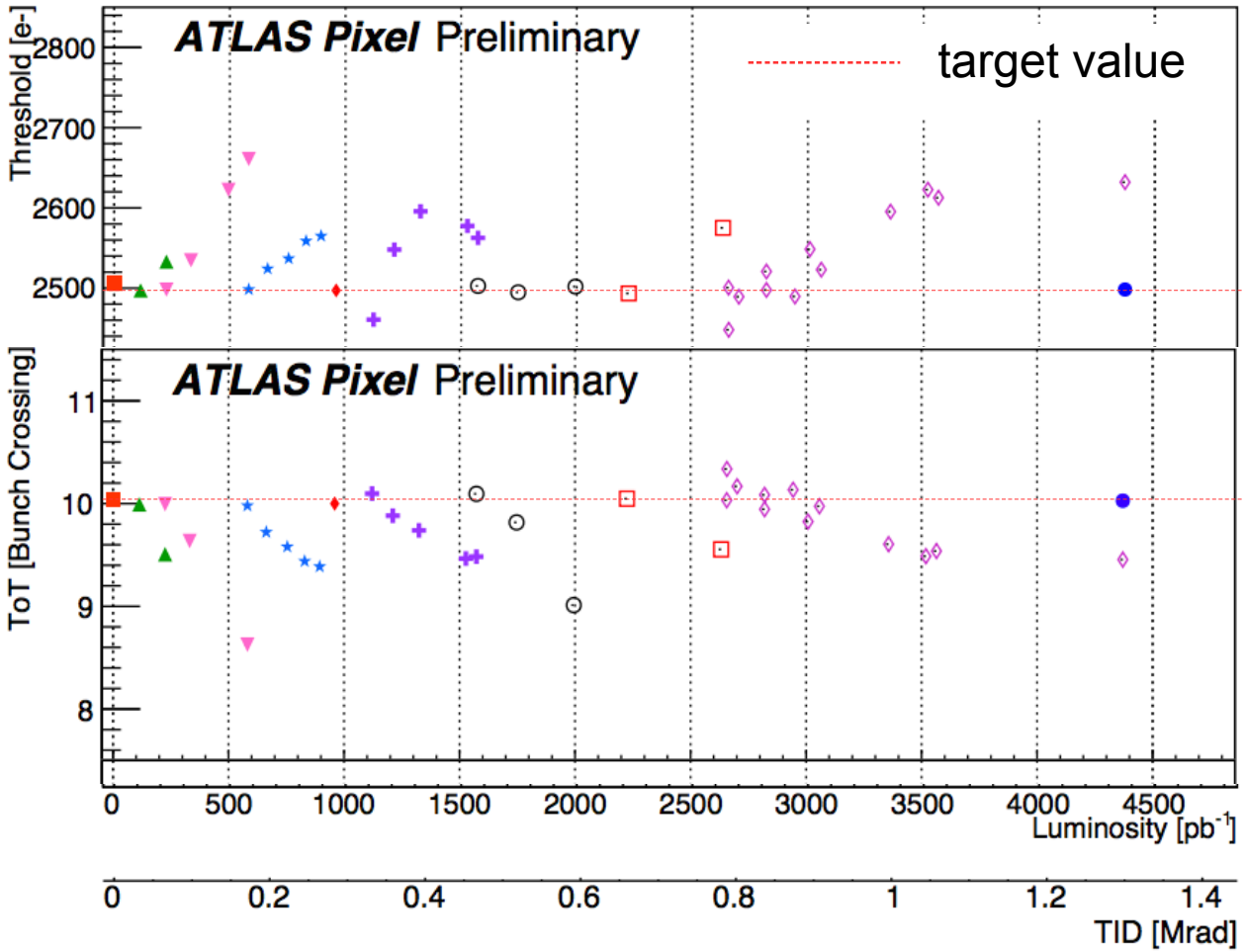
- low voltage current increase and drift of IBL calibration parameters (Threshold and ToT) observed after some months of operation

  Impact on data taking:

  IBL was switched off during one LHC fill due to safety concerns, in addition some modules were switched off that reached the current limit.

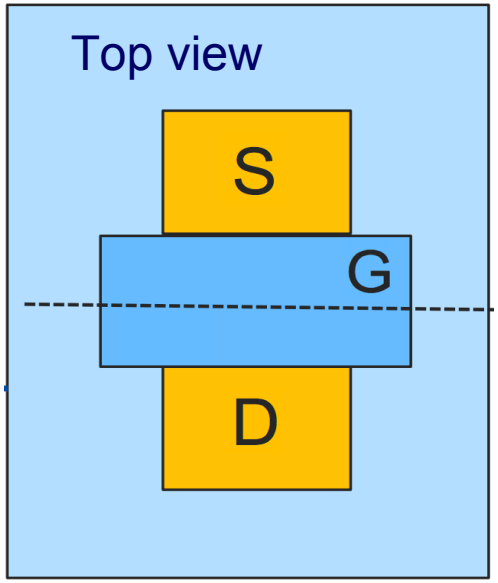
  BUT: FEs still functional, effect needs to be understood to prevent further disruptions

Drift of tuning parameters



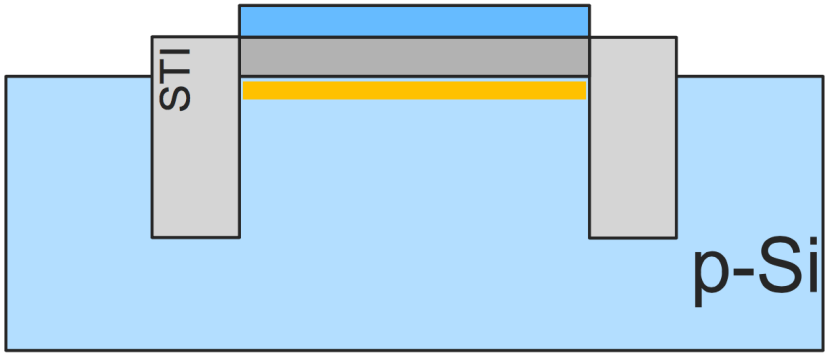
- nominal Threshold value (2500e) drifts upwards with increased integrated luminosity
- nominal ToT value (10BC) drifts downwards with increasing integrated luminosity
- Each color corresponds to a new re-tuning performed to get back to target value

NMOS radiation damage



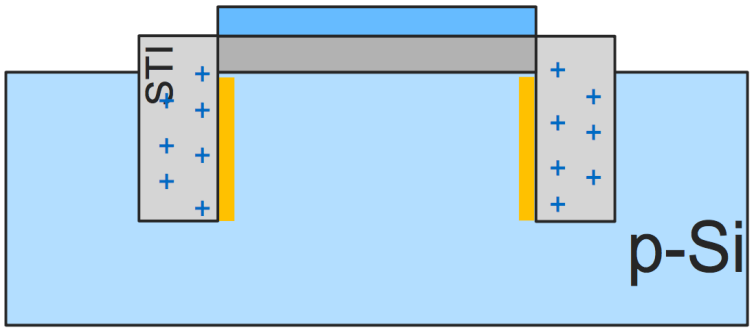
Top view of a NMOS transistor
Channel formation from S to D

Cross section before irradiation



Cross section at indicated line including Shallow Trench Isolation (STI)
Si to SiO2 interface transition:
dangling atomic bonds, acting as charge carrier traps.

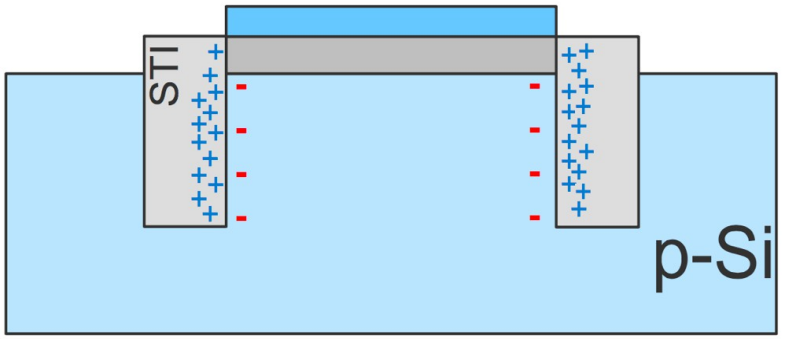
Low TID



After ionizing irradiation:
Channel formation due to electrical field of positive charges trapped in silicon oxide of the STI.

→ current increases due to positive oxide charges

High TID



Positive charge carriers move to SiO2-Si interface.
Interface traps become active in the Si.
Electrons are trapped and compensate the electrical field of the positive charges in the STI.

→ Leakage current decreases

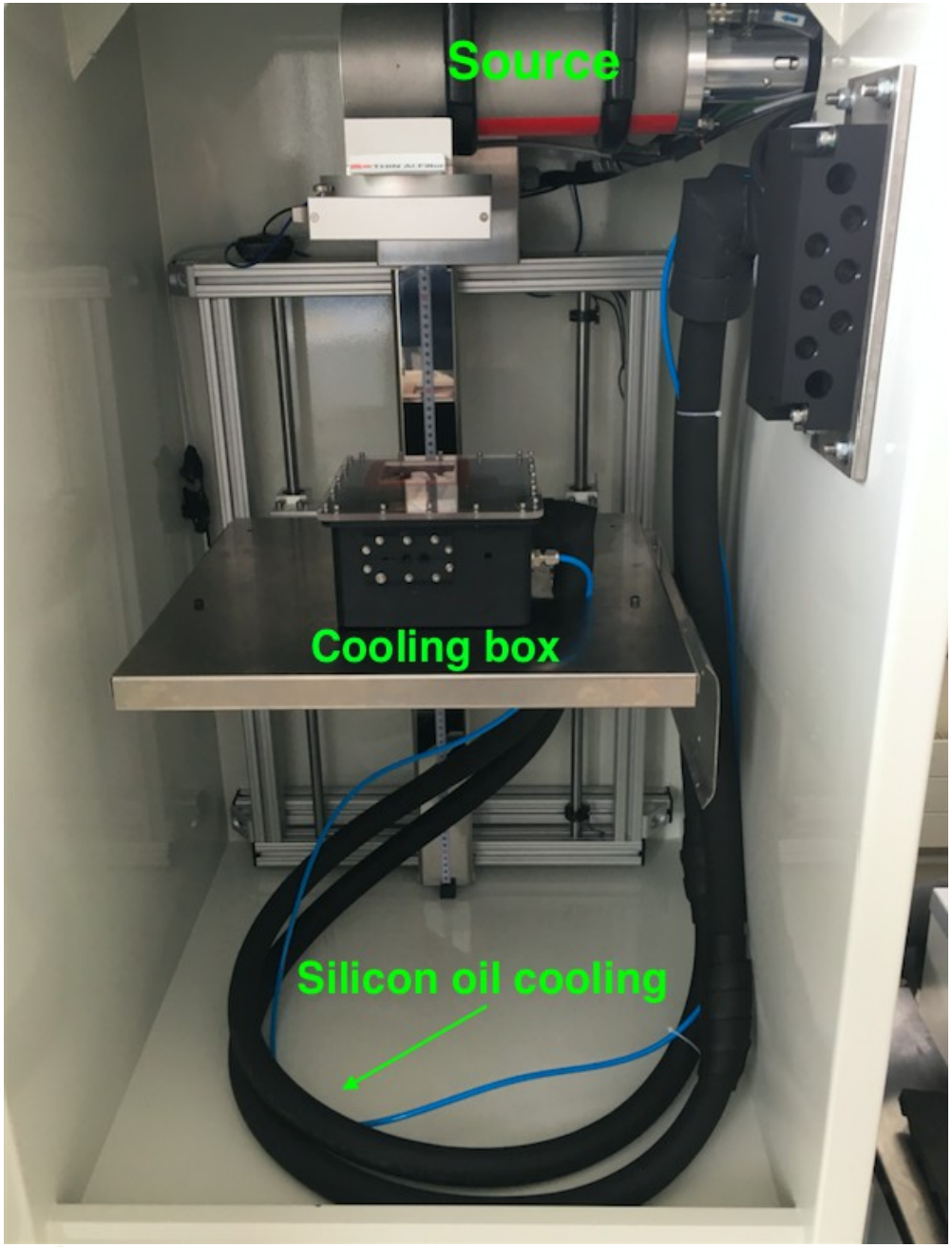
IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 52, NO. 6, DECEMBER 2005 2413 "Radiation-Induced Edge Effects in Deep Submicron CMOS Transistors"

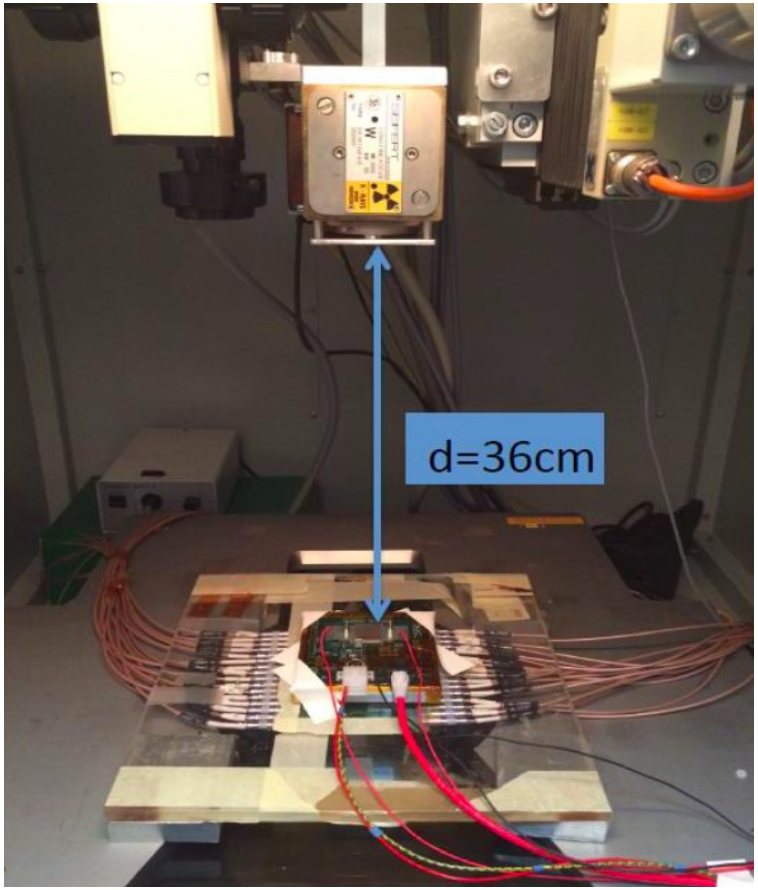
Questions to be answered for operation

- How high is the expected maximum current
- What is the lowest temperature safe for operation
- Will the positive oxide charges or the interface traps anneal / at what temperature does annealing happen

⟶ created task force to investigate current behavior in dedicated lab measurements

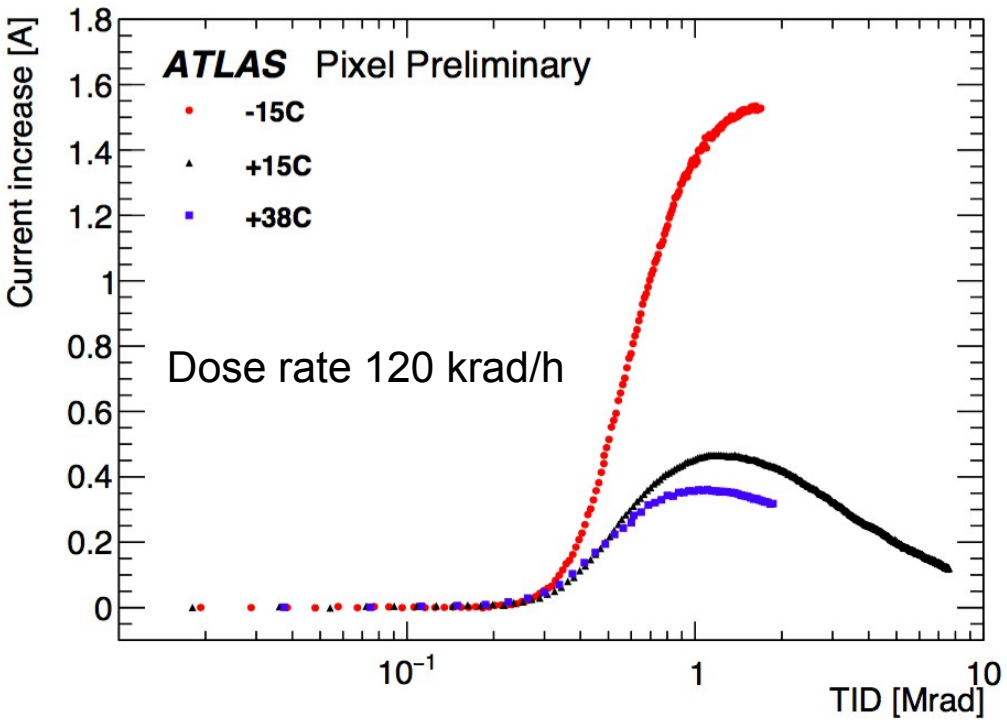
X-ray irradiation setups

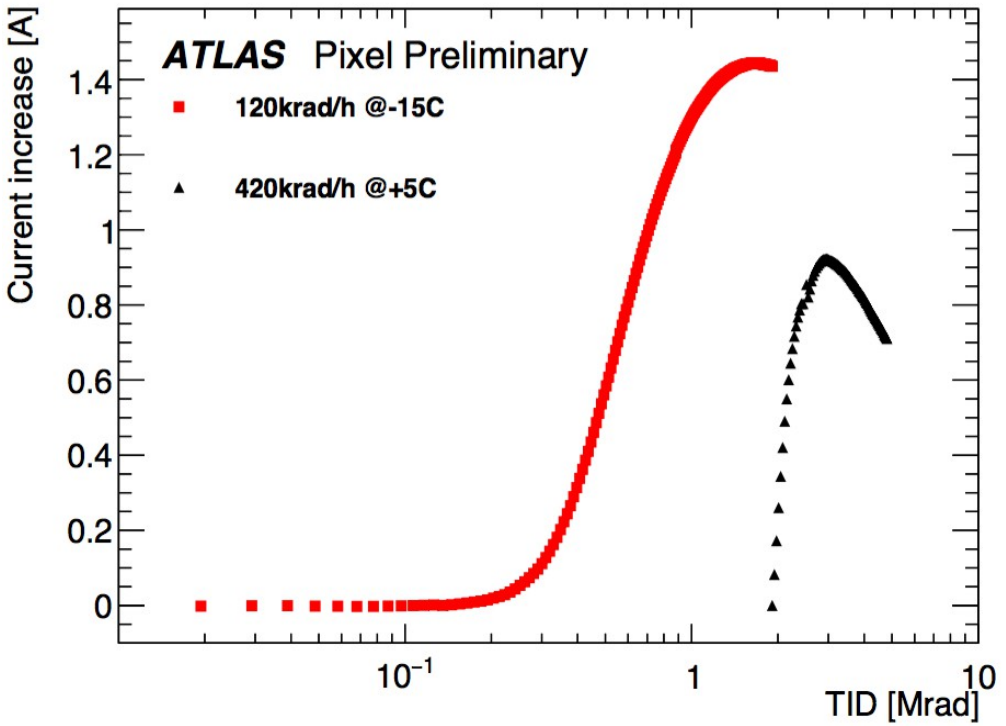


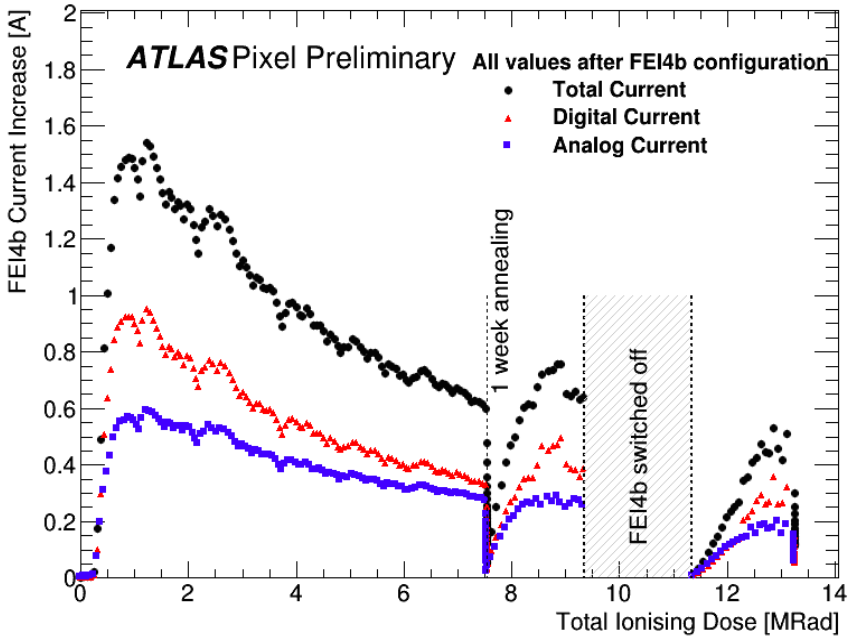


- Seifert RP149 machine and XRAD-iR-160
- Variable dose rate
- Bare FEI4b onto PCB
- Room temperature and cooled measurements

Irradiation results



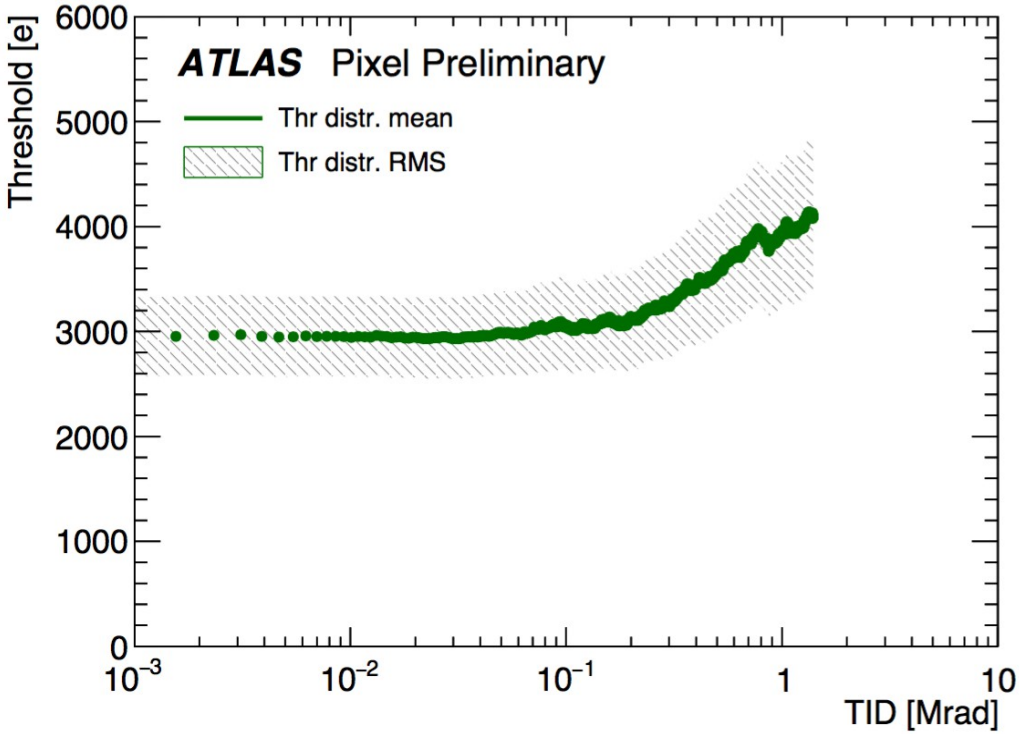


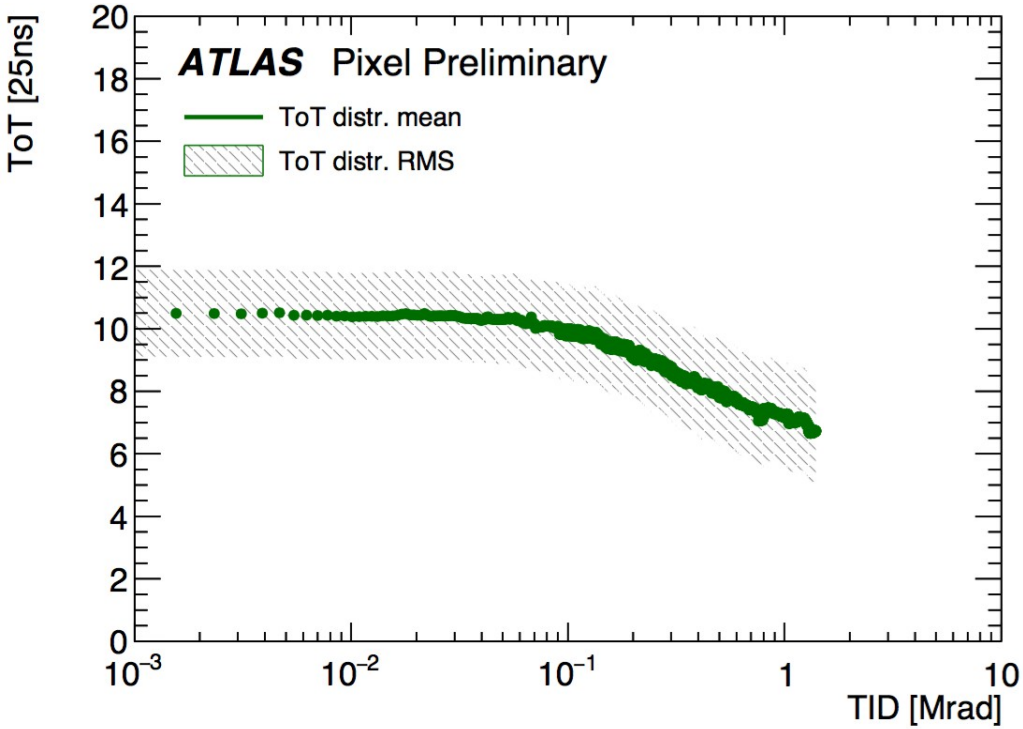


- two consecutive irradiation campaigns
- Between the irradiations several hour annealing period at room temperature

← Result from a comparison measurement performed with 18 MeV protons

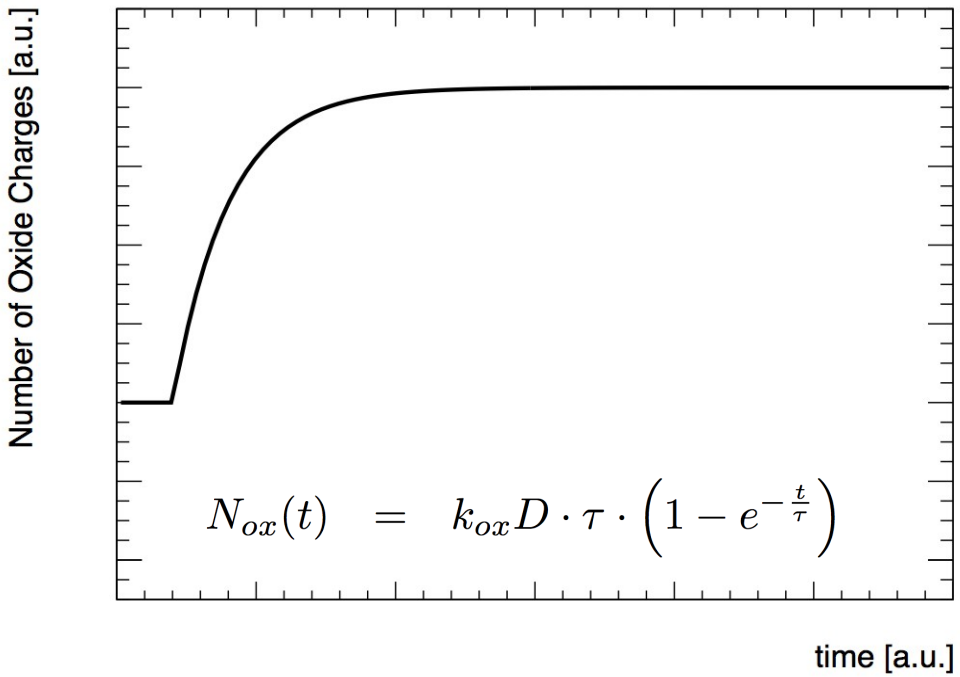
Shift in calibration parameters



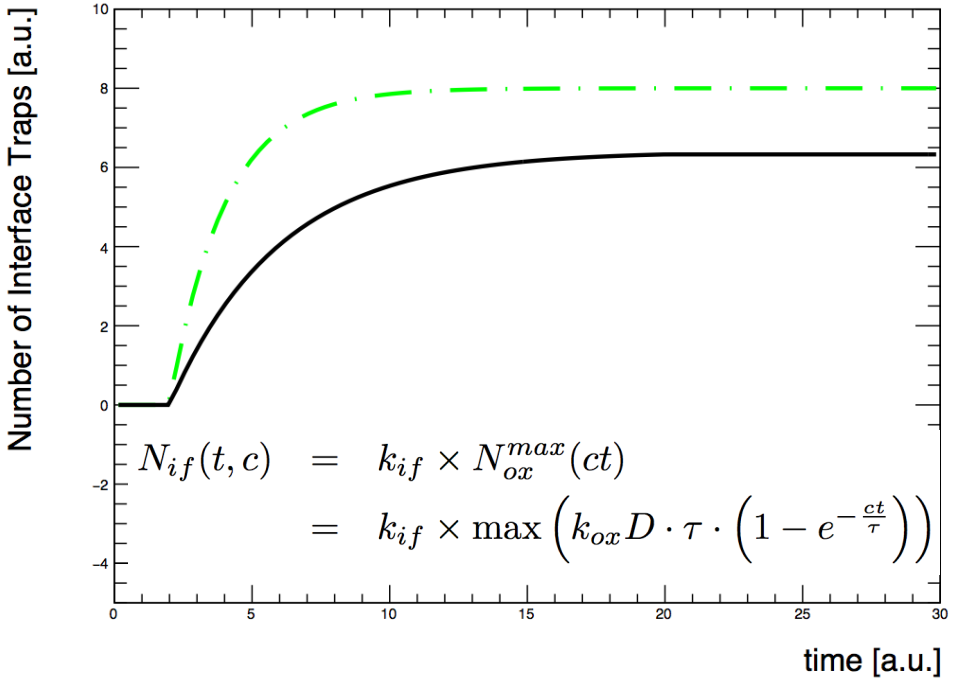


- Irradiation performed at 0 C and 10 krad/h dose rate (comparable to IBL operation conditions)
- Threshold and ToT values show the same trend as the shift observed in scans performed on IBL during interfills

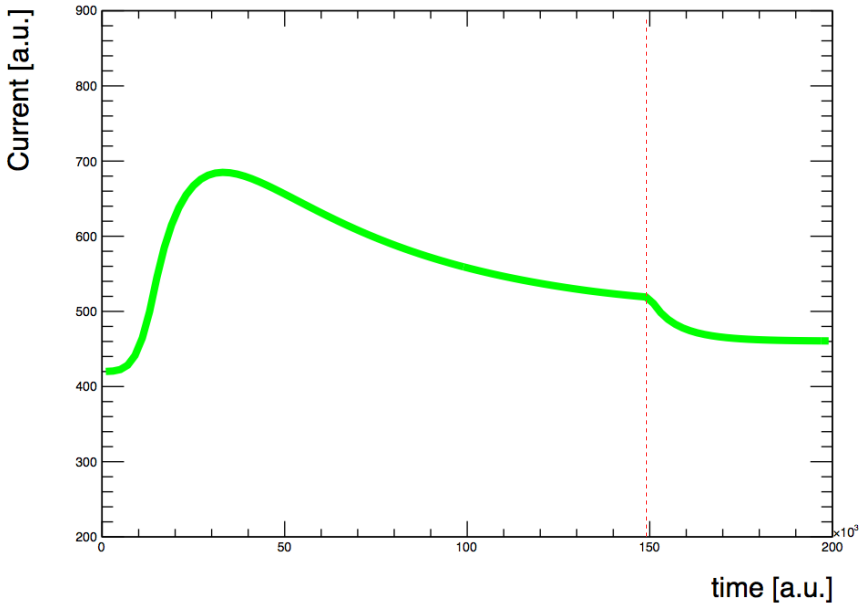
Basic assumptions



Number of positive charges as a function of time (for a fixed dose rate)

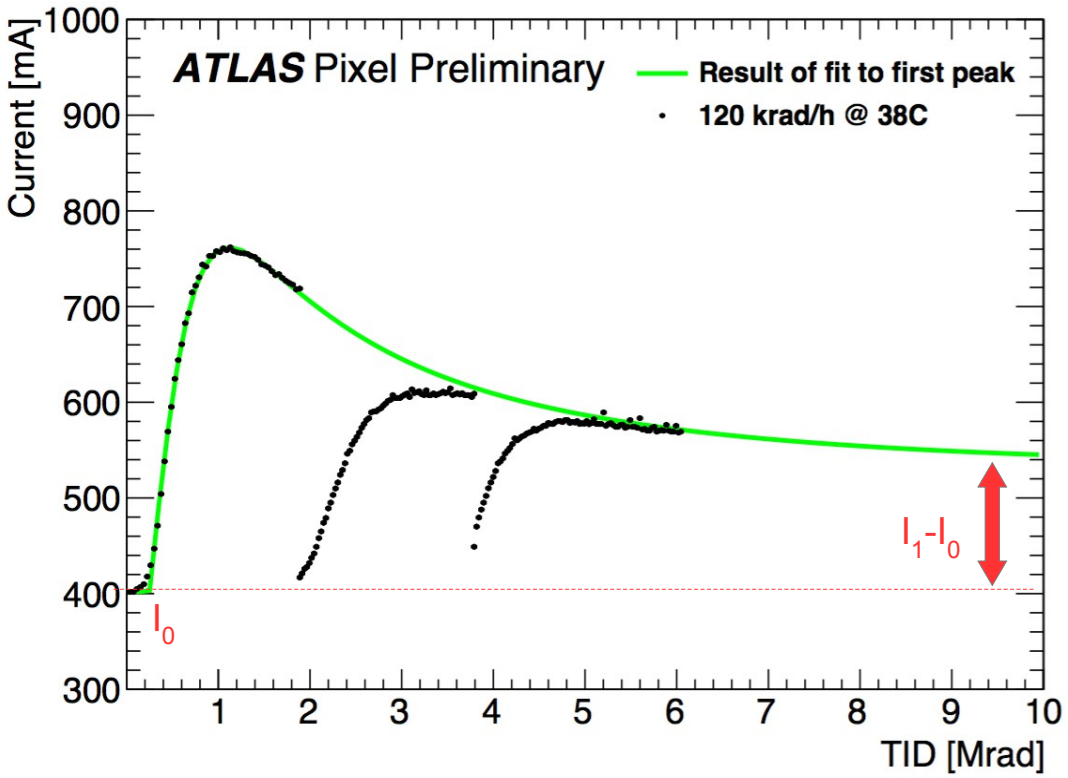


Number of activated interface traps (solid, black line) as a function of time, and the number of positive charges in the oxide (dashed green line)



The total current as a function of the time for arbitrary parameters. Annealing is simulated after the dashed line

First conclusions



- First measurement is giving „boundary current“

I_0 : Unirradiated current consumption

I_1 : Current consumption at high TID

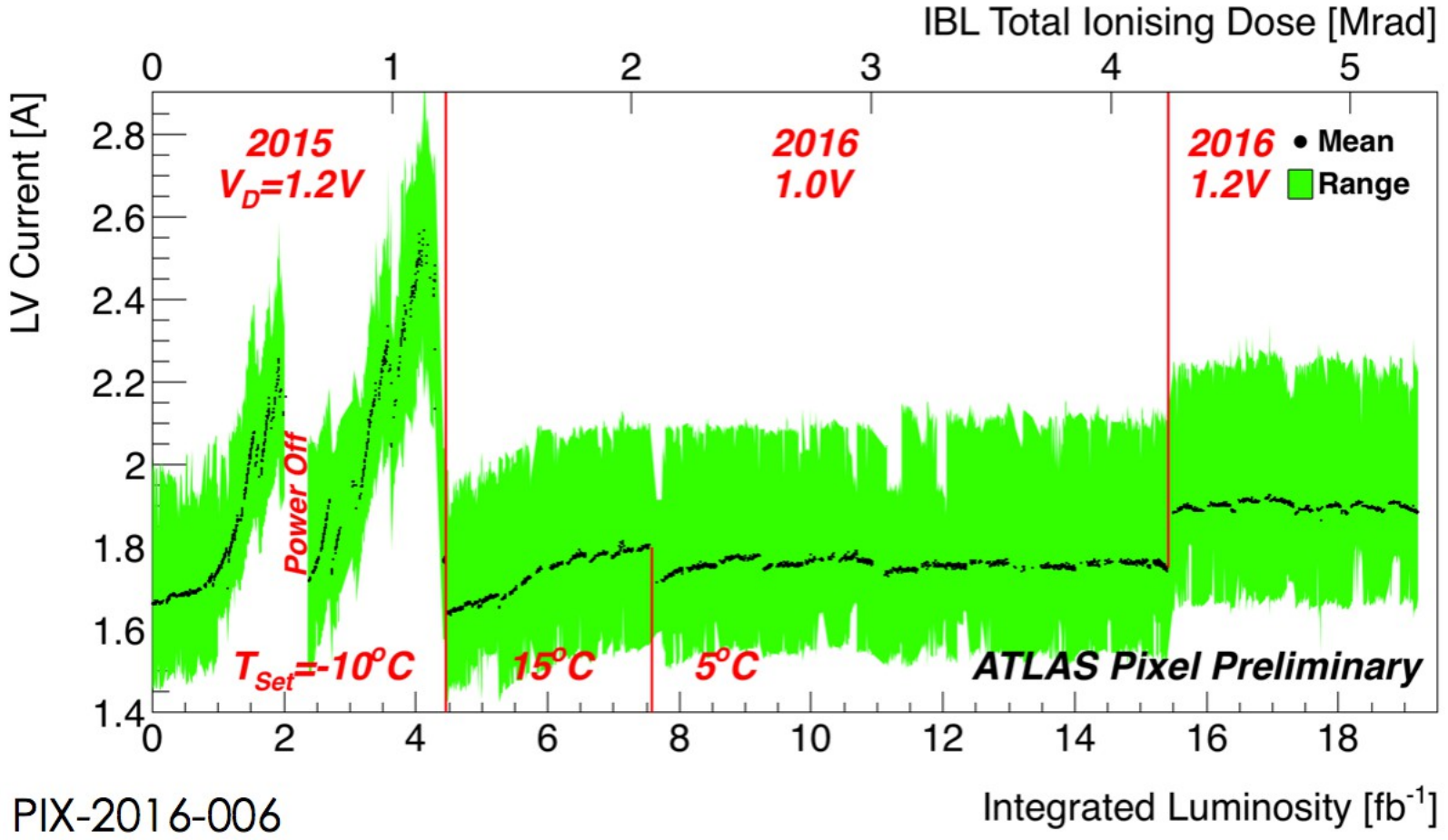
I_1 is technology + design dependent

→ Density of dangling bonds
→ Density of interface traps
→ Density of traps in the oxide
→ Saturation of positive charges

→ Current increase during first 1–2 Mrad of each irradiation step

A paper to describe the model in detail will be published soon by Malte Backhaus

Overview of LV current consumption



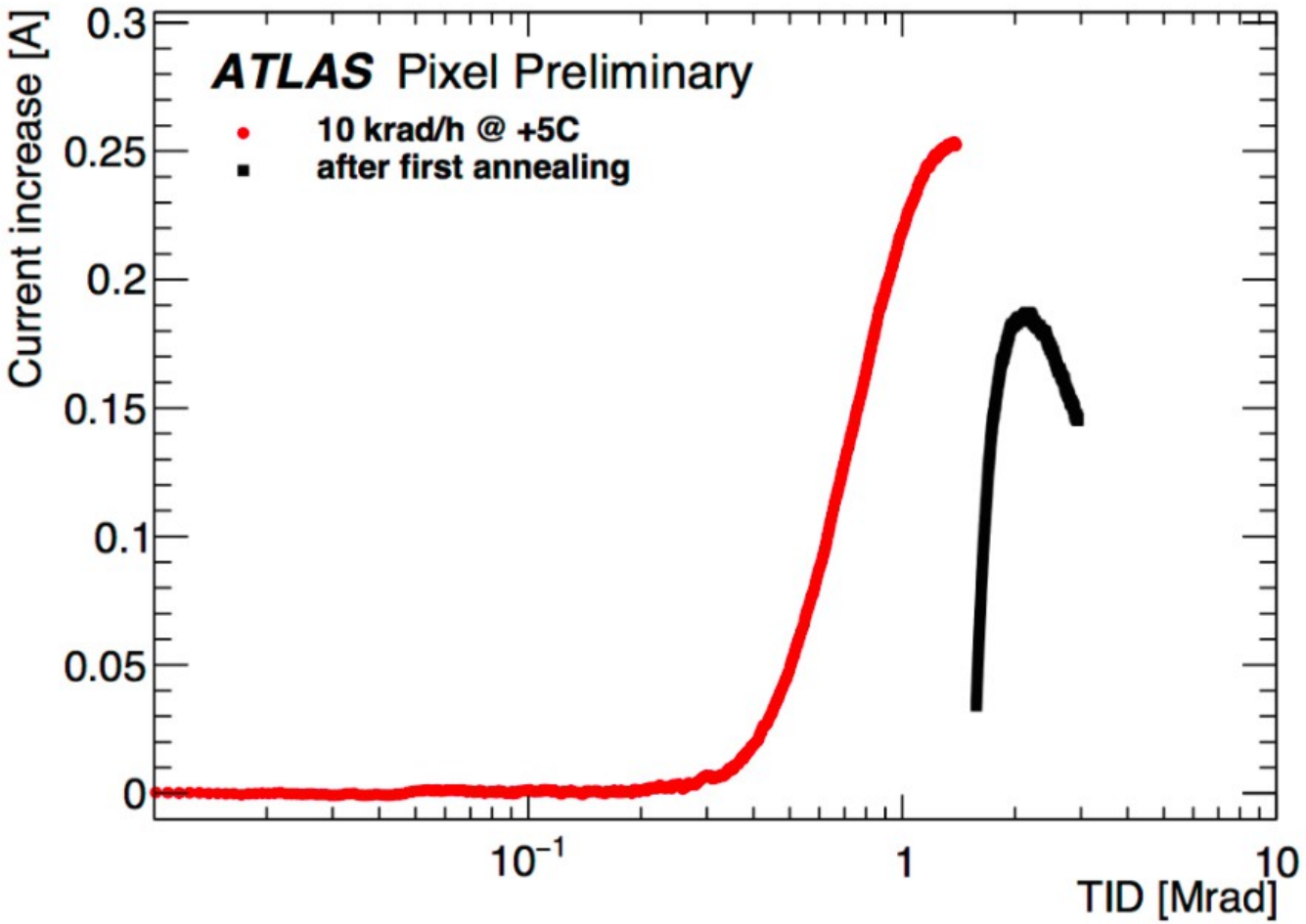
- After 2015 observations, decision was taken to increase temperature and decrease digital voltage
- Results of lab measurements led to decision to reduce the temperature and increase the digital voltage to 1.2V

Summary

- 2015 observation related to LV current increase was very concerning for operation in 2016 with increased peak luminosity
- In addition to the current increase a drift of calibration parameters was observed
- Test results confirmed hypothesis of NMOS leakage current at low TID as origin of LV current increase
- Irradiation data from X-ray and 18 MeV proton beam is giving comparable results
- Results from task force and lab investigations allowed to operate IBL without safety concerns
- IBL accumulated ~9 Mrad so far, maximum peak of current behind us

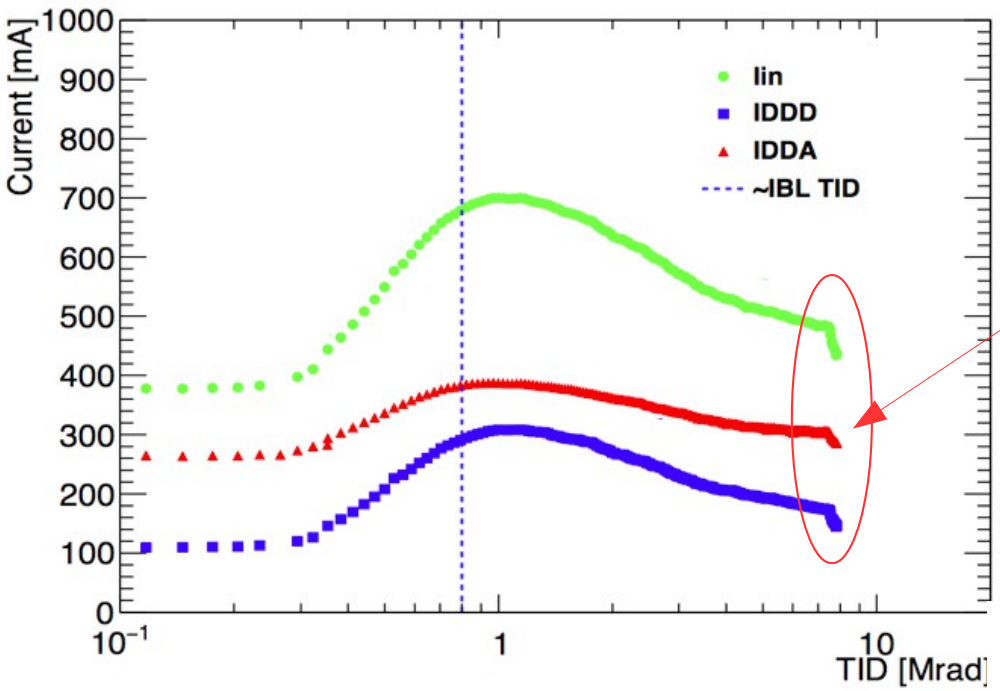
BACKUP

Measurement at expected LHC fluence



- current increase first peak in the order of 250 mA
  → would multiply to a current increase of 1 A for one IBL module group and not exceed safety limits
- IBL chips already went through some annealing times
  → should rather see a lower increase (second current peak) which was measured after 4 h of annealing.

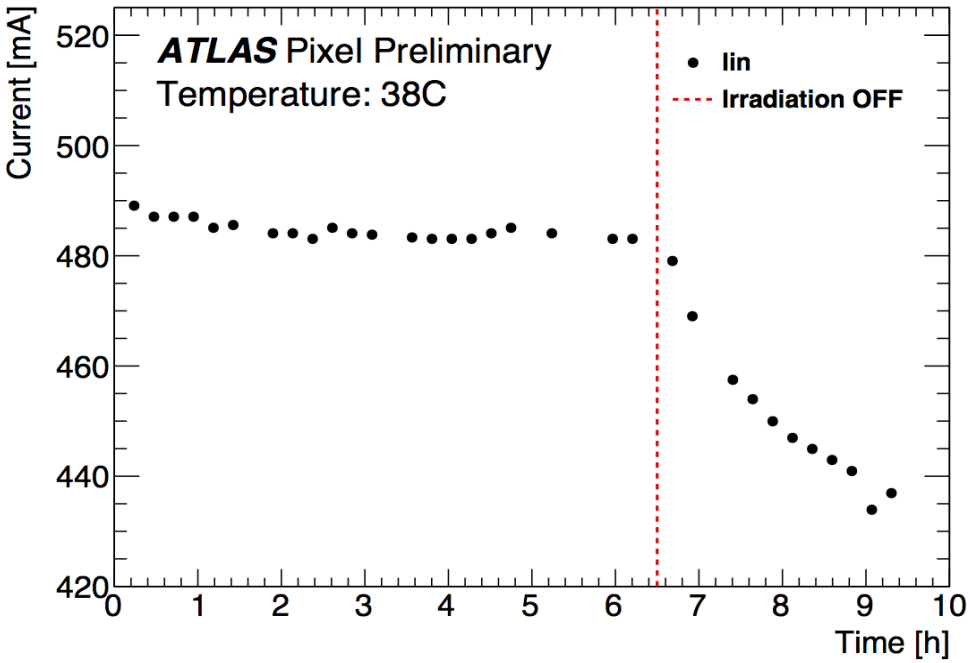
Current consumption during/after irradiation



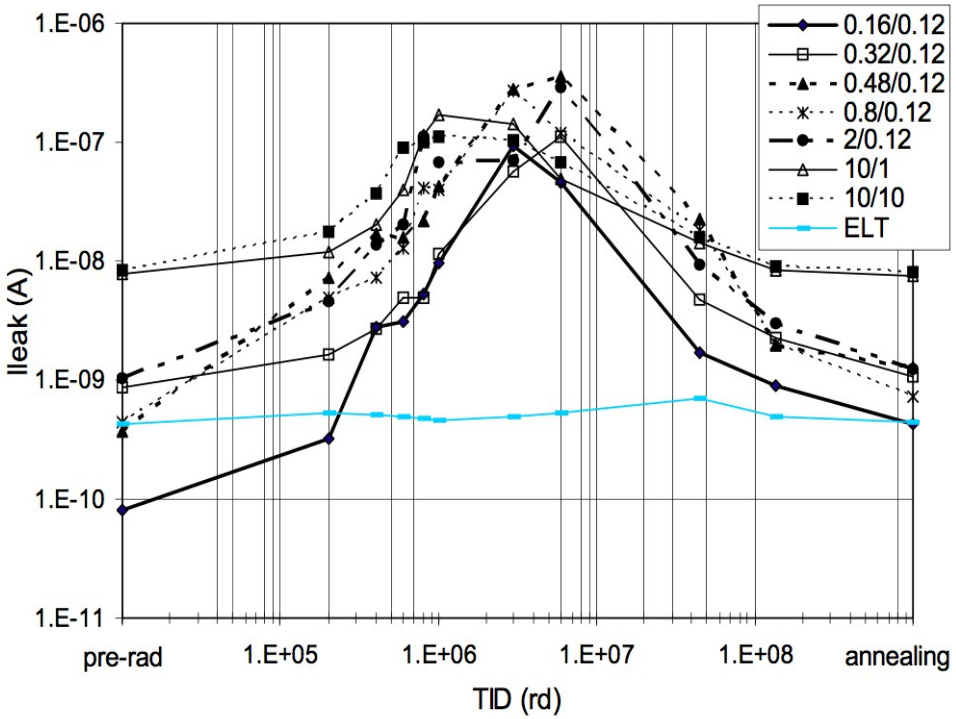
LV current consumption during and after stopping of irradiation

Blue line for comparison: accumulated TID for IBL during first year of operation

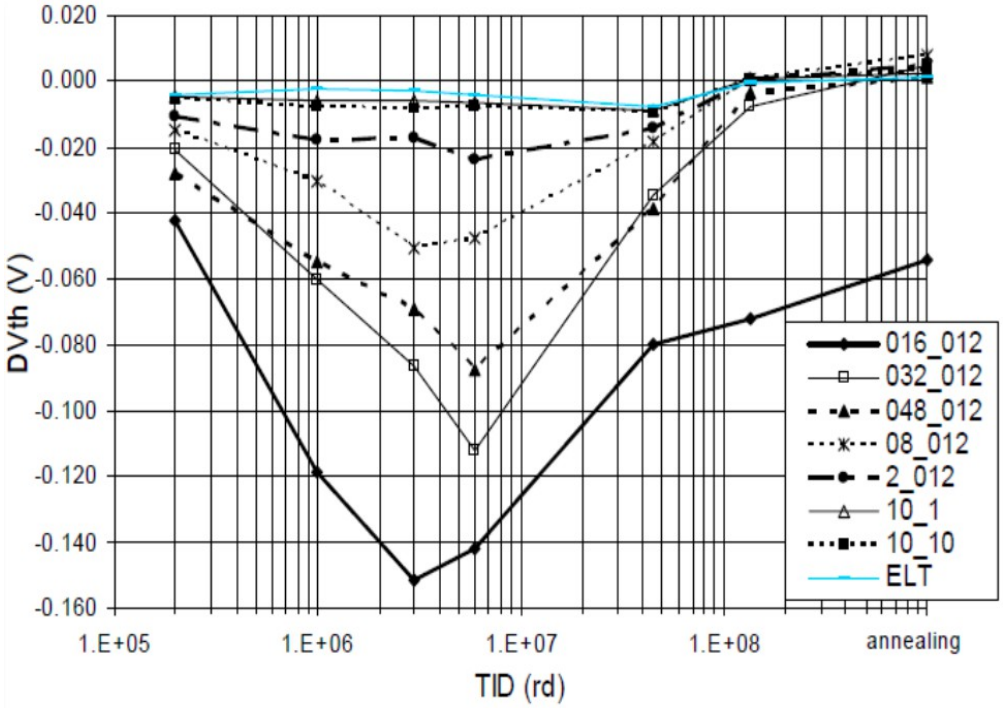
- The current consumption of the chip decreases after stopping the X-ray beam
- For this test the chip was powered during the recovery time
- similar trend observable for IBL modules during interfill periods



Previous measurements on NMOS transistors



Evolution of the leakage current with TID for different NMOS transistor size, up to 136 Mrd. The last point refers to full annealing at 100 C.
The first point to the left is the pre-rad value.



Threshold voltage shift with TID for different NMOS transistor size, up to 136 Mrd.
The last point refers to full annealing at 100 C

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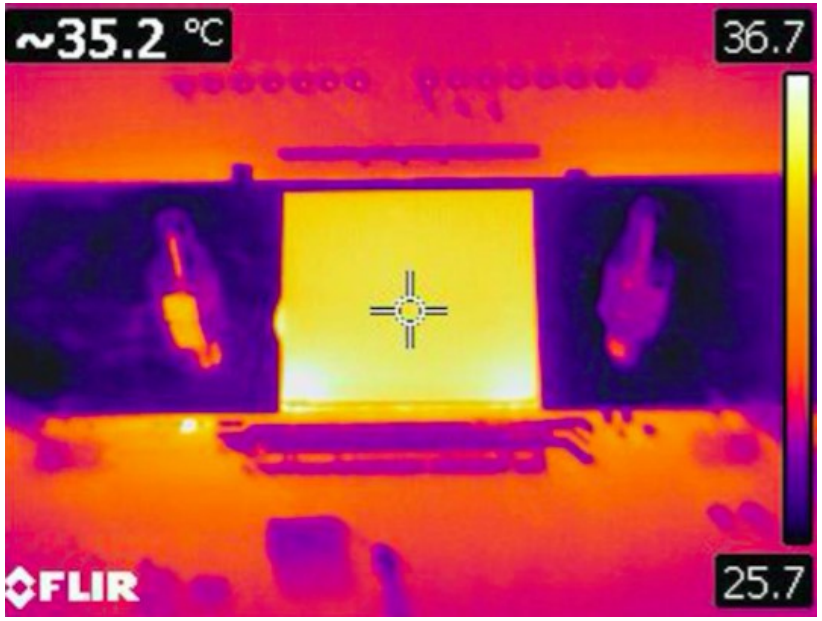
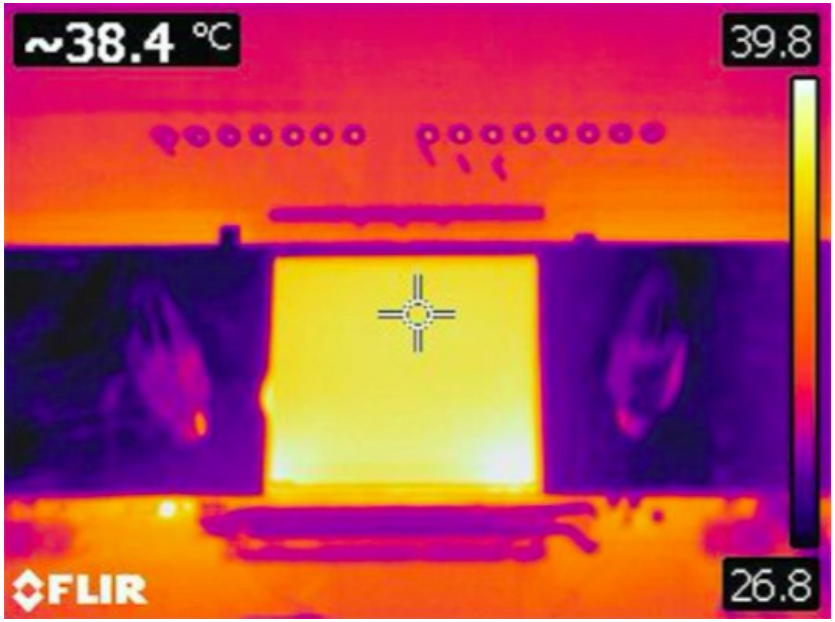
Uniformity check of current increase



After 10min of FE operation (no irrad)



After 60h of irradiation (TID ~ 8Mrad) and FE operation

- Right picture was taken after 9.4 Mrad
- no unexpected hot spots observed

→ points to uniform current increase