Recent Progress of RD53 Collaboration towards next generation Pixel ROC for HL_LHC

L. Demaria - INFN / Torino
on behalf of RD53 Collaboration

Talk layout

1. Introduction
2. RD53 Organization
3. Moving to full size protototype
    1. Analog Very Front Ends
    2. IP-blocks
    3. Small demonstrators
4. RD53A prototype
5. Radiation effects
6. Conclusions

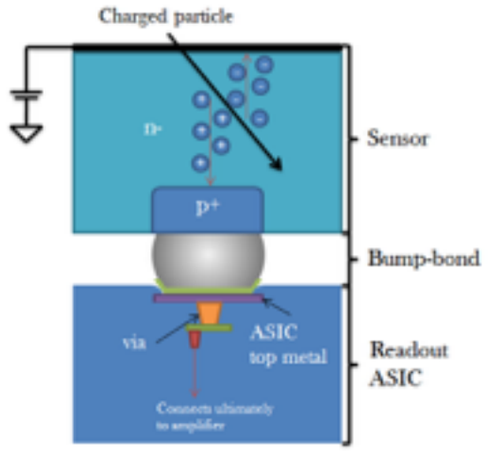
Pixel Detector at HL_LHC

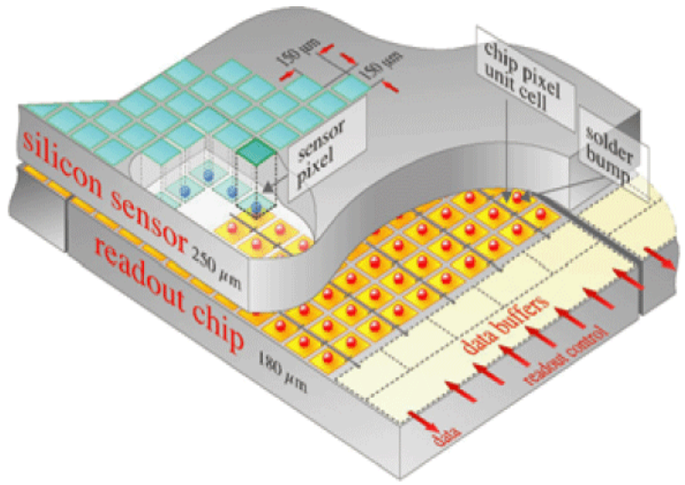
Requirements from HL_LHC experiments

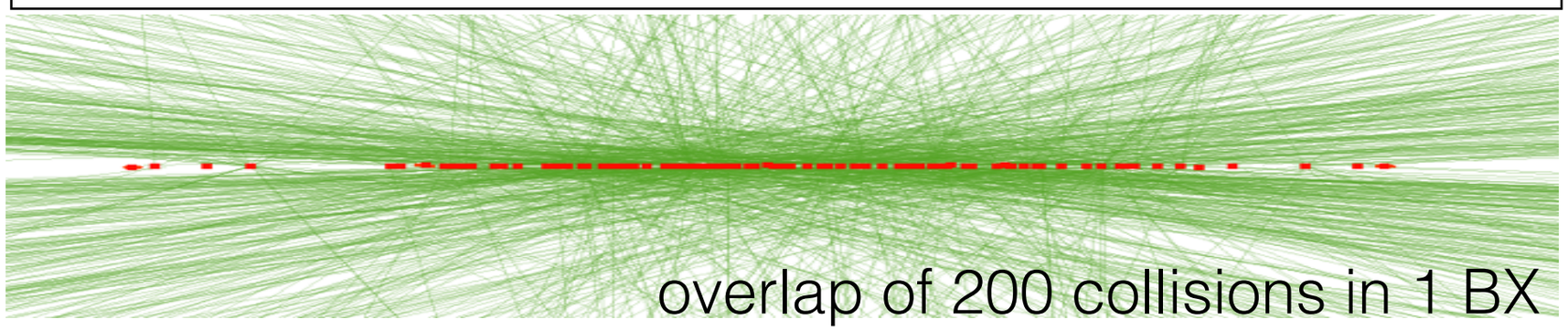
Small pixels: 50x50um^2
Large chips: 2cm x 2cm (~1 billion transistors)
Pixel Hit rates: up to 3 GHz/cm^2 (200 P.U.)
Radiation: 1Grad, 10^{16} n/cm^2 (unprecedented)

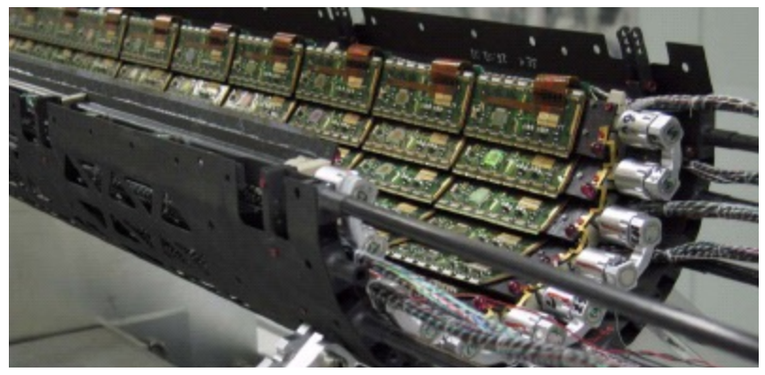
Trigger: up to 1MHz with 12.8us latency
(~100x buffering and readout)
Low power - Low mass systems

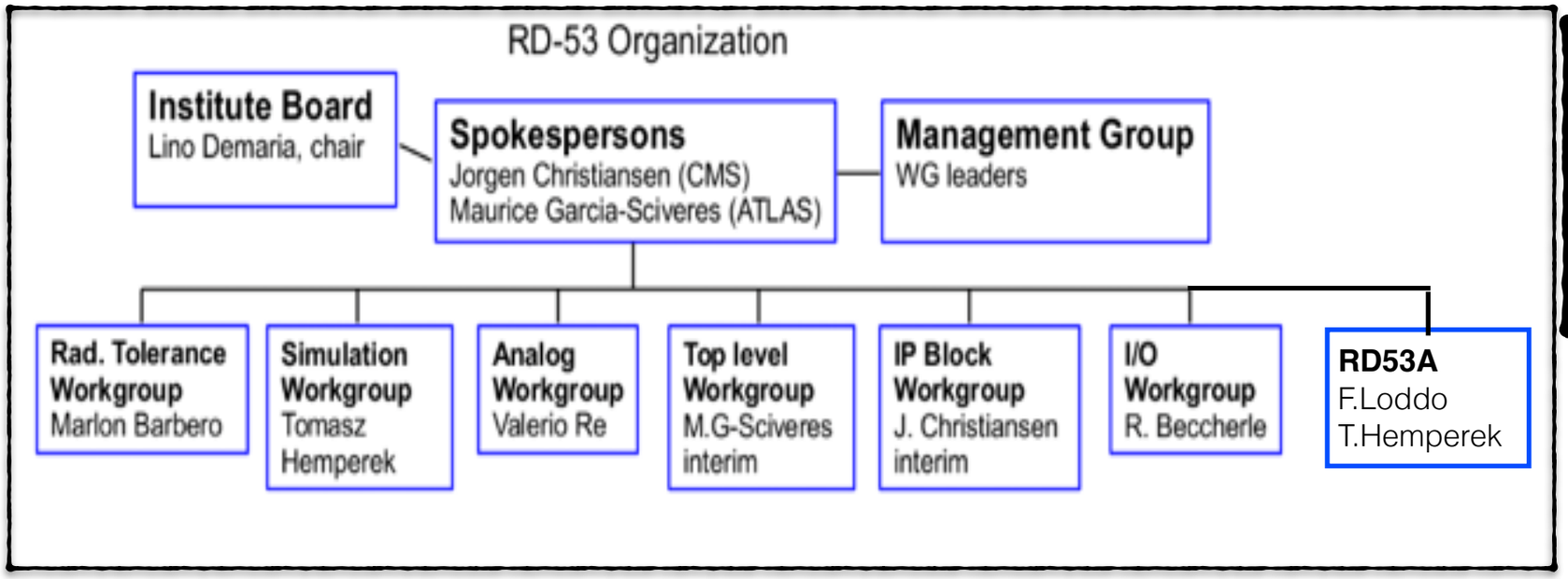
Data readout : up to 4-5 Gbs/s
TRIGGER Latency up to 12.8us (x3) ==> deeper storage buffer











	Country	Town	Institute	Inst. Representative
1	Czech Republic	Prague	FNSPE-CTU/IP-ASCR	Miroslav Havranek
2	France	Marseille	CPPM	Alexandre Rozanov
3	France	Paris	LPNHE	Giovanni Calderini
4	Germany	Bonn	Bonn University	Hans Krüger
5	Italy	Bari	INFN and Politecnico	Flavio Loddo
6	Italy	Milano	INFN and University	Valentino Liberali
7	Italy	Padova	INFN and Politecnico	Alessandro Paccagnella
8	Italy	Pavia	INFN and University	Valerio Re
9	Italy	Perugia	INFN and University	Gian Mario Bilei
10	Italy	Pisa	INFN and University	Fabrizio Palla
11	Italy	Torino	INFN and University	Natale Demaria
12	Netherlands	Amsterdam	NIKHEF	Nigel Hessey
13	Spain	Sevilla	Sevilla University	Rogelio Palomo
14	Switzerland	Geneva	CERN	Jorgen Christiansen
15	UK	Didcot	Sc.&Tech Facilities Council	Mark Prydderch
16	USA	Chicago	Fermilab	David Christian
17	USA	Berkeley	University of California	Beate Heinemann
18	USA	Albuquerque	Univ of New Mexico	Sally Seidel
19	USA	Santa Cruz	U.C. Santa Cruz	Alex Grillo

RD53 Collaboration
is a real and effective synergy
among CMS-ATLAS communities
with a specific and focused goal
with a real main deliverable:
a **LARGE scale FRONT-END ASIC prototype for Pixel-Phase 2 detectors**

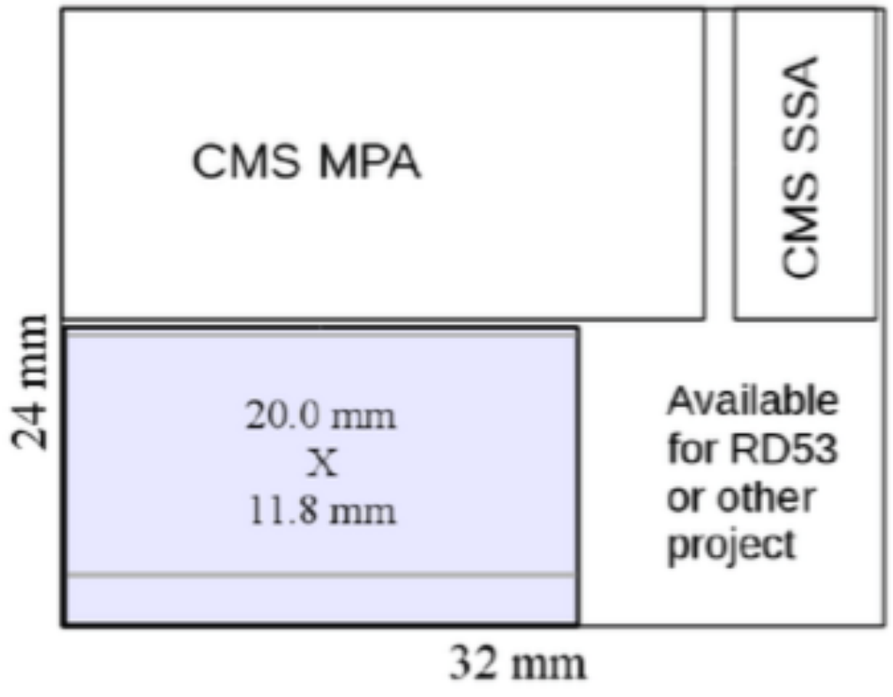
Personal comment:
quite unique experience
challenging when going to decision
EXCELLENT melting pot !

Institutes:
8 CMS, 2 CMS/ATLAS, 9 ATLAS

Web-site: http://rd53.web.cern.ch/rd53/

Full Scale prototype

- Proposed 20x11.8 mm² chip (→ 400x192 pixels), 50x50 µm² pixel
- *Goal*: demonstrate in a large format IC
  - suitability of 65nm technology (including radiation tolerance ≥ 500 Mrad)
  - high hit rate: 3 GHz/cm²
  - dead time loss < 1%
  - trigger rate: 1 MHz
  - low in-time threshold: ~ 1000 e⁻, high speed readout
  - serial powering
- Not intended to be a production chip
  - will contain design variations for testing purposes
  - wafer scale production will enable prototyping of bump bonding assembly with realistic sensors in new technology
    → performance measurement



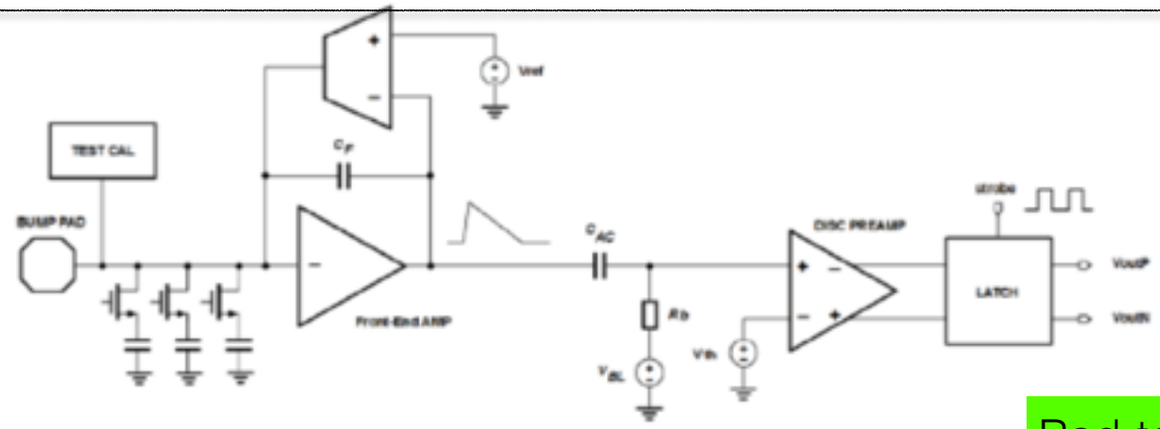
- ❑ **To be completed: December 2016**
- ❑ **To be submitted: End of March 2017**

Sepcs document: CERN-RD53-PUB-15-001 **http://cds.cern.ch/record/2113263**

Essential Components for FE-ASIC:

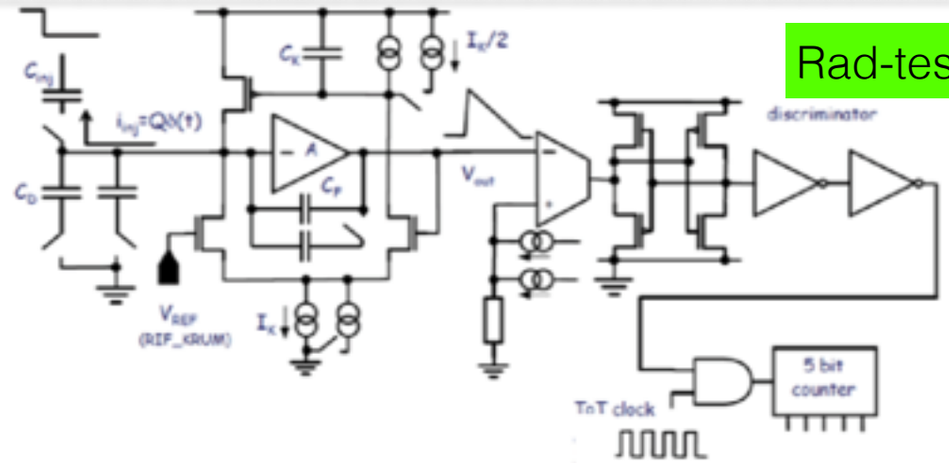
Analog VFE IP-Blocks

Four VFE analog designs



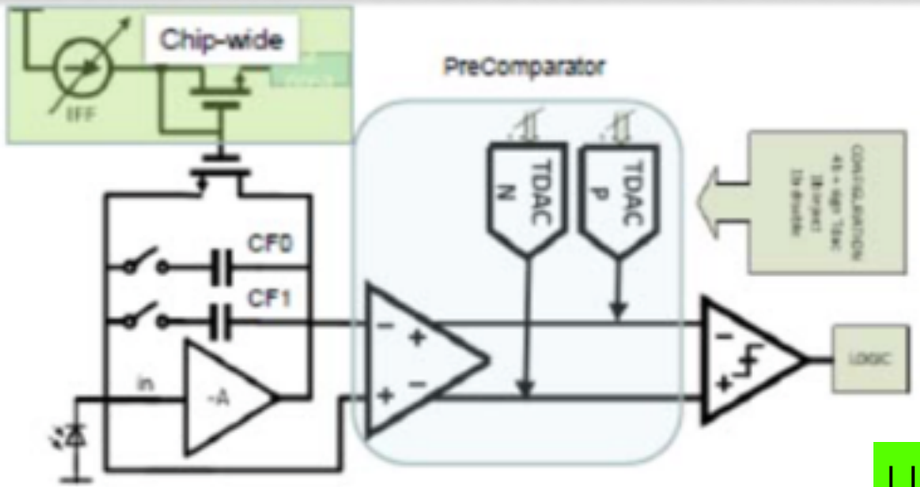
Rad-tested

INFN Torino **– single stage with SAR-like ToT counter using synchronous comparator**



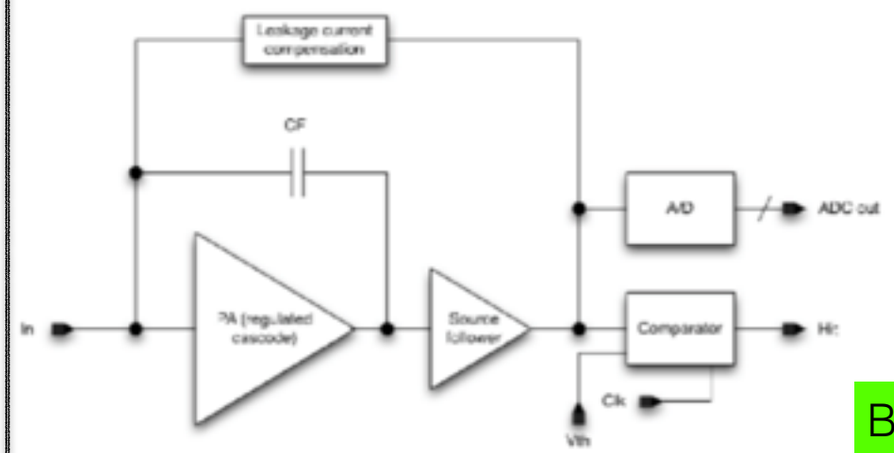
Rad-tested

INFN Bergamo/Pavia **– single stage with current comparator and ToT counter**



Under-test

LBNL **– continuous reset integrator first stage + DC-coupled pre-comparator stage**



Back on Sept

INFN-FNAL **– zero dead time and flash ADC**

They must be **fully tested** (also after irradiation) in their (almost) final version to be safely included in RD53A

RD53: IP blocks

- List of required ~20 IP blocks: assigned to various groups
- Initial specs review done in June 2014
  - 2014: 7 first prototypes submitted
  - 2015: remaining prototypes
  - 2016: versions for RD53A
- IP-block for RD53A have to be prototyped, characterised and tested before / after irradiation up to at least 500 Mrad.

BIAS	• Band Gap	: **CPPM**, **Pavia**, **CERN**
	• DAC	: **Bari**, Prague
In/Out	• I/O PAD	: **CERN, LBNL**
	• SLVDS driver	: **Pavia**, **Pisa**
	• SLVDS receiver	: **Pavia,Pisa**
	• PLL	: Bonn
	• SER	: Bonn, **Pisa**
	• DES	: **Pisa**
	• CDR	: Bonn
	• Cable Driver	: Bonn
Power Monitor	• Monitoring ADC	: **CPPM**, **Bari**, **CERN**
	• Temperature Sensor:	**CPPM**
	• Radiation Sensor	: **CPPM**
	• Analog Buff RtoR	: RAL
	• Power-ON Reset	: **Sevilla**
	• Shunt LDO	: Dortmund
	• Config. Memories	: **CPPM**
	• SRAM EOC	: **CERN**, **Milano**
	• Others : VCO, EFUSE, DC-DC….	

IP on bold have prototypes TESTED and oK

Small Size (64x64 pixel(s) Demonstrators

- FE65p2 demonstrator
- CHIPIX65 demonstrator

Small demonstrators

They are a full exercise of chip integration and constitute a trial version before moving to the full size prototype. Both (2x2) analog Islands on digital

- **FE65P2** (LBNL + Bonn)
  - digital architecture for pixel region (evolution of FEI4) 4b-ToT
  - single **Analog VFE : LBNL version**

- **CHIPIX65_demo** (INFN)
  - new architecture for pixel region (larger sharing of latency buffer)
  - Proving **Multiple Analog VFE : Torino, Pavia versions**
  - **IP-block from RD53**

	Pixel Matrix	Analog VFE	Analog / Digital Isolation	IP-Block	Pixel Region & Arch	Bias-Distrib	Powering	Digital CORE
FE65P2	64x64 pixels	AFE_LBNL	Analog in deep n-well Digital in deep n-well PAD in deep n-weel	few and not RD53A	(2x2) Distributed Latency Buffer	Single stage mirroring	standard	(4x64)
CHIPIX65 demonstrator	64x64 pixels	AFE_TO AFE_PV	Analog in deep n-well	**RD53A IP-blocks**: DAC, ADC, SER, sLVS-TX, sLVS-RX, Bandgap, CERN I/O Pads	(4x4) central Latency Buffer	Double stage mirroring	standard	(4x4)
RD53A	400x192 pixels	AFE_LBNL AFE_TO AFE_PV AFE_FNAL -- tbc : review	Analog in deep n-well Digital in deep n-well PAD in substrate tbc	**RD53A IP-blocks**: DAC, ADC, SER, sLVS-TX, sLVS-RX, Bandgap, CERN I/O Pads, PLL , ShuntLDO, T-sens, Rad-sens	tbd	Double stage mirroring	standard / Serial-Poweering	(8x8) / (4x16)

FE65P2 demonstrator

CERN ATLAS EXPERIMENT

Institutes: LBNL, Bonn

BERKELEY LAB

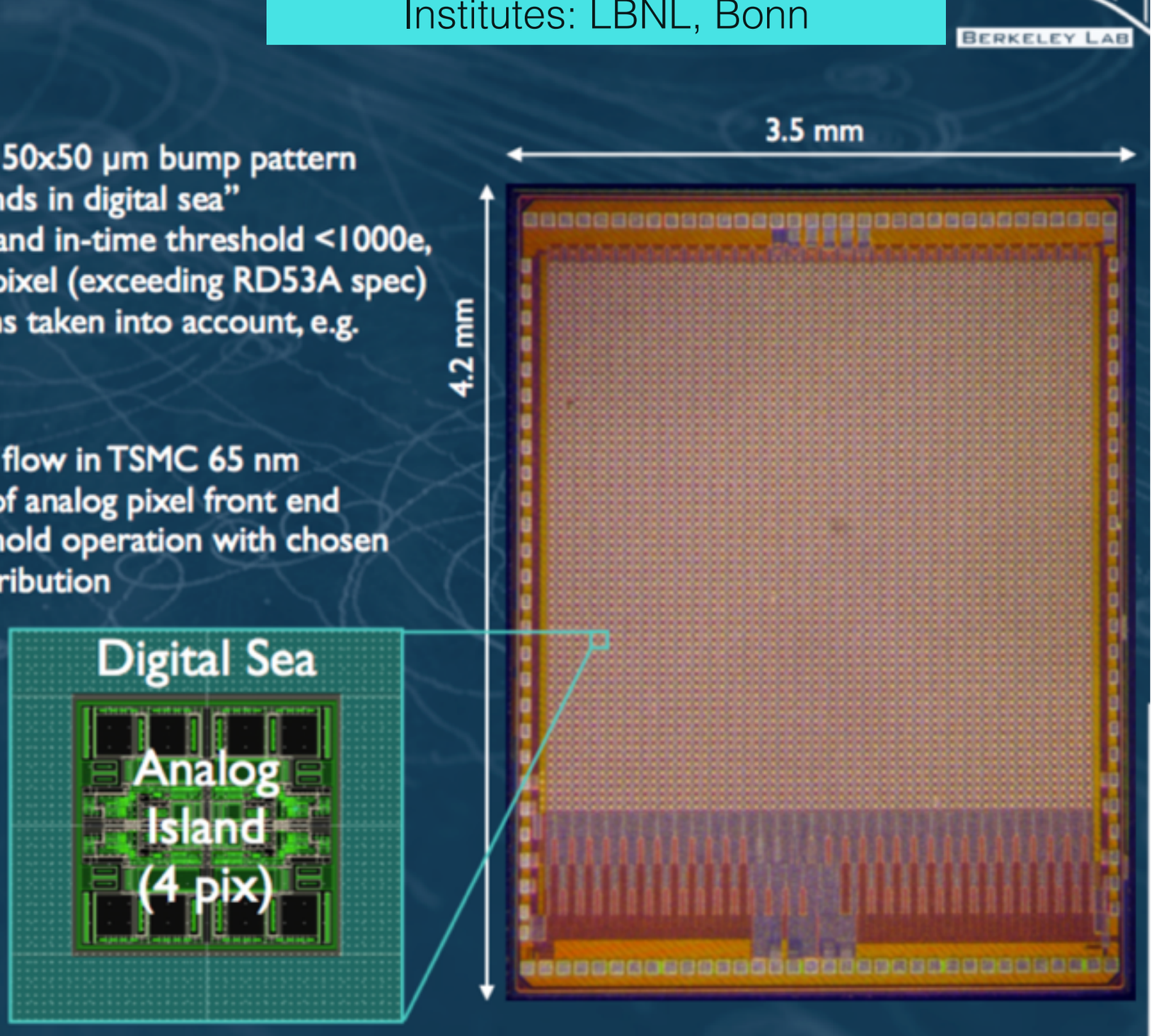
Specifications:

- TSMC 65 nm design
- 64x64 pixel matrix with 50x50 µm bump pattern
- Designed as "analog islands in digital sea"
- Stable threshold <500e and in-time threshold <1000e, while consuming <4µA/pixel (exceeding RD53A spec)
- Large chip considerations taken into account, e.g. power distribution

Goals:

- Exercise and test design flow in TSMC 65 nm
- Test prototype version of analog pixel front end
- Demonstrate low threshold operation with chosen isolation and power distribution
- Use for sensor testing
- Test radiation hardness

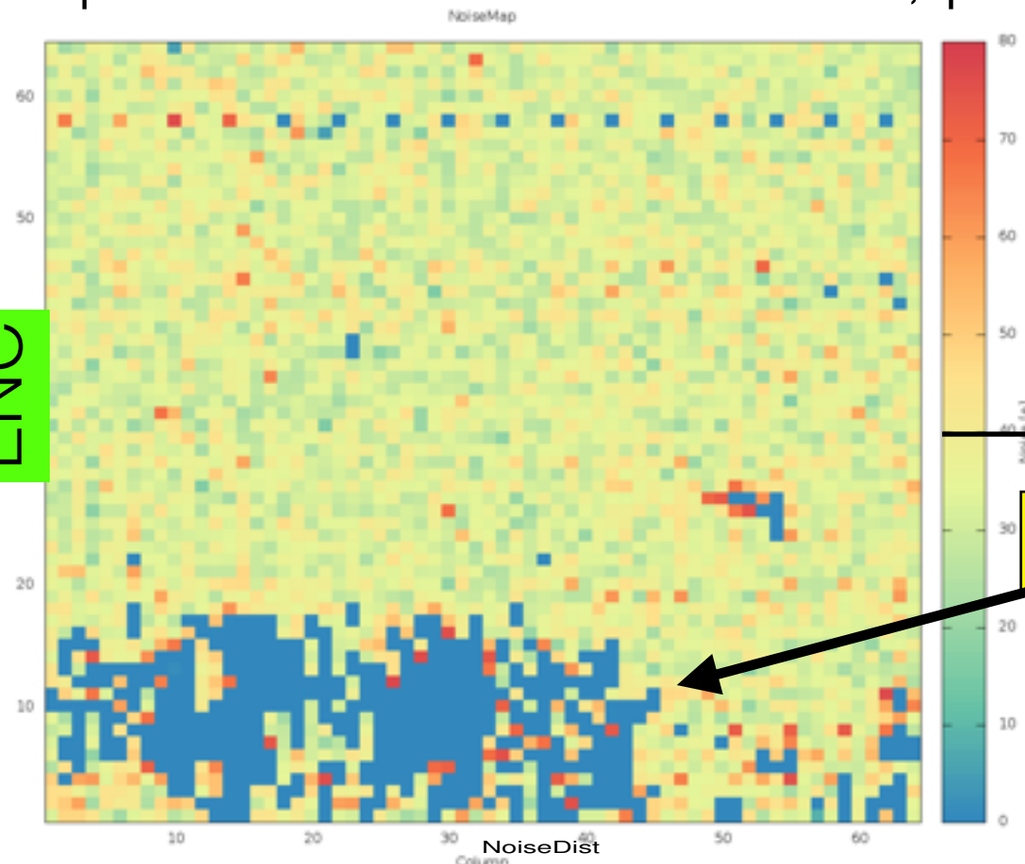
Received chip 21-Dec-2015



FE65P2 + planar sensor

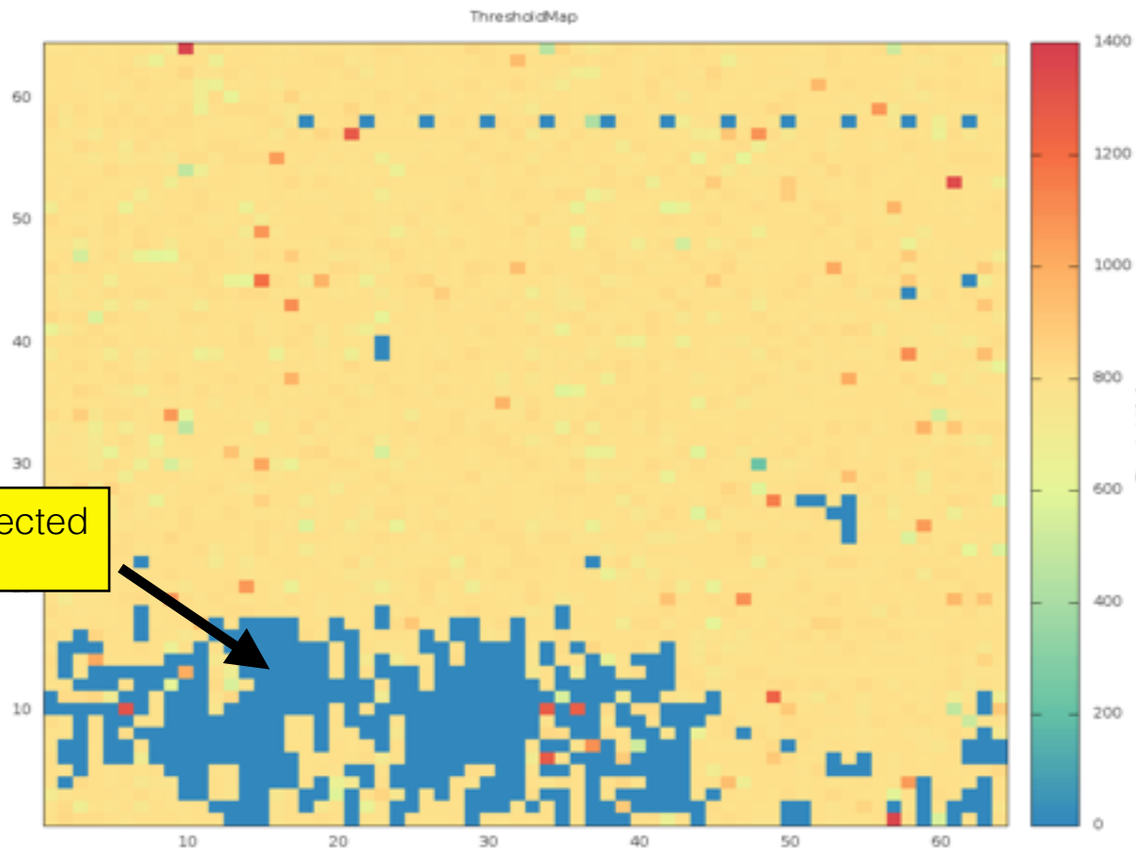
planar 300um thick sensor, partially depleted

ENC

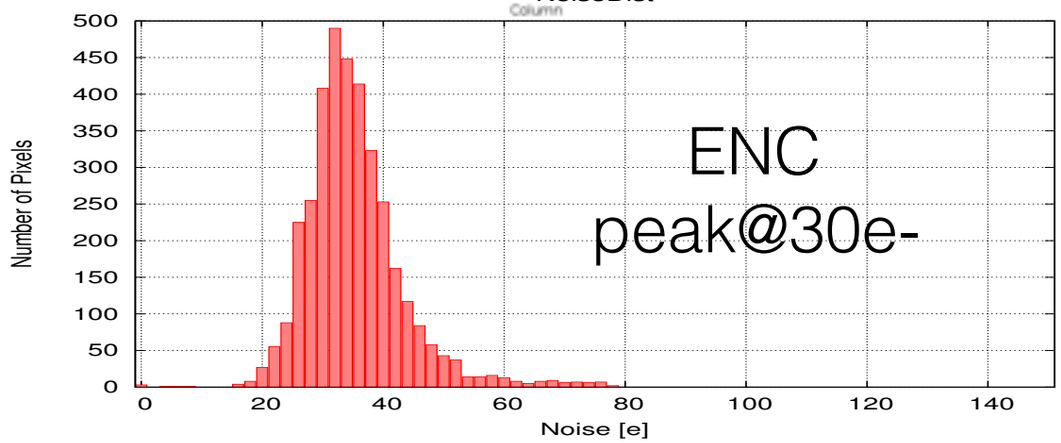


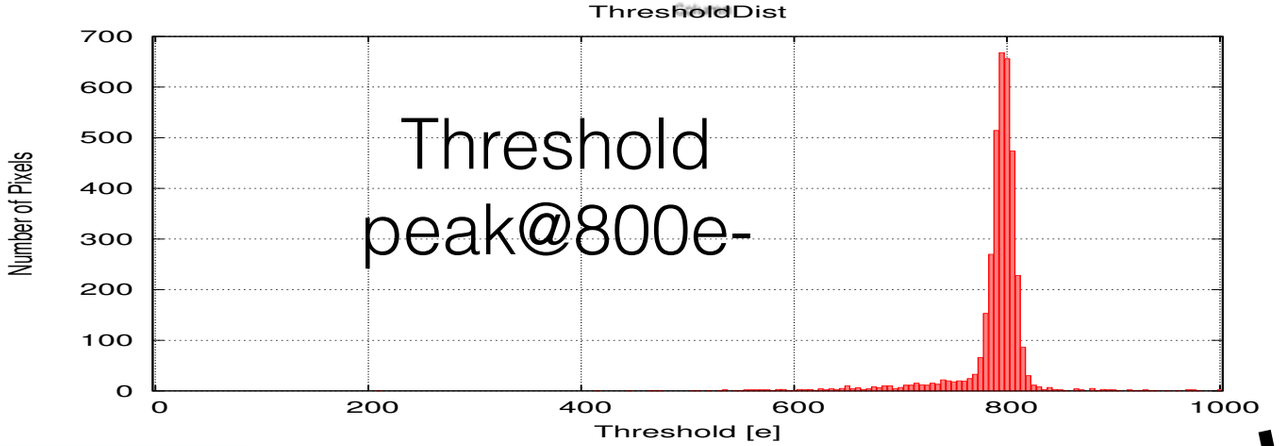
40e-

undisconnected bumps



Abs. Threshold



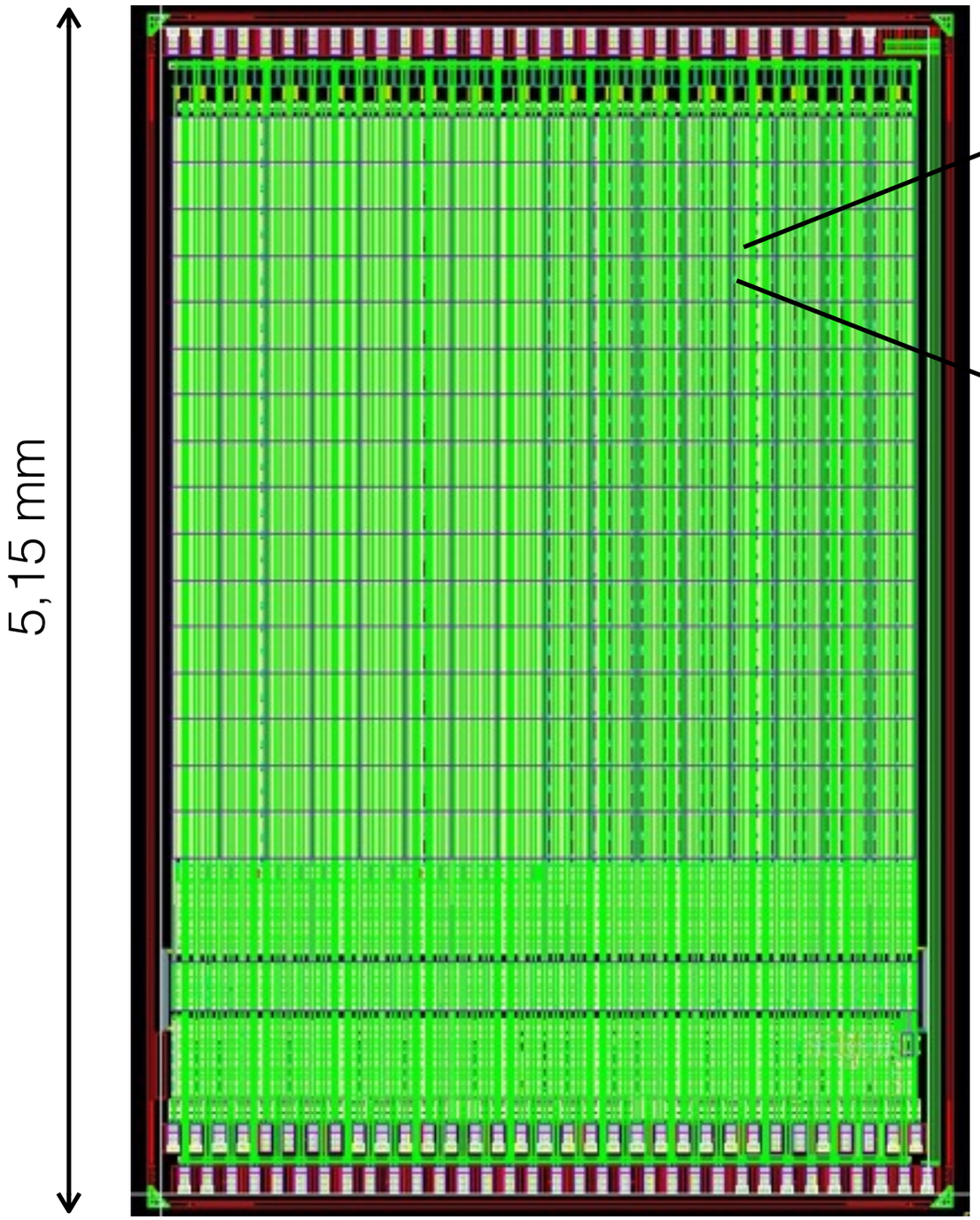


Excellent noise and threshold performance

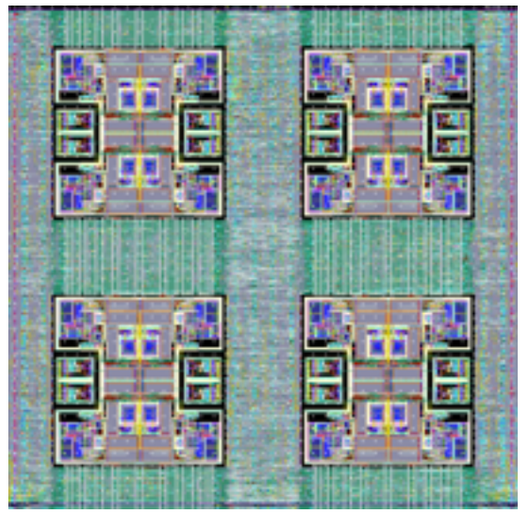
Preliminary results !

CHIPIX65 demonstrator

CHIPIX65: 2013 CALL project INFN - CSN5
Web-site: http://chipix65.to.infn.it



(2x2) Analog Islands
on (4x4) pixel region digital architecture



submitted on
5-July-2016

64x64 pixel matrix - 50x50 um²

HL_HLC flux rates: 3 GHz/cm²
Trigger latency : 12,5 us
Low power consumption
5-bit ToT signal digitisation
In-time threshold <1200 e-
Noise ~100e- @50fF input capacitance

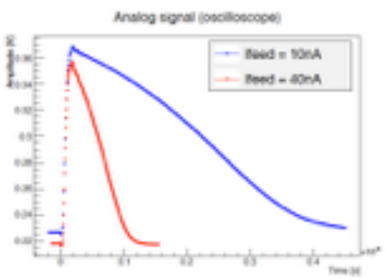
VFE & IP-block developed in RD53

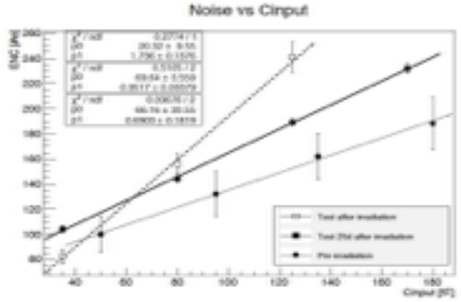
~3M of digital standard cells

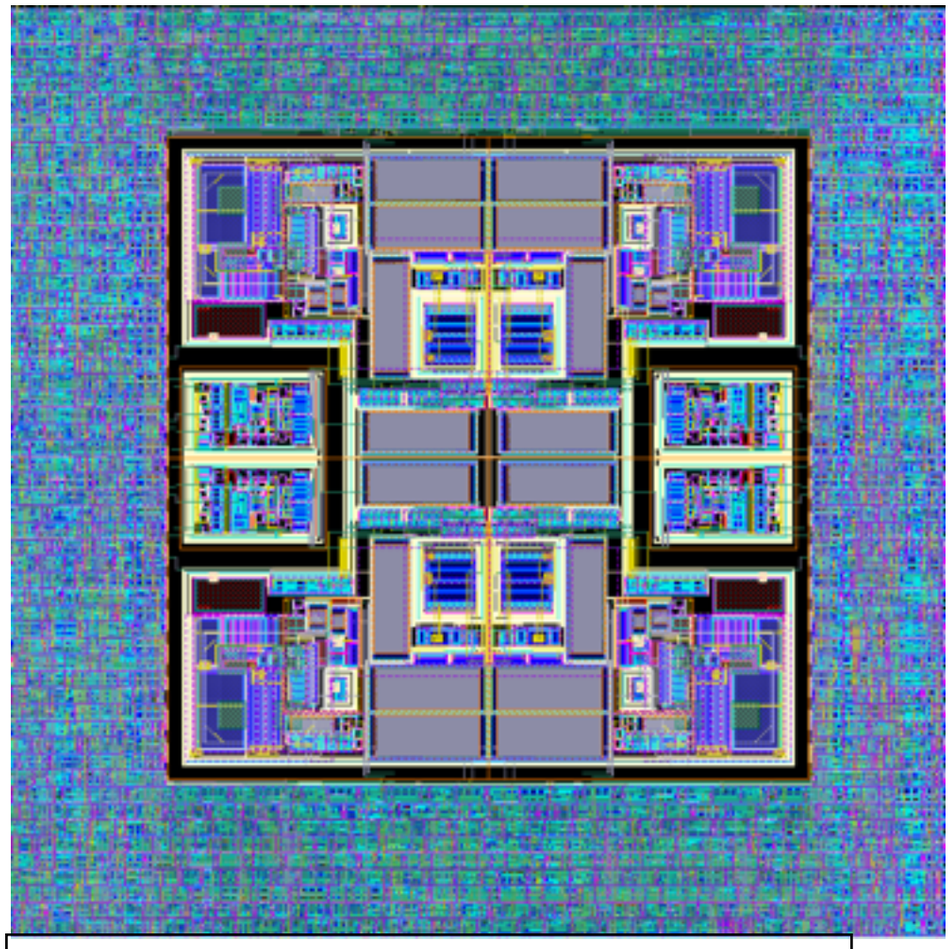
INFN institutes: To, Ba, Le, Mi, Pd, Pg, Pi, Pv

CHIPIX65 demonstrator

Analog Very Front End:
- (32x64) synchronous design
- (32x64) asynchronous design
- up to 50nA leakage current/pixe
- 5bit signal: ToT measurement in <150ns@Q=10ke-



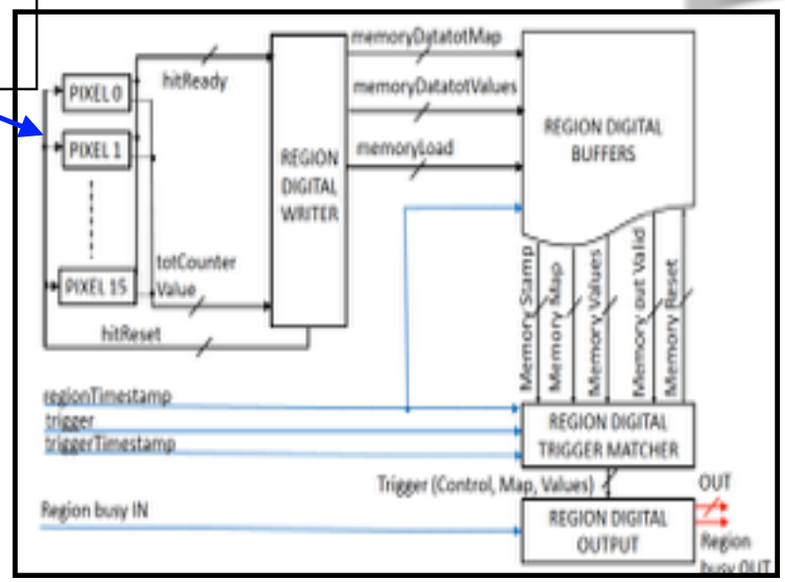




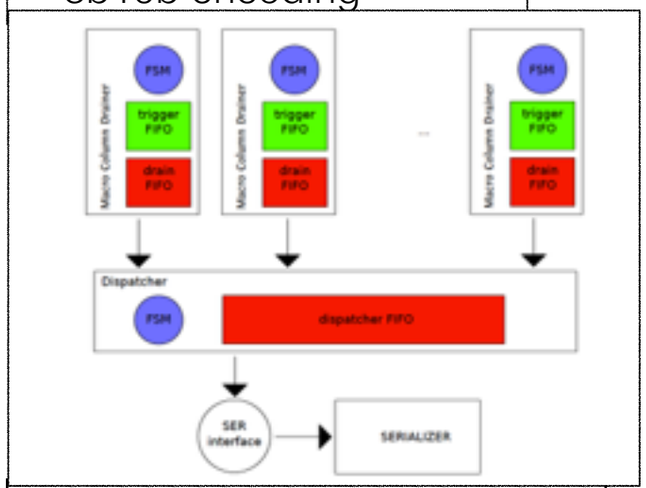
2x2 analog island on digital see

Digital architecture:
- Organised into (4x4) Pixel Region
- central latency buffer
- inefficiency<0.1%

Running mode:
- Triggered / triggerless / debug
- BinaryOnly/5-bit ToT
- EOC scan-chain

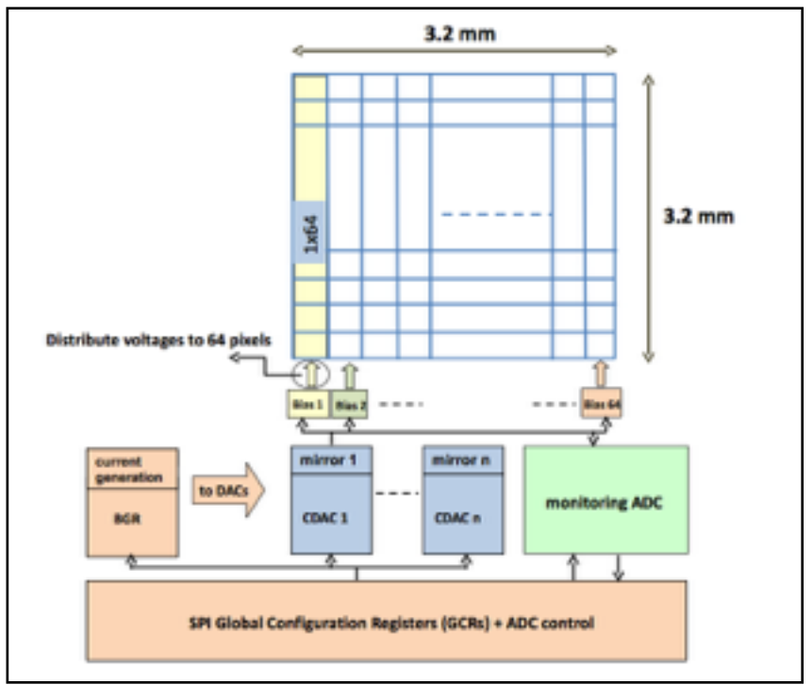


Input / Output:
- Fully digital
- Configuration via SPI
- serial readout@320 MHz
- 8b10b encoding



IP-Blocks:
- 16 DAC (10bit current steering)
- 1 BandGap
- 1 monitoring ADC (12bit)
- 8 x sLVS-RX
- 2 x sLVS-TX
- 1 Serializer

Bias and monitoring

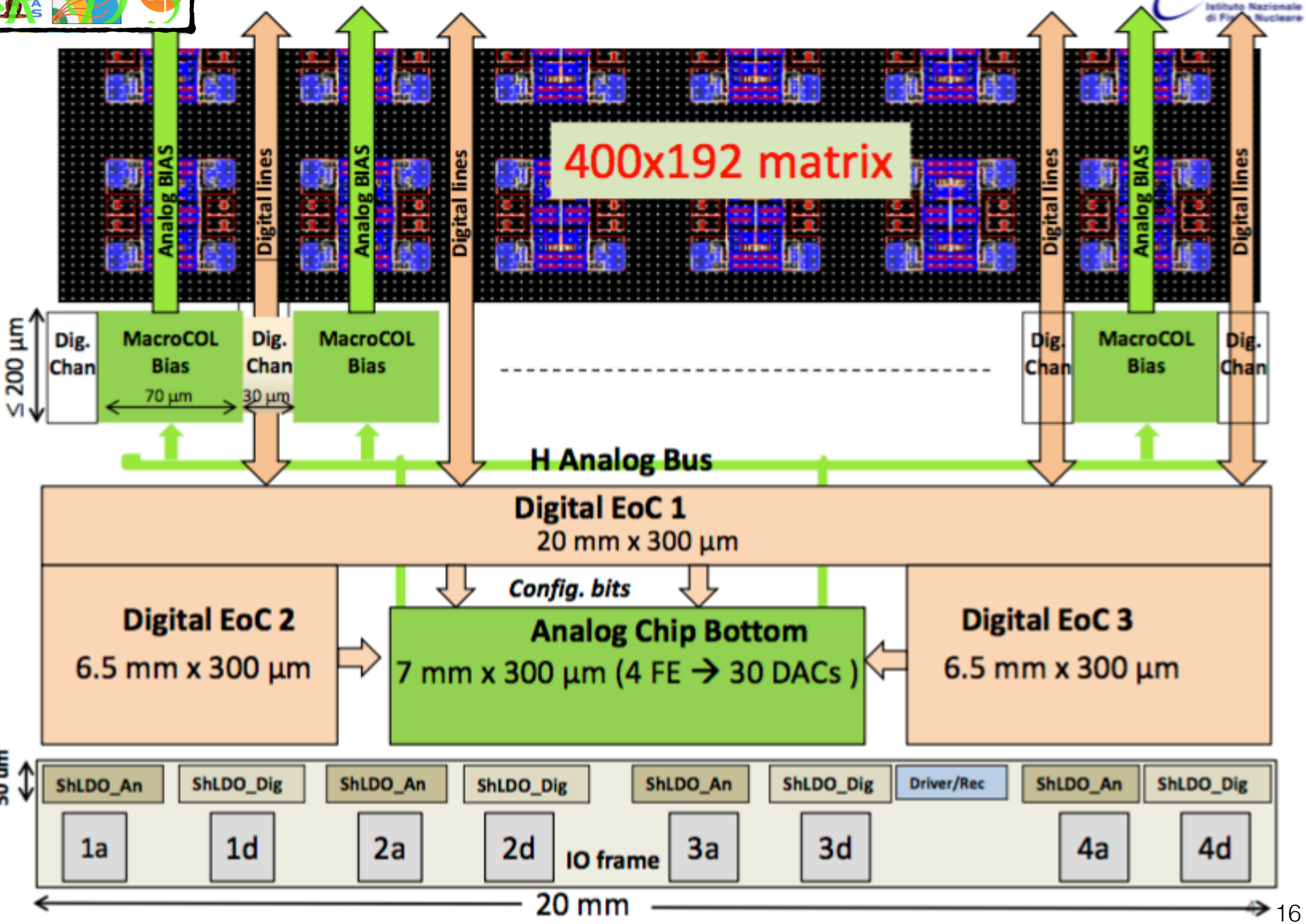


More on E.Monteil poster

RD53A
Full size prototype

- (400 x 192) pixels
- 2 cm^2

RD53A floorplan



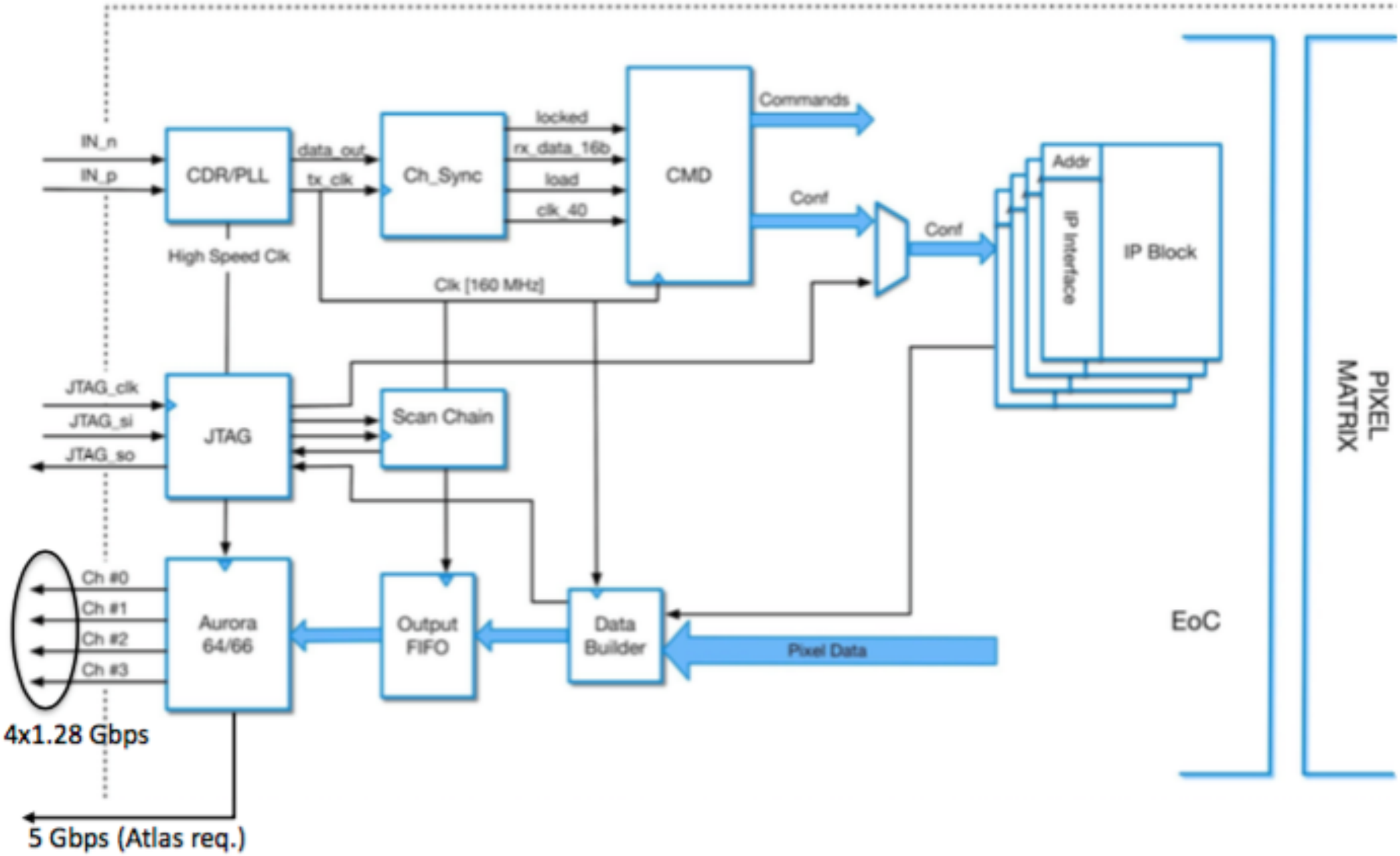
Analog Chip Bottom

- Macroblock containing all analog IPs
- To be assembled "manually" in analog environment (Virtuoso) and simulated with analog and mixed-signal simulator
- Based on IPs: all prototyped. Most of them already tested and irradiated, for few of them waiting for test results

Main blocks	Main Sub-Blocks	Comments
Monitoring Block	ADC, Bandgap, Buffer	High level simulation started
Current generator	Bandgap	Provides T and Vdd independent I reference for Bias DACs
Bias Dacs	10 bit current-DAC (35)	Bias the analog FE and IPs
Calibration Block	12 bit voltage-DAC (2), Pulser, Buffer	Injection pulse generation
POR		Power On Reset
CdrSer	PLL, CDR, SerDes	PLL, Clock Data Recovery, SerDes
Sensors	TempSens, RadSens	

In case of different developments of the same IP, the final choice at the end of July based upon test result

Digital End of Column



Pixel Array Logic

Optimization trade-off

- **area** → current PR is **rather full**
- **low and "constant" power** → continuous study and optimization ongoing
- **radiation tolerance** up to 500Mrad → first check to estimate timing problems, initial solution
- **SEU tolerance**
  → SEU injection to be integrated in the simulation framework
- **low hit inefficiency** (dead time and buffers losses)
- **analog losses** determined by TOT conversion **already close (or >!) to 1%**
- would ideally **need more buffer locations** for lower digital losses → need for area

Space is critical: to go above 4-bit ToT and 12.5 usec latency (L1-only) seems to be not trivial limit for 3GHz/cm^2 pixel rate, if a 50x50 um^2 is realised in CMOS 65nm, with rad-hard options.

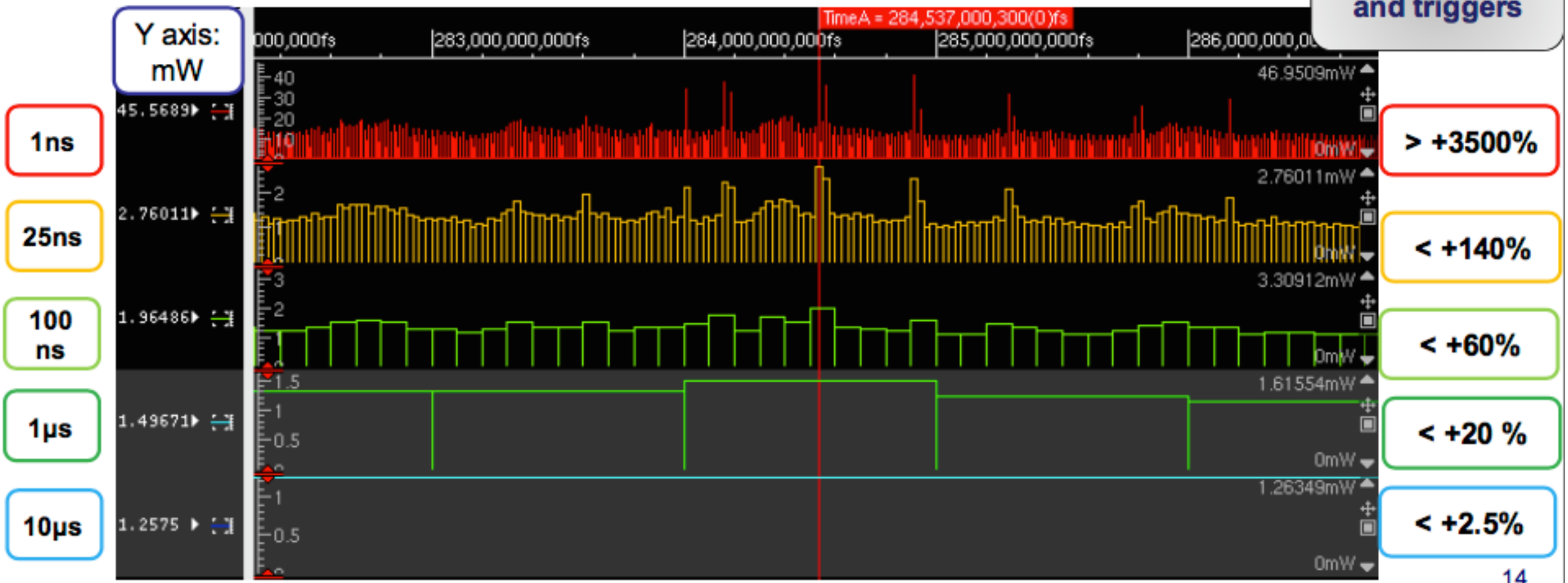
Work on-going => Two digital architectures under analysis (FE65P2 and CHIPIX65)

Powering Profile

Power profiling

- **Time resolution: 1ns, 25ns, 100ns, 1 µs, 10 µs** (zoom on shorter simulation window)
- delay corner considered: RD53A typ
- activity conditions: **with hits** (3 GHz/cm^2 hit rate) **and triggers** (1 MHz rate)

Wrap-up: hits and triggers



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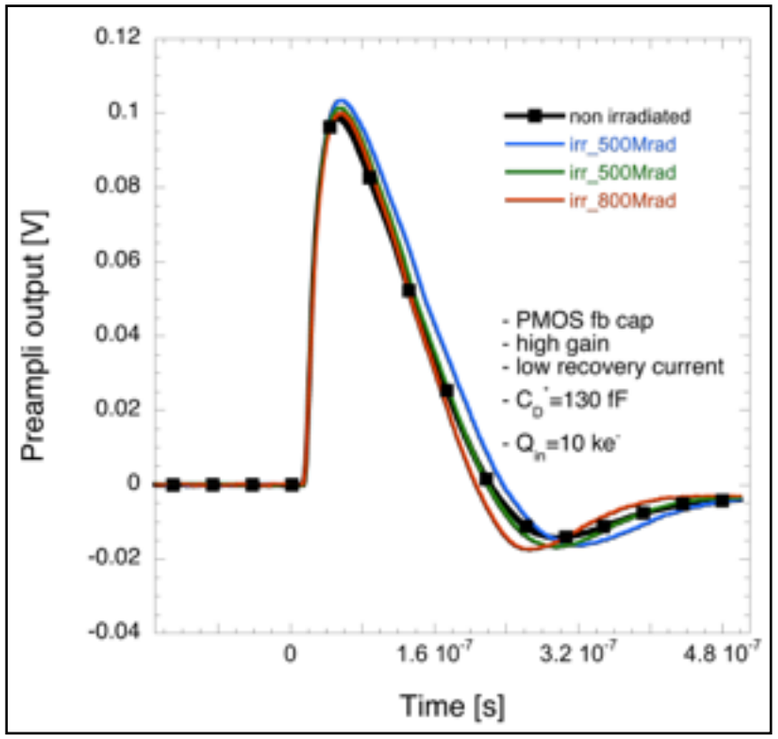
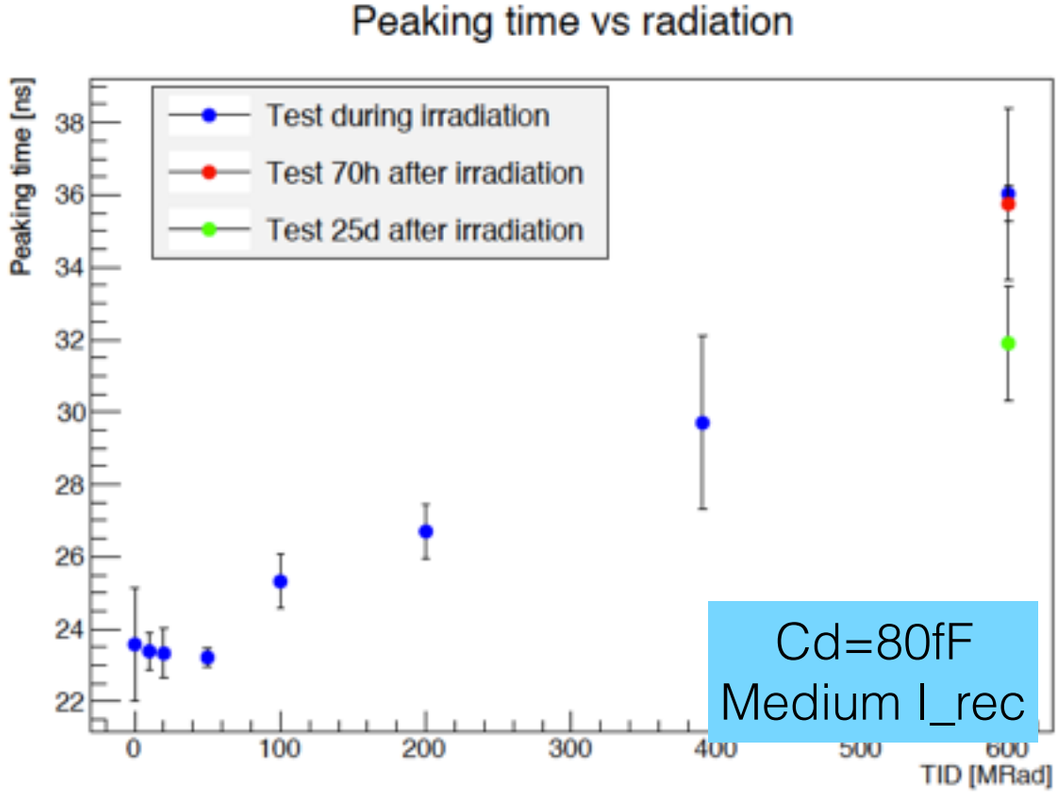
Very important for Serial Powering

Radiation Effects

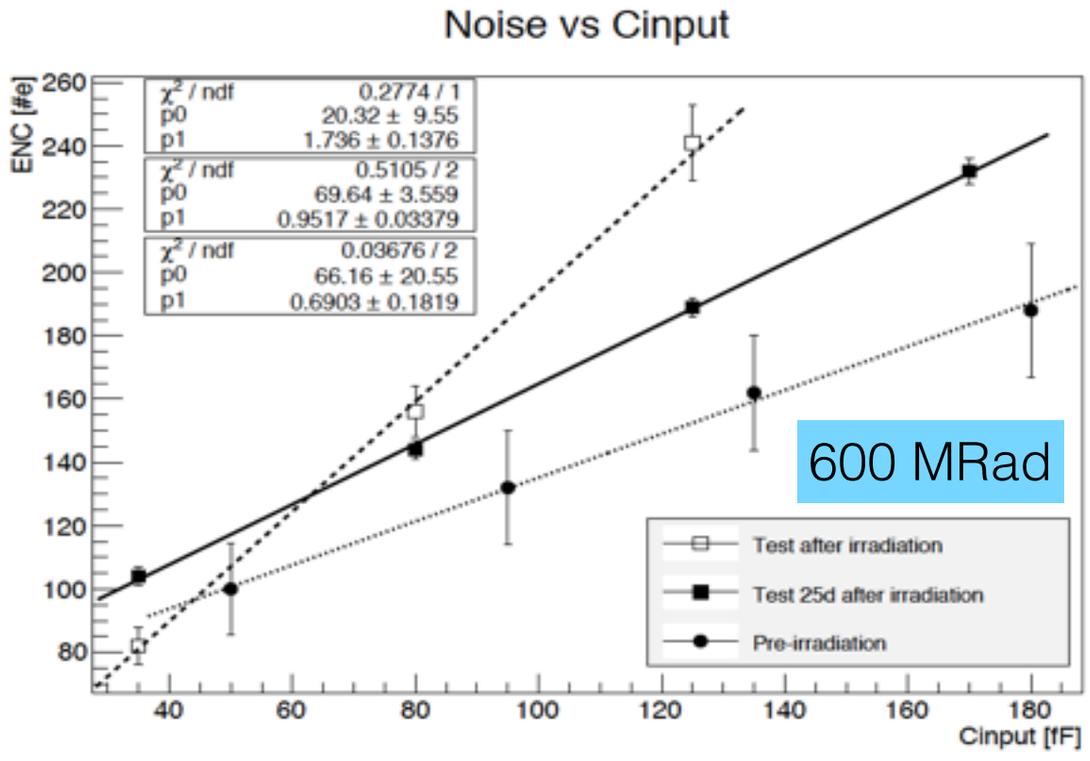
TID: Analog VFE





- No major worry: **two out of four analog-architectures tested under radiation** and no serious problem see

- Gain decrease of ~5%
- Slower signal but looks ok
- 10-20% increase of noise



Digital library radiation test chip DRAD

Motivation

Radiation damage is severe in short and narrow channel. Most of the standard cells in digital libraries use minimum length transistor (L=60 nm) and small width (W~200 nm)

- What will be the effective performance degradation of *digital circuits* at > 100 Mrad?
- Do we need modified libraries for high rad and/or high speed?
- High density digital is critical for high hit rates and long trigger latency

DRAD: joint effort between RD53, MPA and LPGBT (CERN, LBNL, NIKHEF)

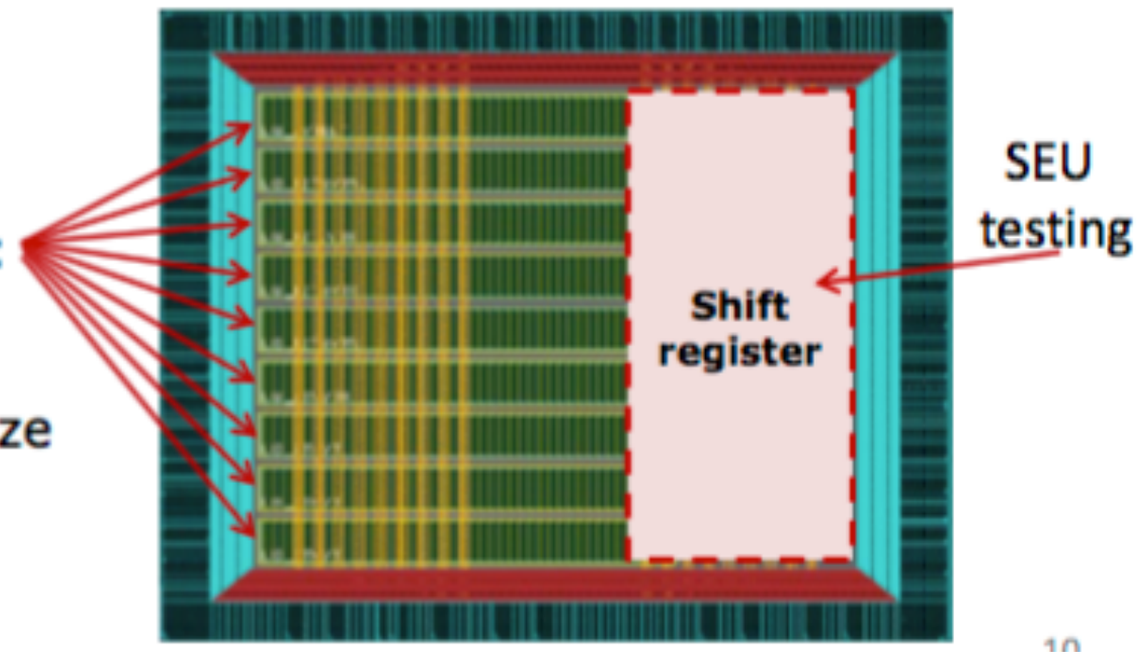
Goal: measure the speed degradation and power consumption of a subset of the digital library from the foundry and of modified libraries with larger transistor (which should reduce performance degradation)

Submitted: 03/2016 (Europractice mini@sic)

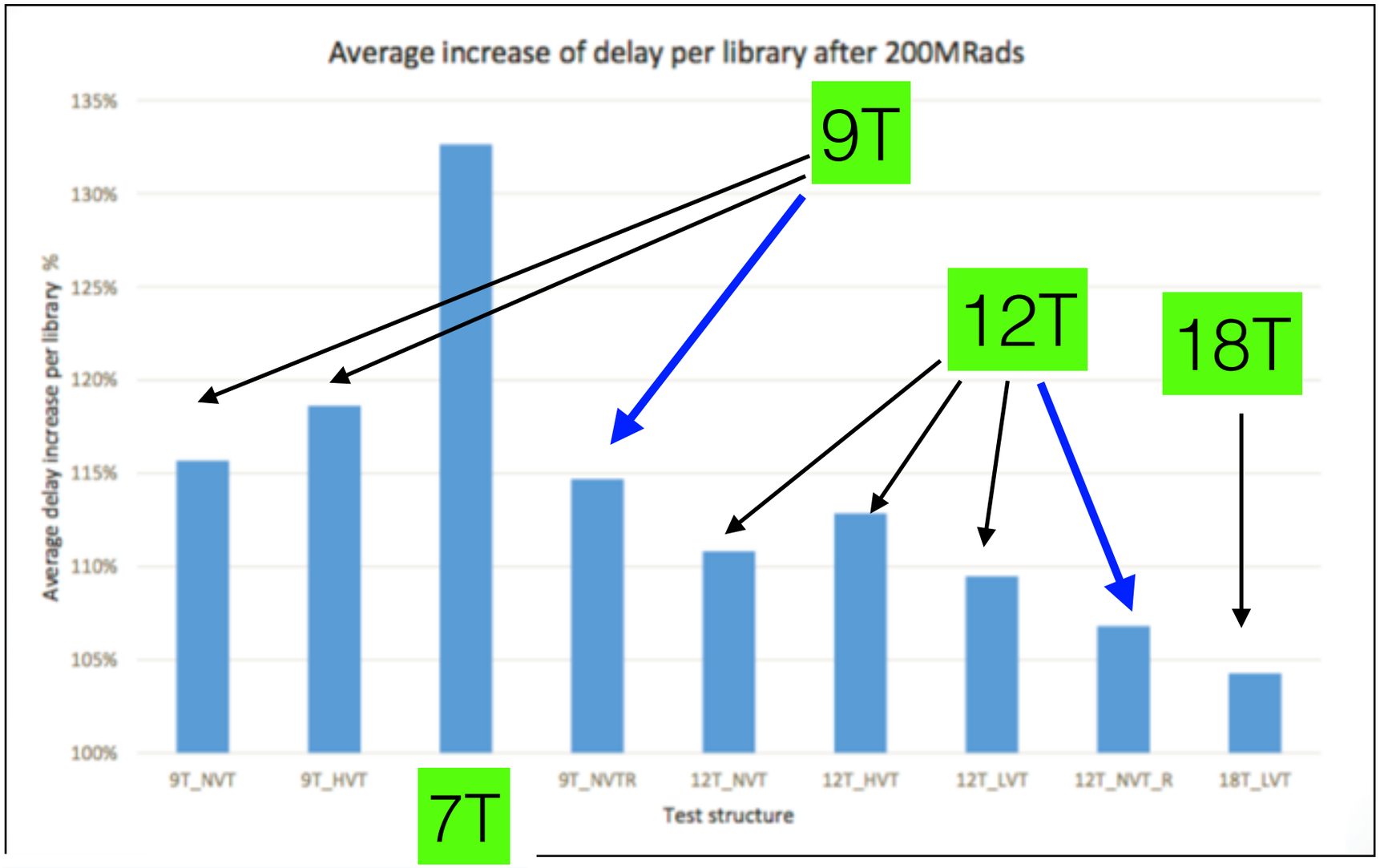
Tests ongoing @ CERN

Schedule and deliverables
- Rad test results → Sept.
- Library → Oct.

9 libraries: Different V_T flavours, transistor size and shape



DRAD : first results



NEXT Steps:

- Repeat tests with cooling:
  - 200 MRads with cooling.
  - 1000 MRads with cooling.
- Radiation campaign up to 500MRads.
- Continue with the current annealing testing and annealing at 100˚C.

CELL HEIGHT

7 Track: 1.4 uM

9 Track: 1.8 uM

12 Track: 2.4 uM

18 Track: 3.6 uM

- 9T is the digital library for Pixel-Matrix (7T cannot be used)
- so far results in agreement with simulation models derived from single MOS radiation characterisation results

Conclusions

- CMOS 65nm choice is obligatory for Pixel-ROC at HL-LHC given the particle flux, the L1 trigger latency and rate

- Major progress during the last year
  - VFE, most of IP-block developed
  - Small Demonstrators
  - RD53A started for real

- Important points for RD53A are:
  - ANALOG: dead-time of analog
  - Area / Power for digital in pixel matrix (keeping up efficiency)
  - Serial Powering
  - Digital Radiation Hardness

- Lot to be done but submission of RD53A for end of March 2017 is a solid milestone

- Lot will be learnt from RD53A - stay posted !