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SI LAB
Silizium Labor Bonn

Overview and perspectives of HR&HV CMOS

Tomasz Hemperek

Overview

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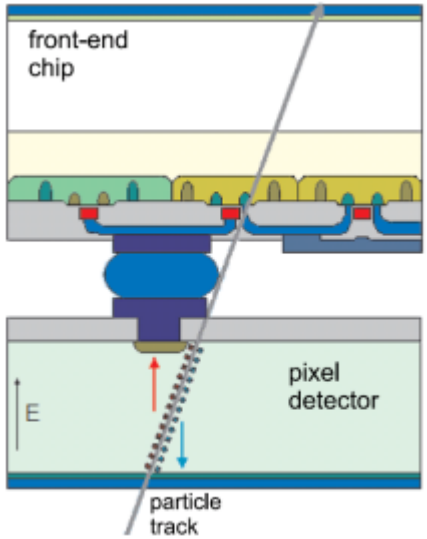
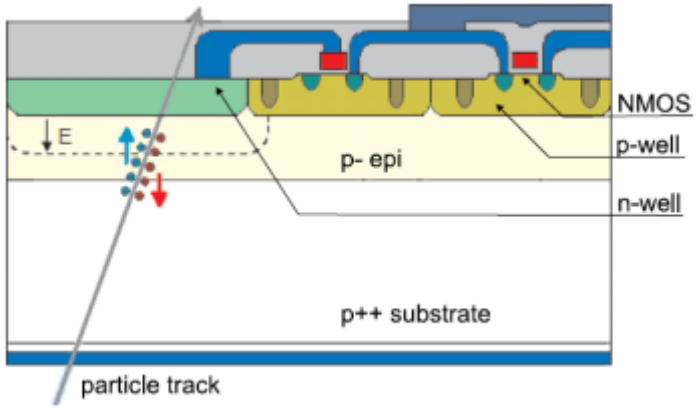
- Introduction
- Sensor design parameters by example (NIEL)
- Implementations and measurements

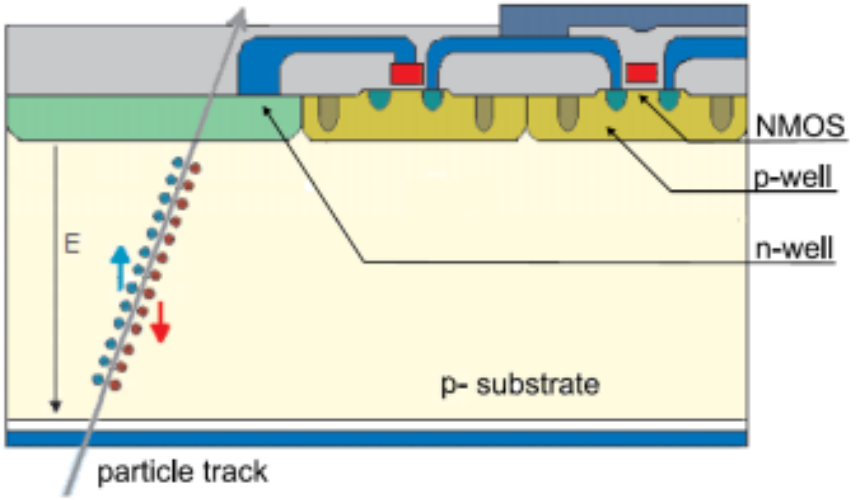
Hybrid Pixel Detectors



Monolithic Pixels

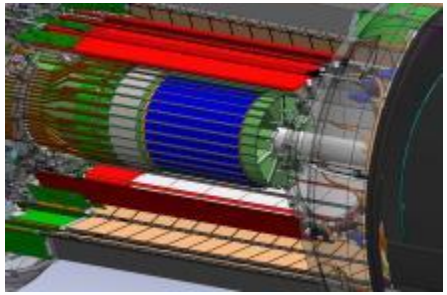


Depleted Monolithic Pixels

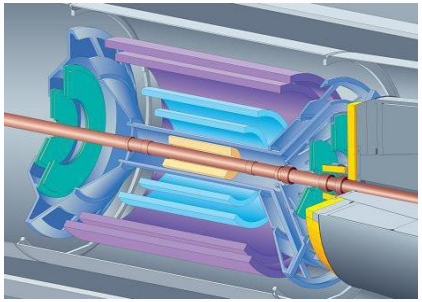


Introduction

STAR

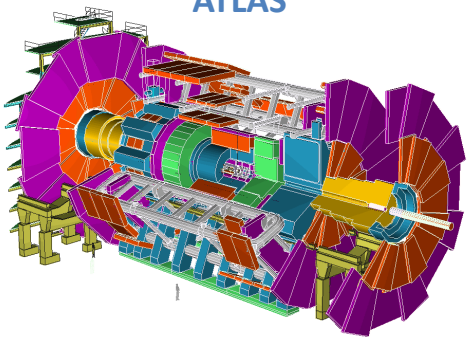


ALICE-LHC



ILC

ATLAS



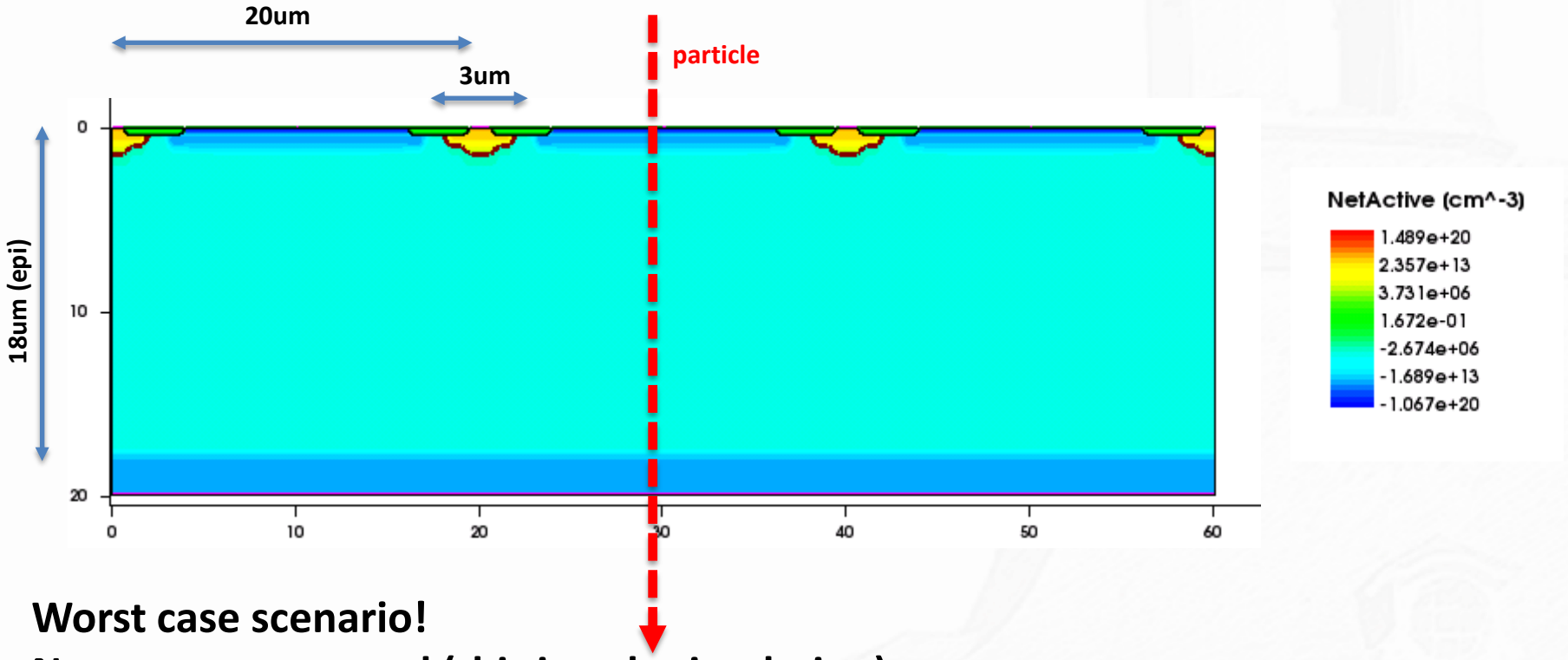
Requirements for inner pixel layers

	STAR	ALICE-LHC	ILC	ATLAS-LHC	ATLAS-HL-LHC
Timing [ns]	200 000	20 000	350	**25**	**25**
Particle Rate [kHz/mm^2]	100	10	250	1000	10000
Fluence [n_{eq}/cm^2]	> 10^{11}	> 10^{13}	10^{12}	**2x10^{15}**	**2x10^{16}**
Ion. Dose [Mrad]	> 0.3	0.7	0.4	**80**	**>500**

Monolithic CMOS ?

Sensor Design Paramters

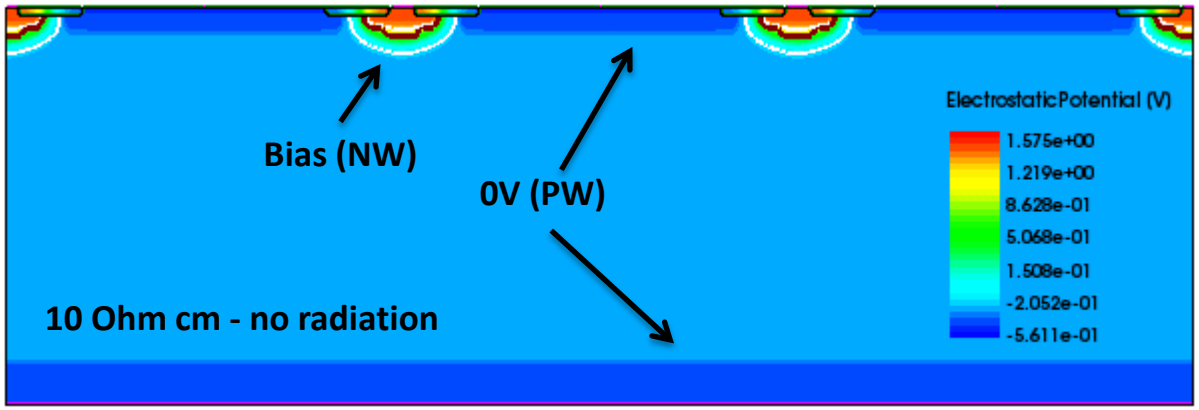
- Substrate doping concentration (resistivity)
- Maximum sensor bias voltage
- Geometry (thickness, fill-factor)



- **Worst case scenario!**
- **No acceptor removal (this is only simulation)**

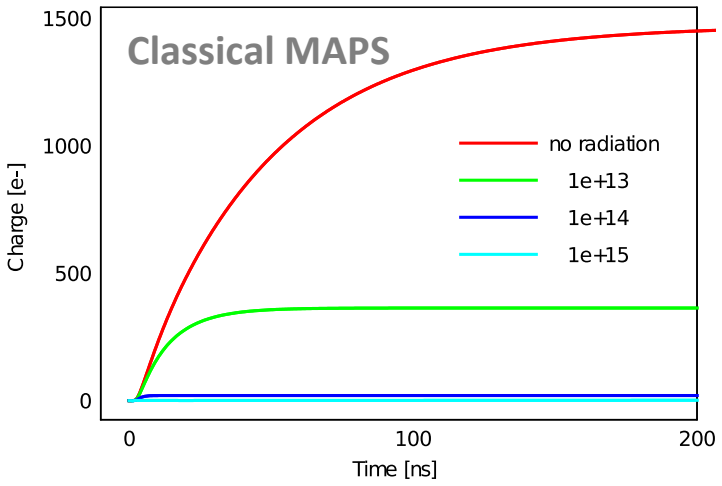
Code: https://gitlab.cern.ch/TCADExamples/ChargeCollection

Bias voltage influence

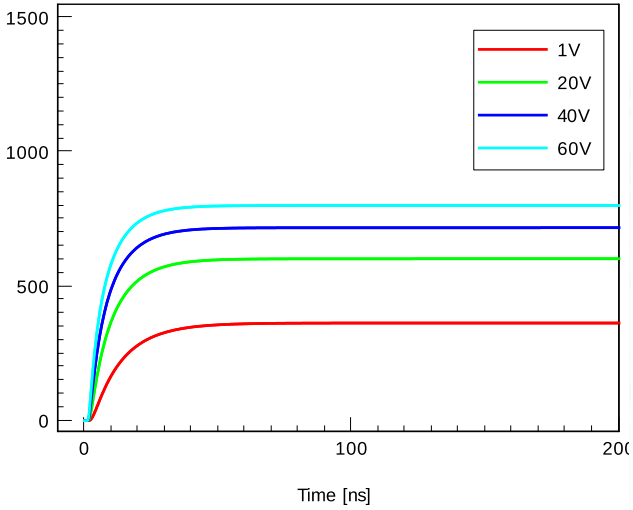


Resistivity: 10 Ohm-cm

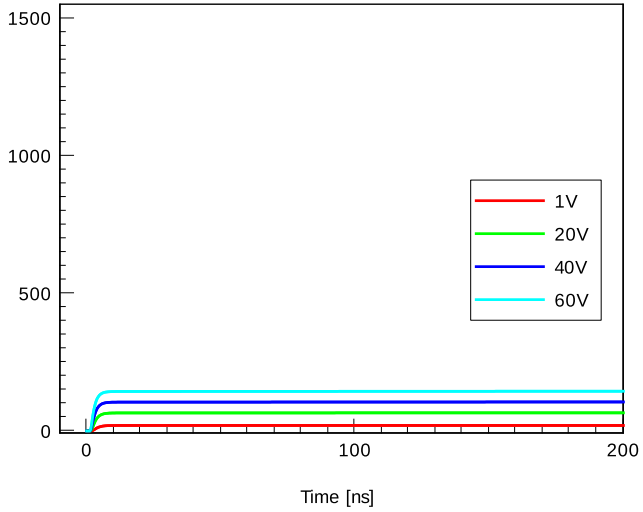
Bias @ 1V



$10^{13} n_{eq}/cm^2$



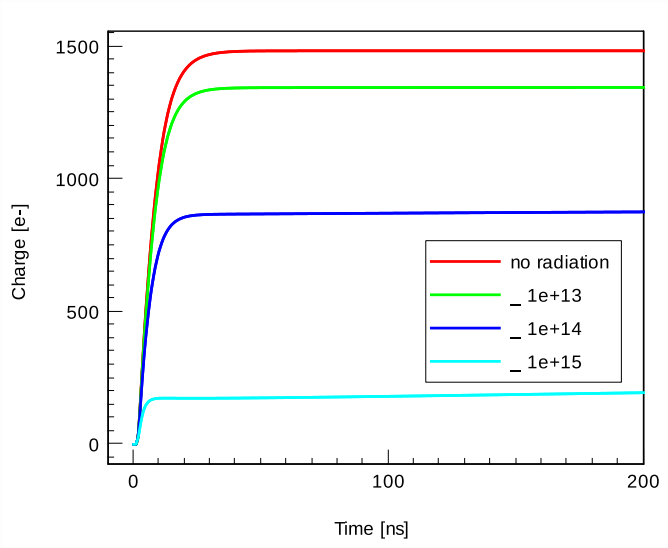
$10^{14} n_{eq}/cm^2$



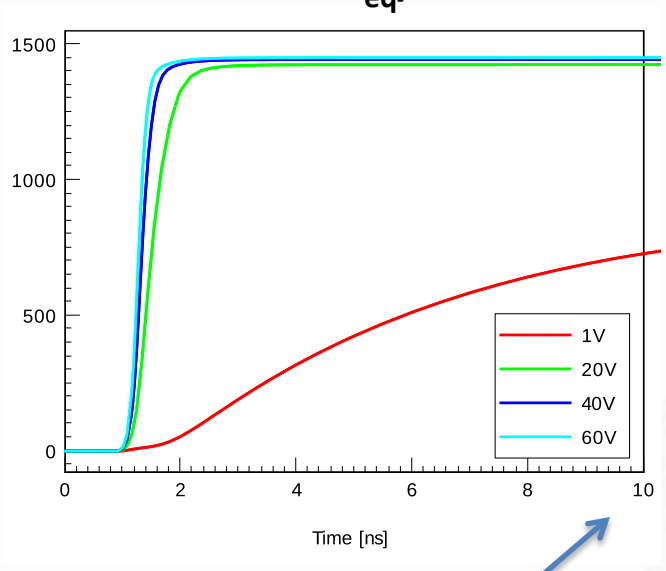
Substrate doping concentration (resistivity)

Resistivity: 2k Ohm-cm

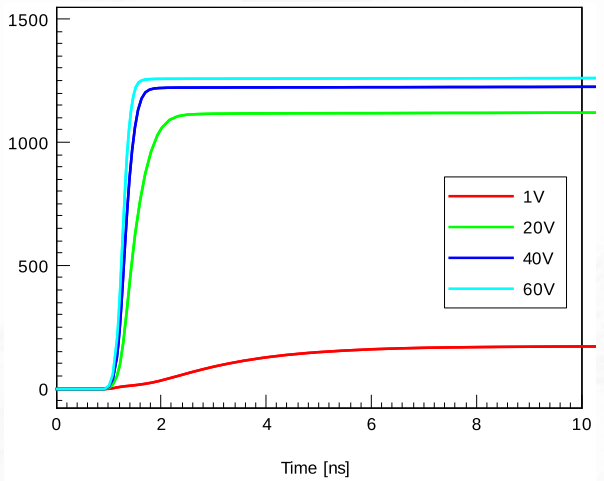
Bias @ 1V



$10^{14} n_{eq}/cm^2$



$10^{15} n_{eq}/cm^2$



scale

Substrate doping concentration (resistivity) cd.

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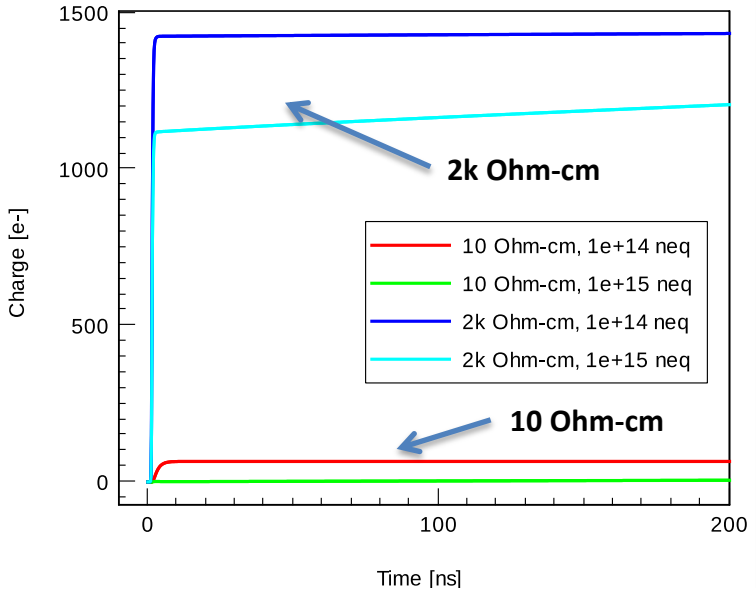
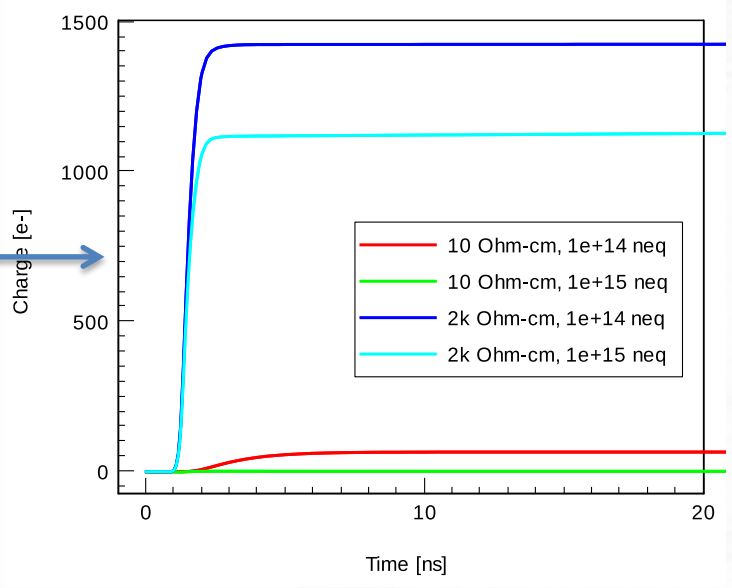
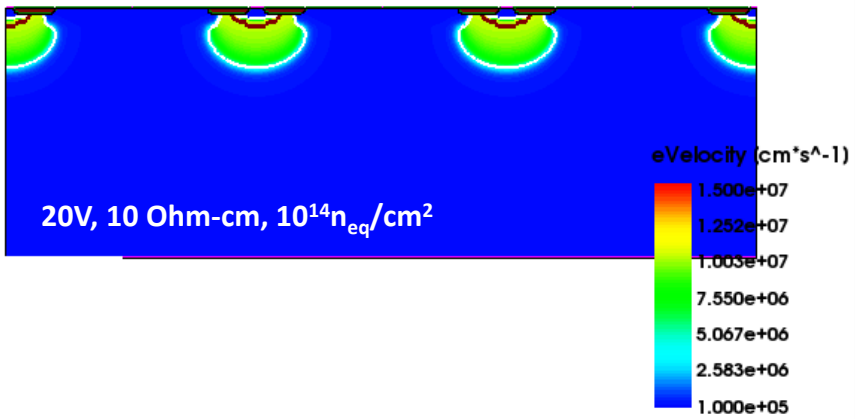
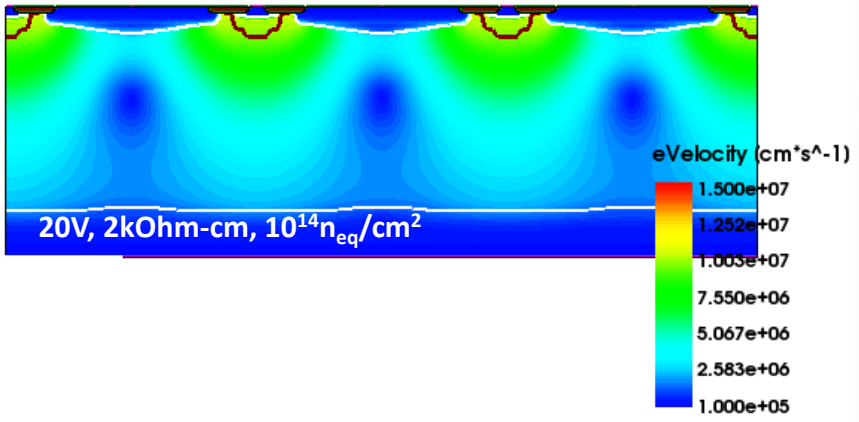
Bias @ 20V



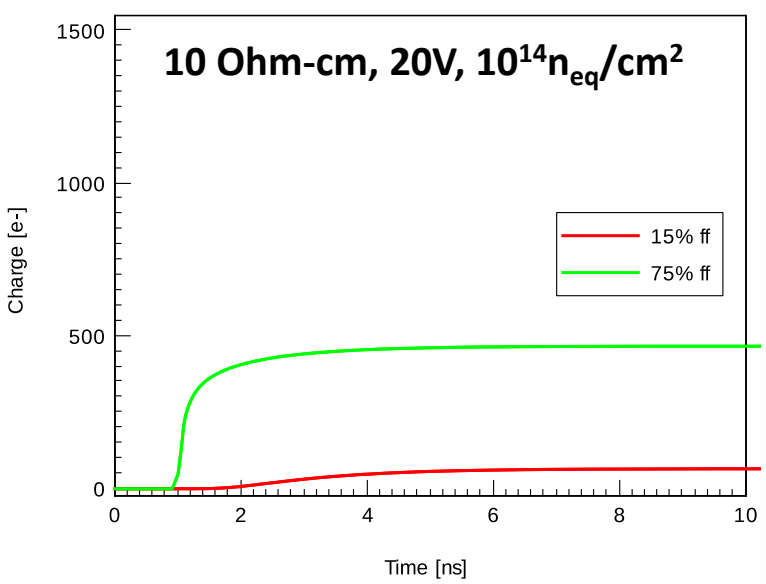
Zoom

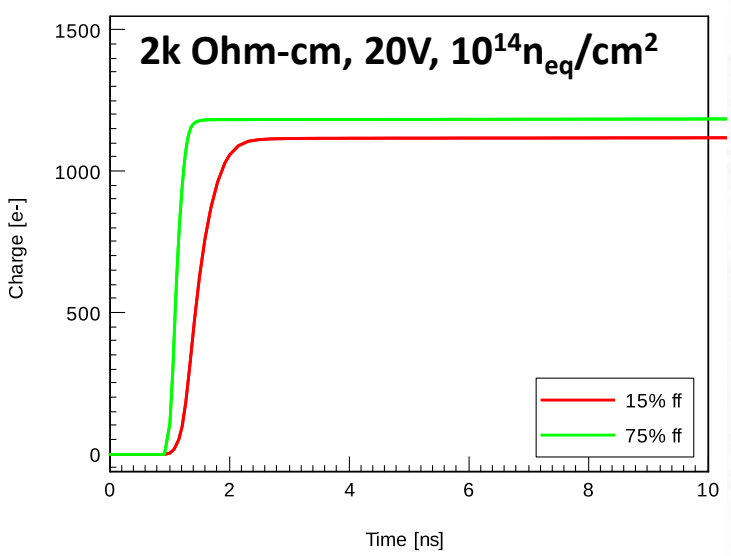


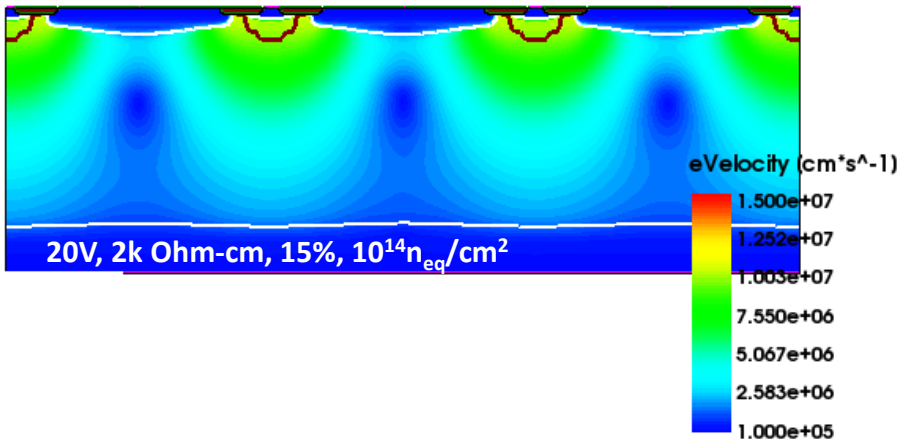


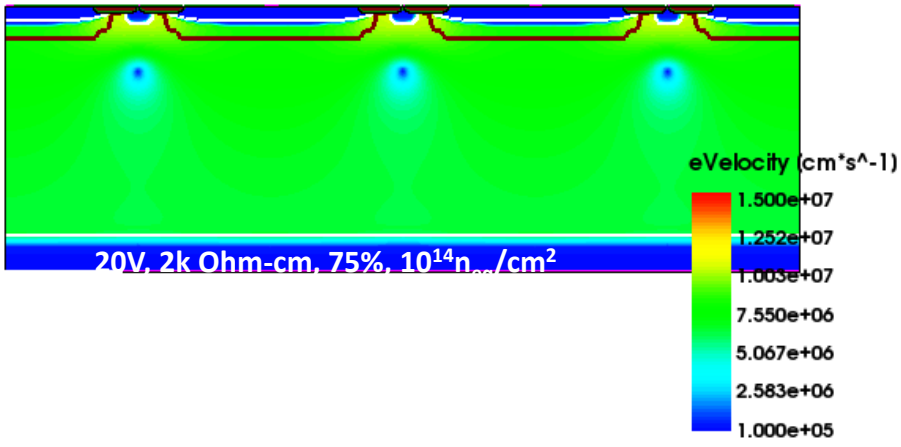


Geometry/Fill Factor









Technology Overview

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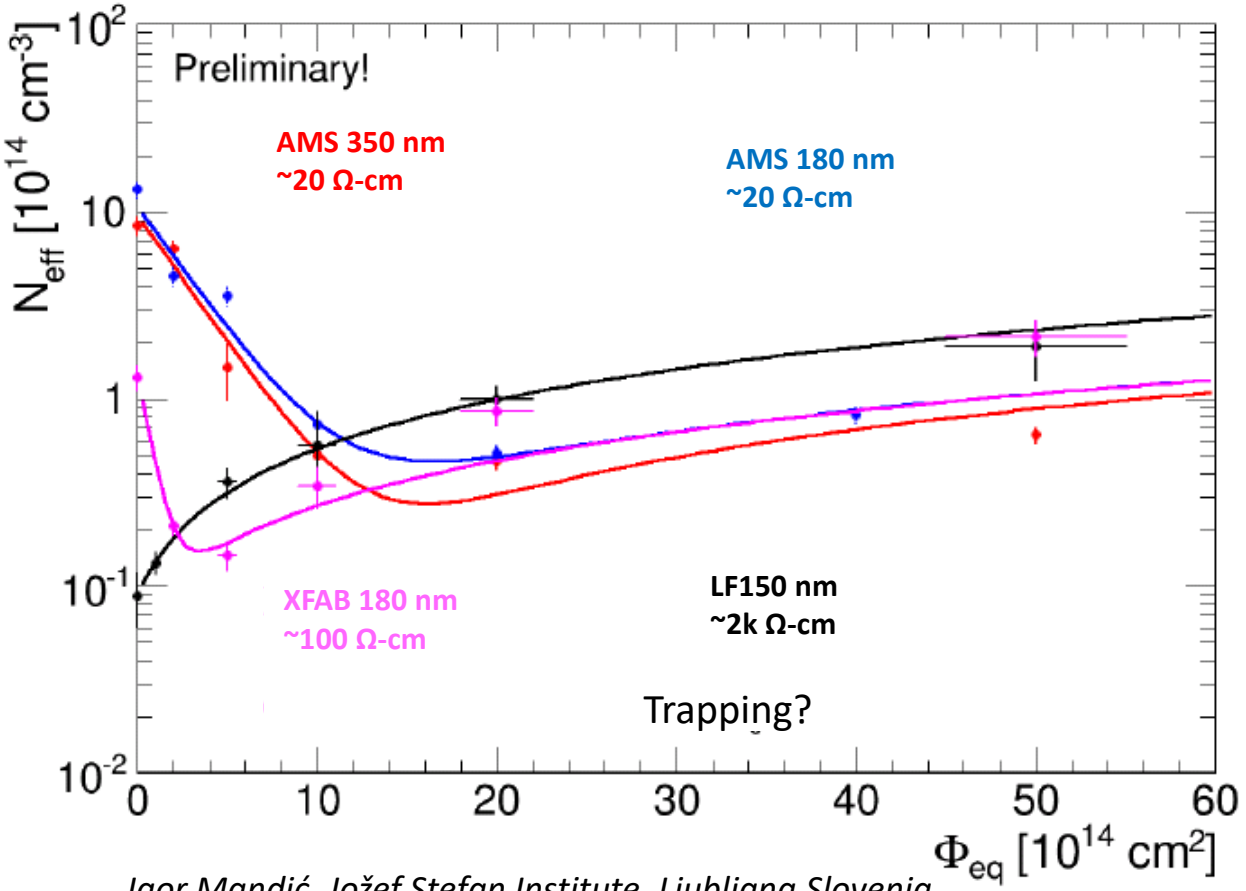
- **AMS 350 nm**
- **AMS 180 nm**
- **LFoundry 150 nm**
- Global Foundry 130 nm
- **ESPROS 150 nm**
- Toshiba 130 nm
- **TowerJazz 180 nm**
- STM 160 nm *
- IBM 130nm
- **XFAB 180 nm**
- ON Semiconductor 180 nm

*see: S. Hitesh [P]

Sensor performance

Substrate Properties – TCT



Igor Mandić, Jožef Stefan Institute, Ljubljana Slovenia
11th "Trento" Workshop, February, Paris, 2016

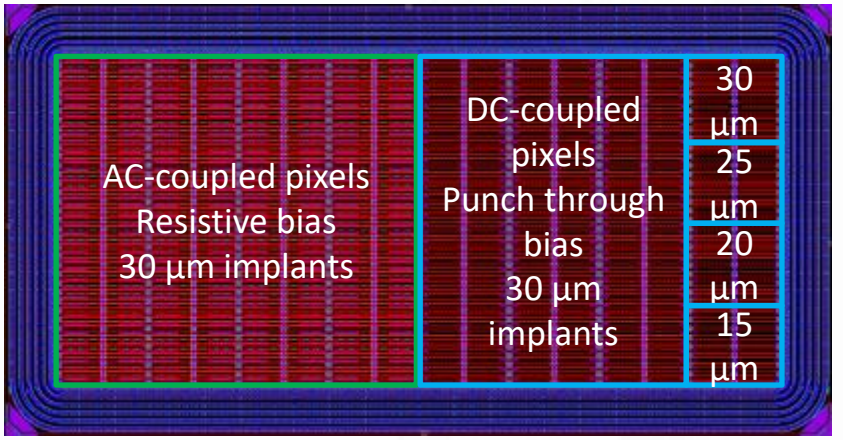
After 10^{15} n_{eq} all substrate materials behave similar

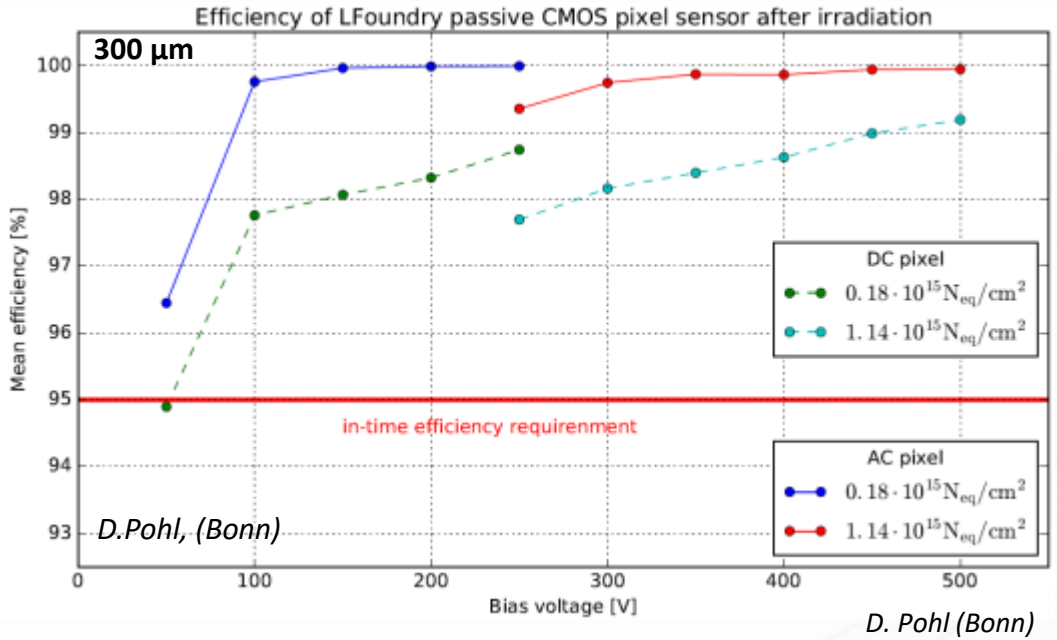
Low resistivity material device performance biggest challenge is at ~10^{14} n_{eq}

See: Ivan Vila, "Application of …"

Passive LFCMOS sensor prototype

- LFoundry 150 nm CMOS technology
- 2 kΩ-cm p-type bulk, 8“
- 100/300 µm thick, backside processed
- Bump bonded to the ATLAS FE-I4
- Pixel size: 50 µm x 250 µm
- Matrix size: 16 x 36 pixels (1.8 mm x 4 mm)
- Bonn + MPI





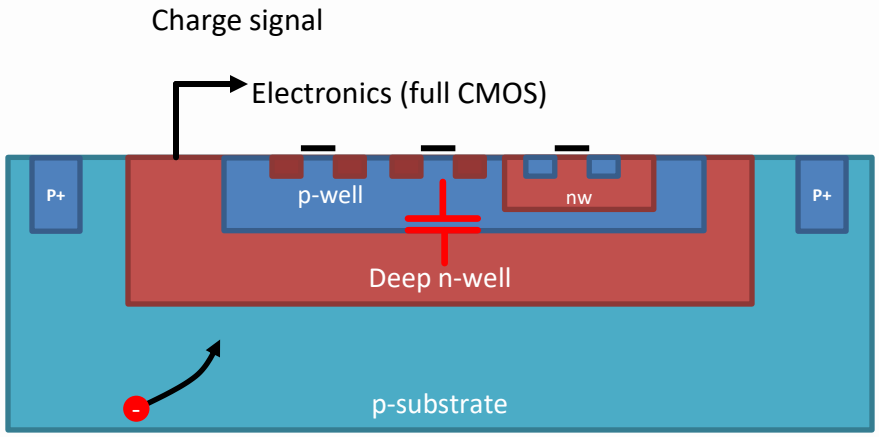
D. Pohl (Bonn)

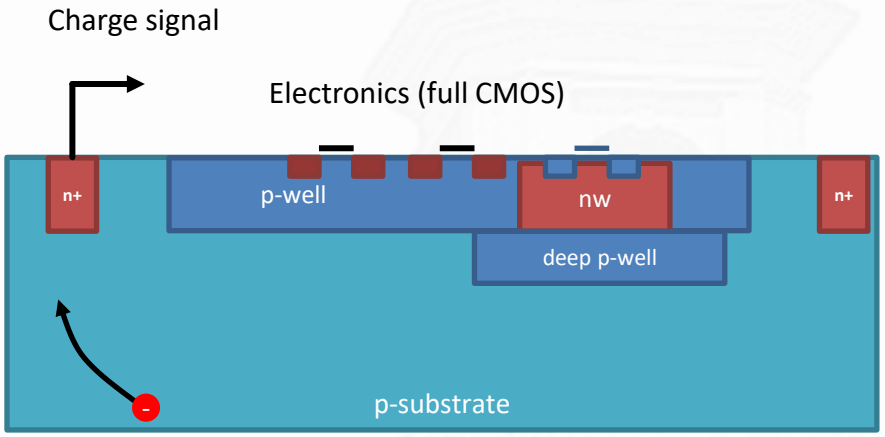
CMOS foundries can do good planar sensors (8”).

113 of 114 measured sensors have identical parameters

Device performance

Bulk process options (simple options, n-on-p)





Electronics **inside** charge collection well

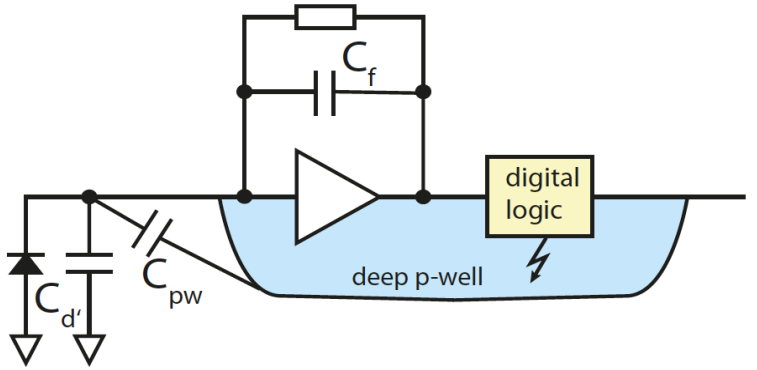
- Collection node with **large fill factor** → rad. hard
- Large sensor capacitance (DNW/PW junction!) → x-talk, noise & speed (power) penalties
- Full CMOS with isolation between NW and DNW

Electronics **outside** charge collection well

- Very **small sensor capacitance** → low power
- Potentially less rad. hard (longer drift lengths)
- Full CMOS with additional deep-p implant

Consequences of the additional inter-well capacitance

- larger total detector capacitance: $\mathbf{C_d} = C_{d'} + C_{pw}$

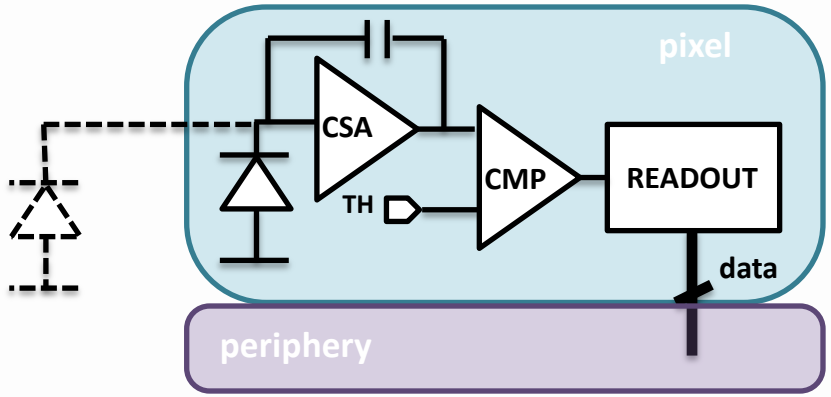


- noise $ENC^2_{thermal} \propto \frac{4}{3}\frac{kT}{g_m}\frac{\mathbf{C_d^2}}{\tau}$
- timing $\tau_{CSA} \propto \frac{1}{g_m}\frac{\mathbf{C_d}}{C_f}$

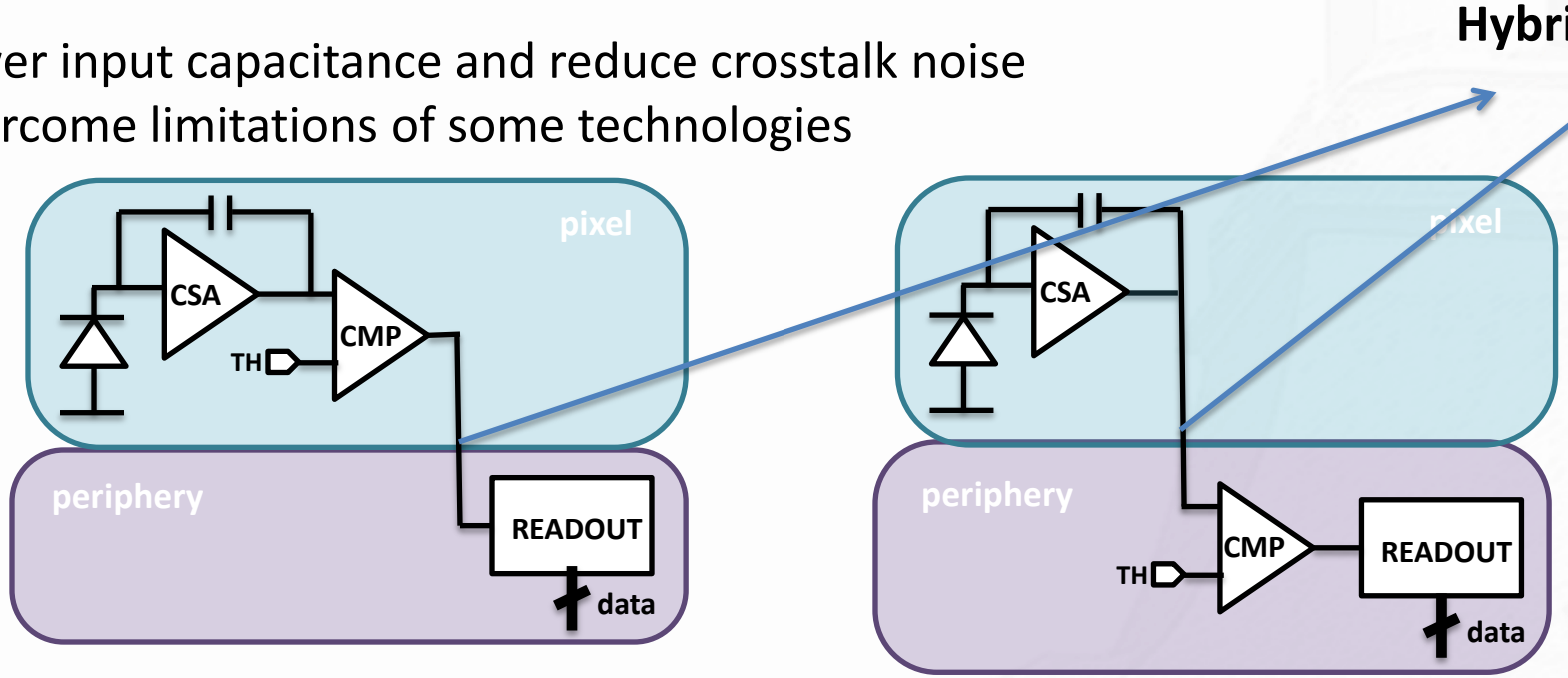
need to increase g_m to compensate
=> increased power ($g_m \propto I_d$)

- cross talking into sensor
  The PW/DNW capacitance C_{pw} directly couples into the sensor (the CSA imput node).
  Even with careful layout and low noise digital circuitry the operation threshold can be affected.
  For example: for C_{pw} = 100 fF, ΔV_{pw} = 1mV => $Q_{x\text{-}talk}$ = 625 e^-

Readout concepts



- Lower input capacitance and reduce crosstalk noise
- Overcome limitations of some technologies



Configurations

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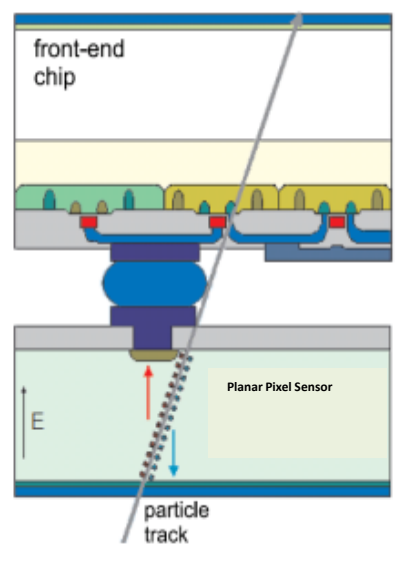
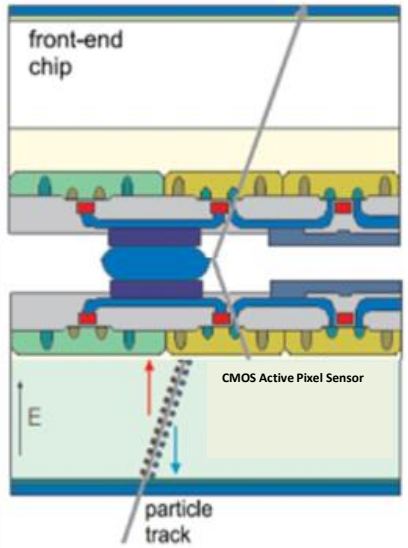
Standard Hybrid



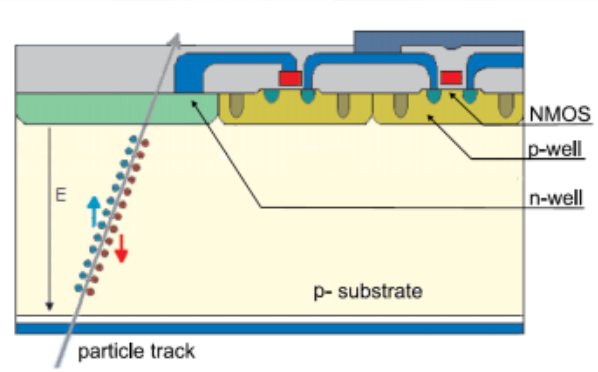
with CMOS planar sensor

CMOS Active Hybrid



Bumped or glued

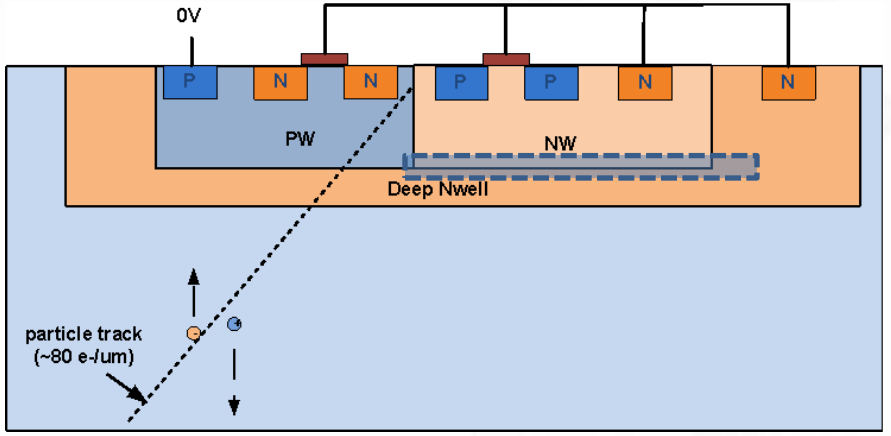
Depleted Monolithic

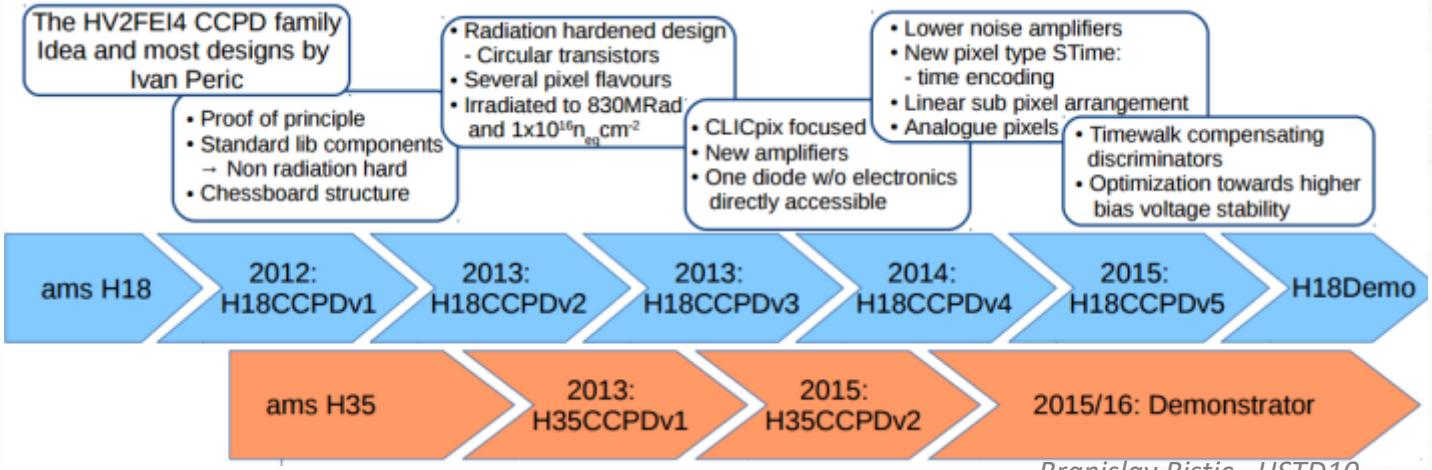


CMOS Devices Performance

AMS 180nm/350nm

- Substrate: **10 (initially) – 2k Ohm-cm**
- Bias: >60 – 100 V
- 180nm/350nm
- 3-6 metal layers
- KIT, Geneva, Barcelona, Liverpool, CCPM, CERN, Bonn , ..





Branislav Ristic - HSTD10

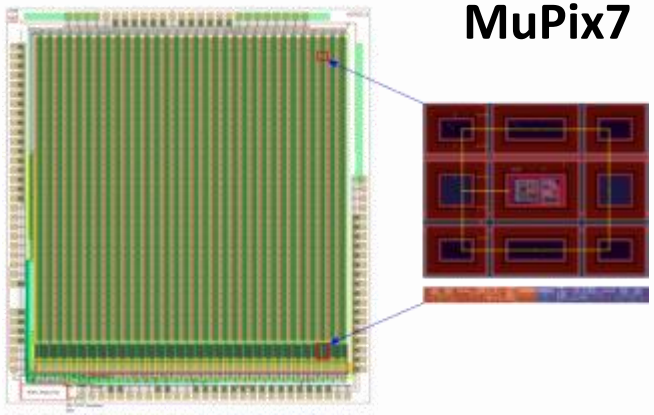
- Initially low resistive substrate now also **high**
- Initially no **PMOS isolation** now also available

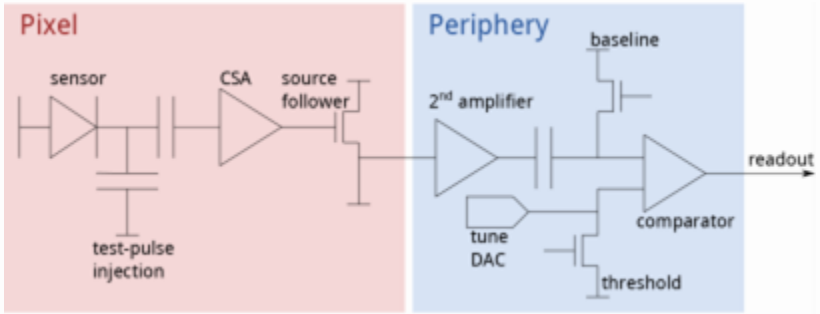
I. Peric et al. Nucl.Instrum.Meth. A582 (2007) 876-885
Nucl.Instrum.Meth. A765 (2014) 172-176

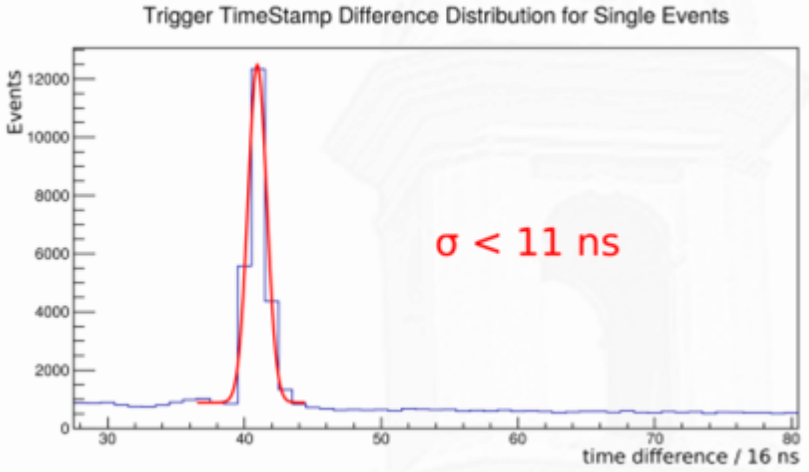
AMS 180 – MuPix - Mu3e @ PSI

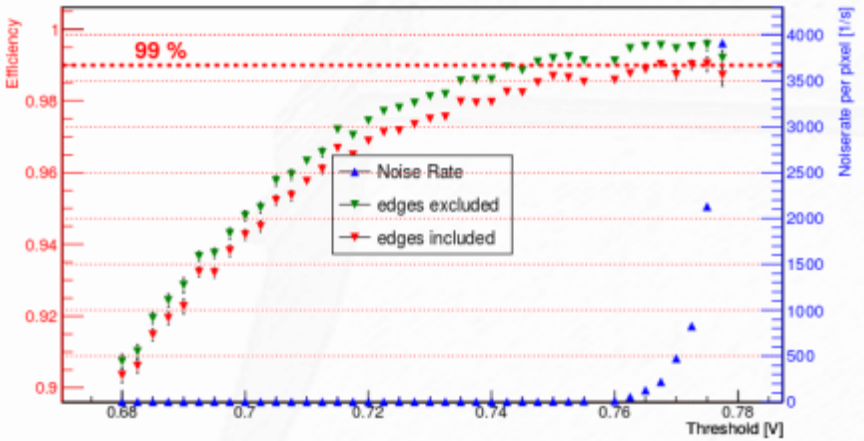
Technology: AMS 180nm
Dimension: 40 x 32 pixels (103 x 80 µm^2 each)
Preamplifier Inside pixel cell
Bias: 85V
Substrate 20 Ohm-cm (initially)

MuPix7







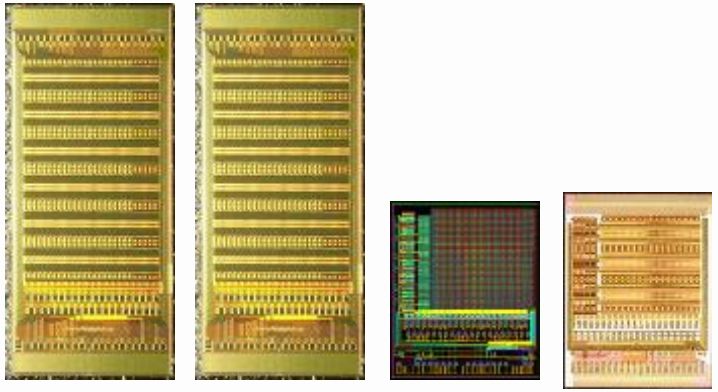


Dirk Wiedner, VCI2016

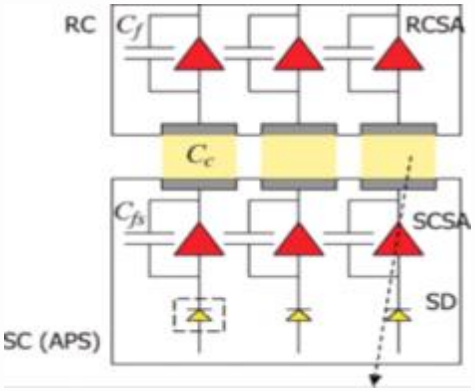
see: F. Meier Aeschbache, ”MuPix7 …”

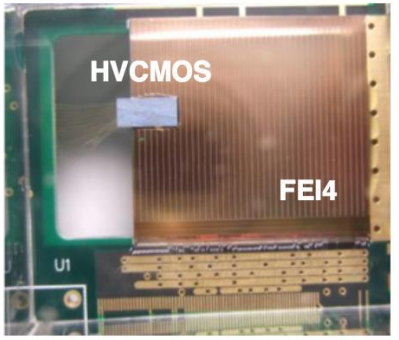
AMS 180 - CCPDv4

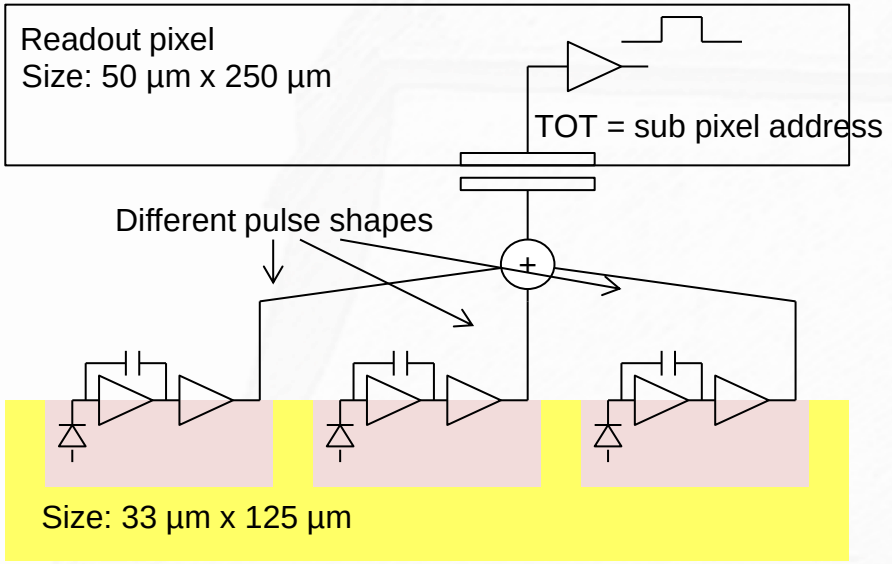
Technology: AMS 180nm
Dimension: 24 x 36 pixels (125x 33µm^2 each)
Bias: > 60V
Substrate: 20 Ohm-cm



CCPDv1 CCPDv2 CCPDv3 CCPDv4

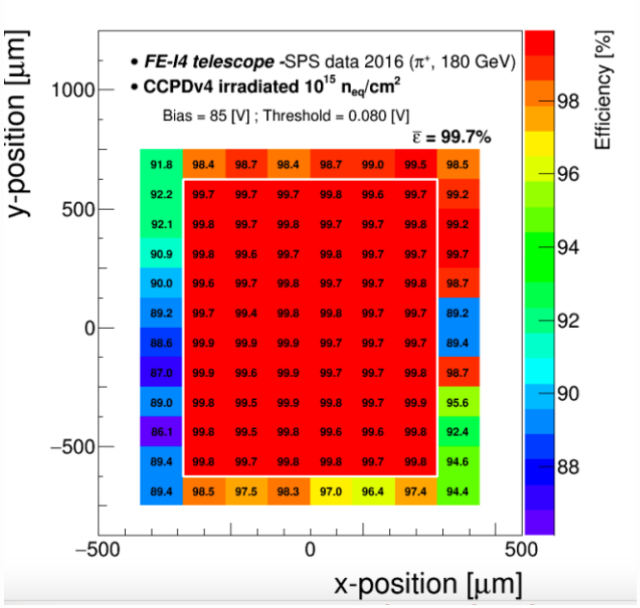


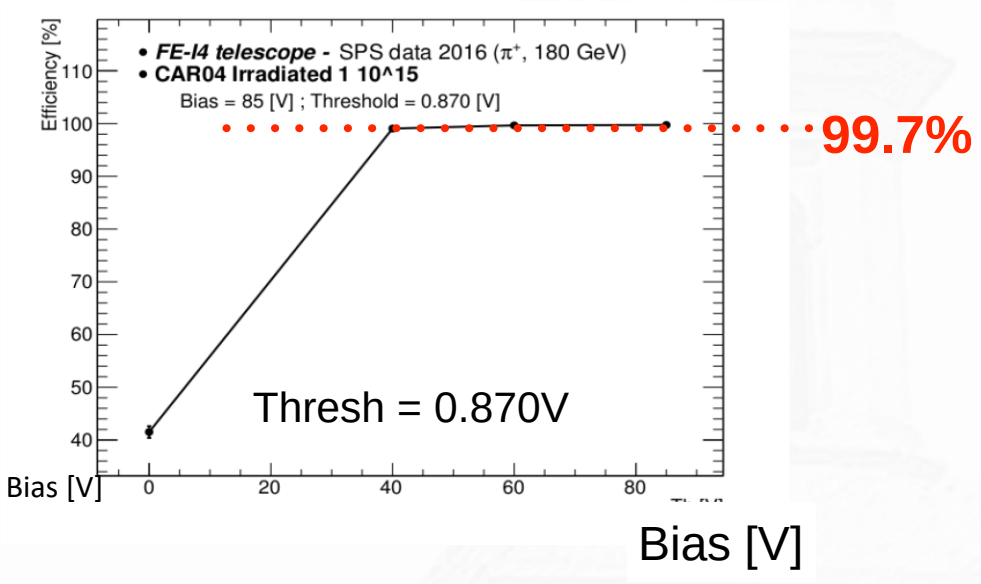


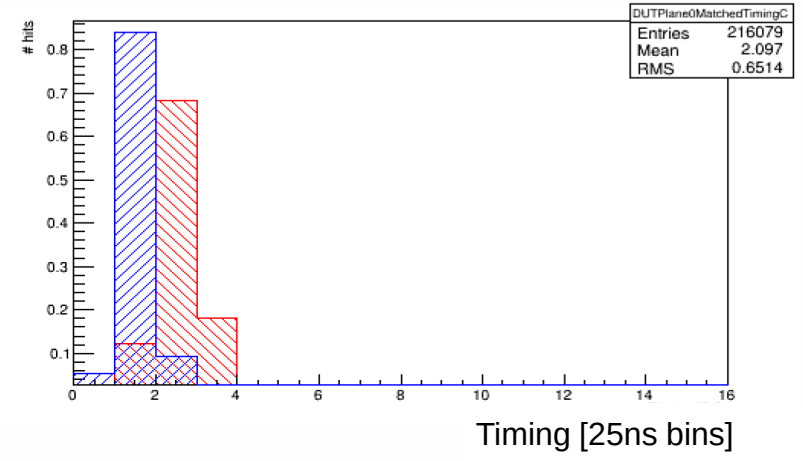


see I.Peric, "Status of HVCMOS …"

AMS 180 - CCPDv4 - Efficiency







High detection efficiency after $10^{15} n_{eq}$
Large monolithic design in preparation in AMS180.

see I.Peric, “Status of HVCMOS …”

AMS 350 demonstrator (H35DEMO)

4 resistivity : 20Ωcm (standard), 80Ωcm, 200Ωcm, 1kΩcm

Device types:

- Standalone nMOS matrix
- Analog matrix
- Standalone CMOS matrix (monolithic)

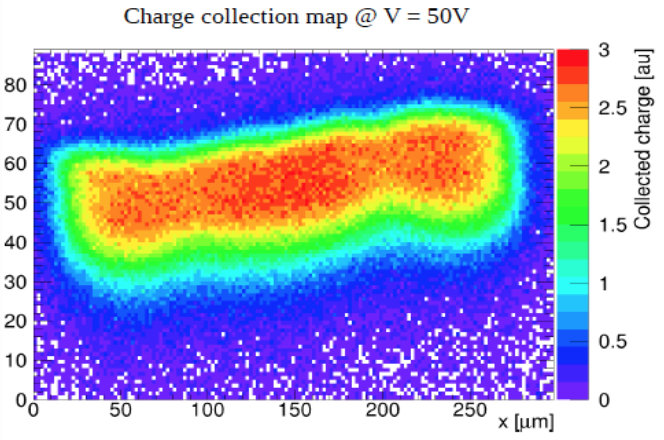
Demonstrated Bias up to 160V

Full readout + control in preparation for summer test beams

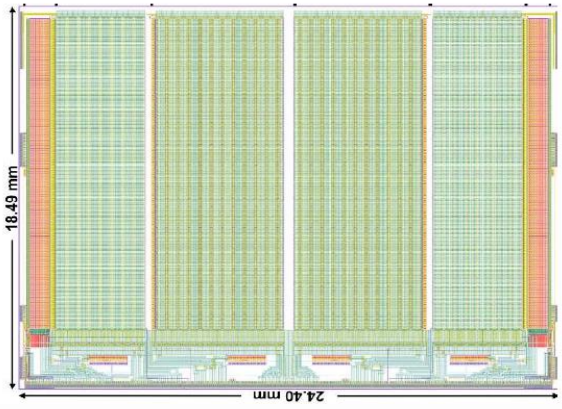
Irradiation campaign ongoing up to 1.5e15n_{eq}/cm^2

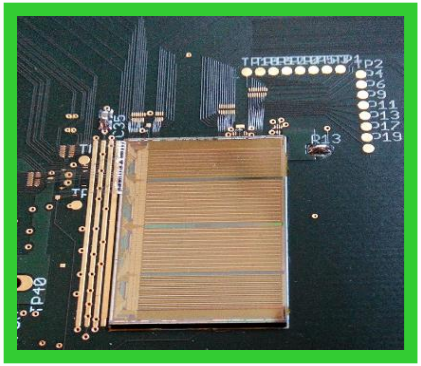
First TCT Results on 200 Ohm-cm substrate agree well with TCAD simulations

Edge TCT of H35DEMO Pixel 200Ohmcm
Pixel active on full length, 20-30um depletion



Mathieu Benoit (UniGe)

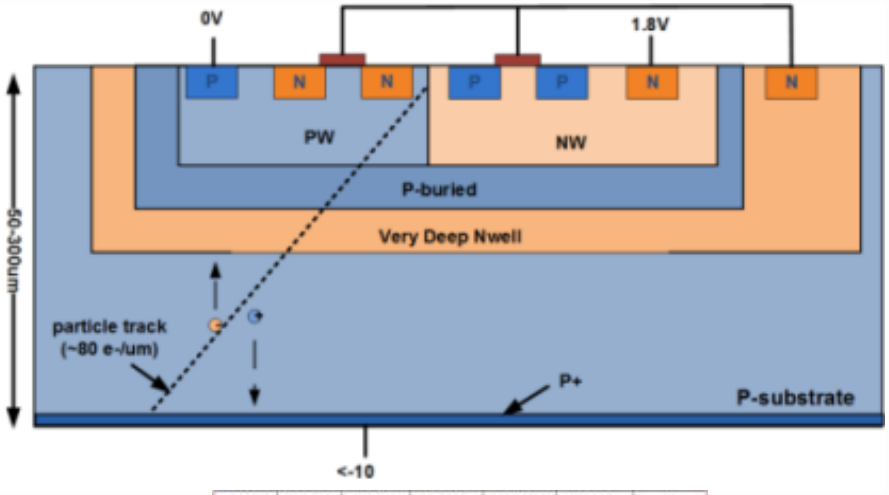


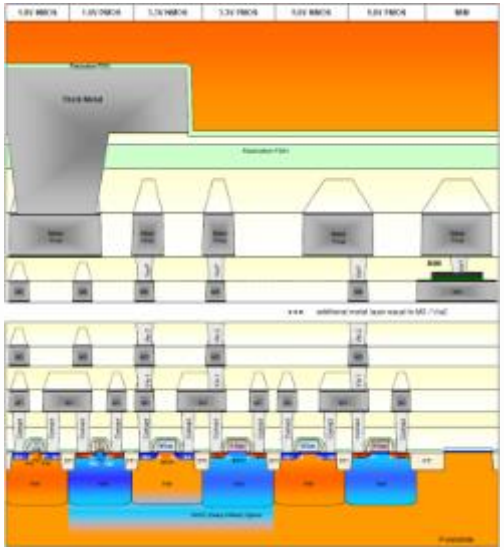


see: I.Peric, “Status of HVCMOS …”
E. Vielella Figuras [P]
A. Calandri [P]

Strip development:
CHESS-1, CHESS-2, …

LFoundry LF150



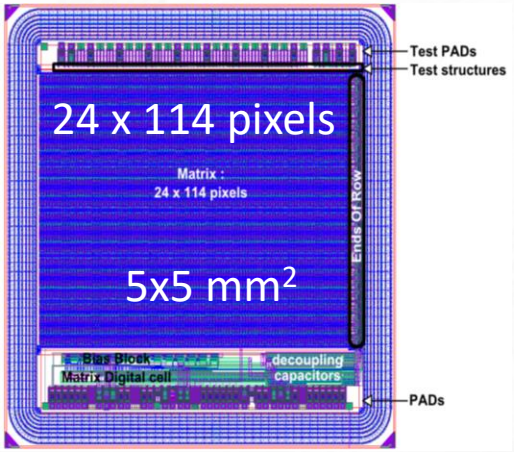


LFA150:

- L-Foundry 150 nm process (deep N-well/P-well)
- Up to 7 metal layers
- Resistivity of wafer: >2000 Ω·cm
- Small implant customization
- Backside processing

CCPD_LF prototype:

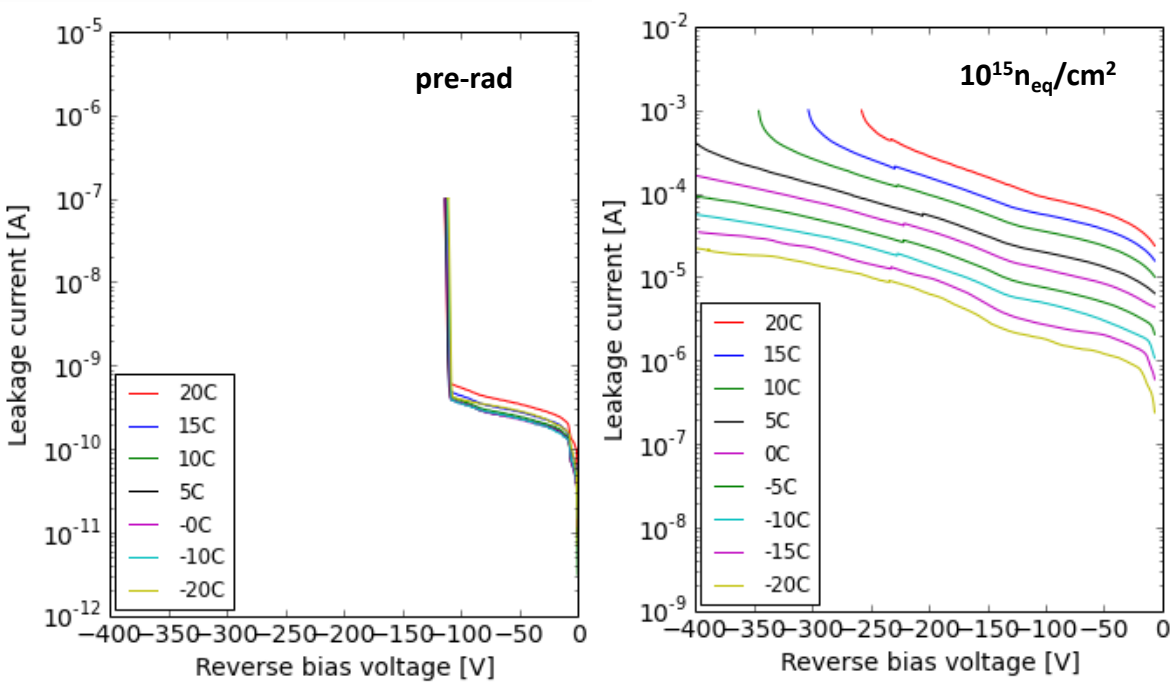
- Pixel size: 33um x 125 µm (6 pix =2 pix of FEI4)
- Chip size: 5 mm x 5 mm (24 x 114 pix)
- Bondable to FEI4 (+pixel encoding)
- **300um and 100um** version
- Bonn + CCPM +KIT



P. Rymaszewski et al., JINST 11 (2016) 02 C02045
T. Hirono et al., doi:10.1016/j.nima.2016.01.088

CCPD_LF

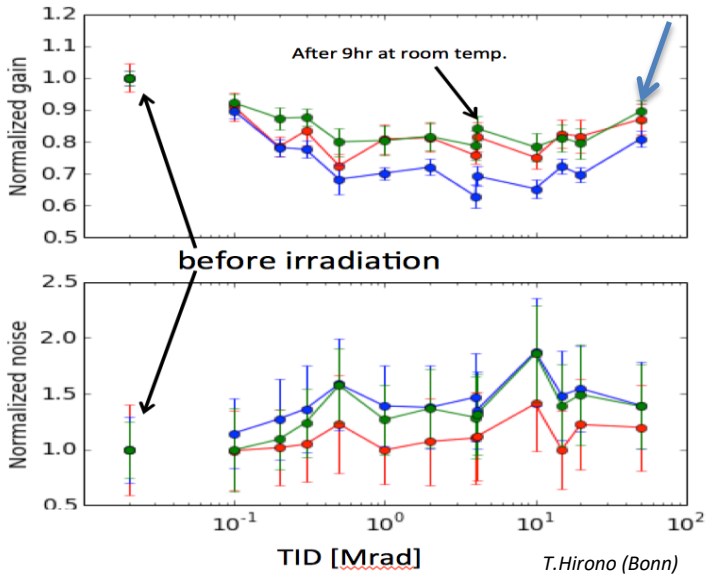
Leakage current



T.Hirono (Bonn)

TID

50MRad

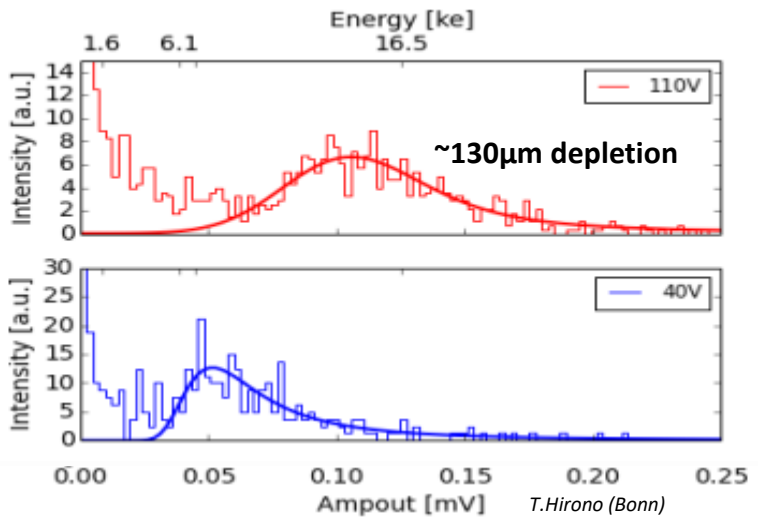


T.Hirono (Bonn)

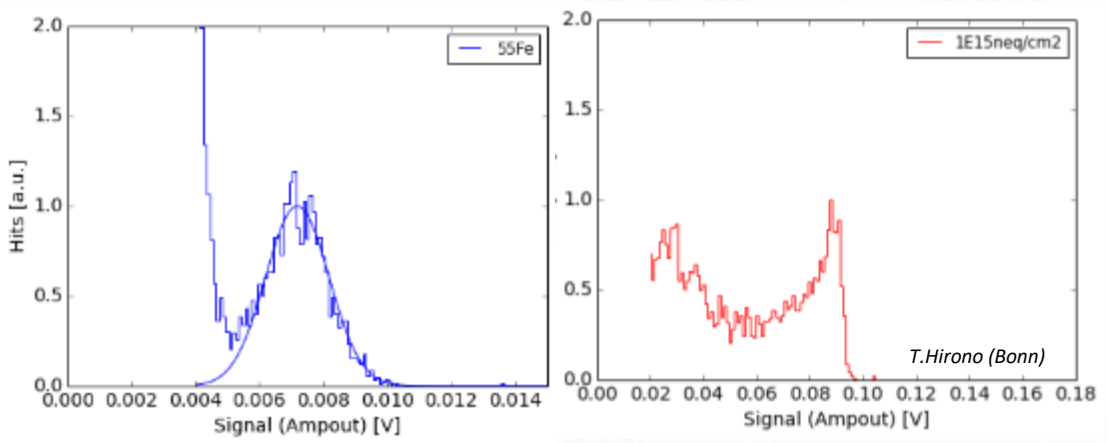
Normal (L=0.9um)
Long (L=1.5um)
Enclosed Layout (ELT)

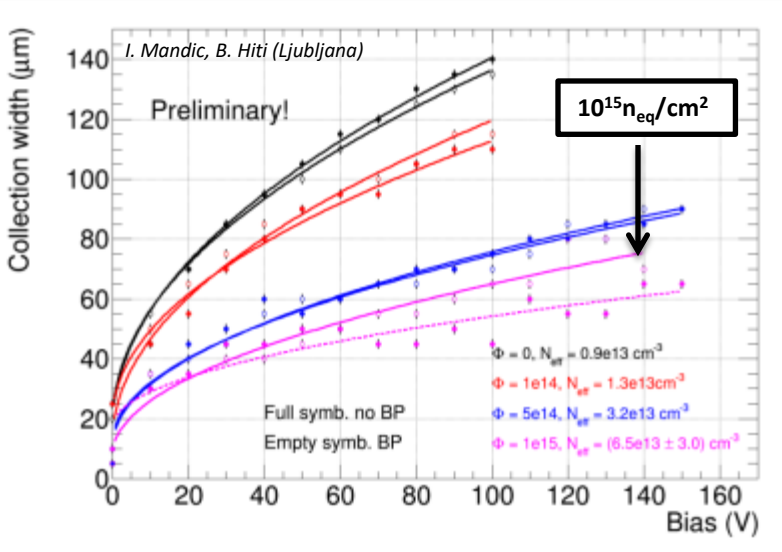
CCPD_LF results

MIP (3.2 GeV) spectrum (before radiation)

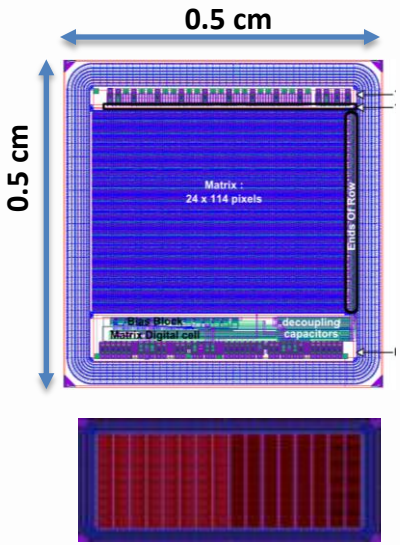


Sepctrum of ^{55}Fe and ^{241}Am after $10^{15}n_{eq}/cm^2$

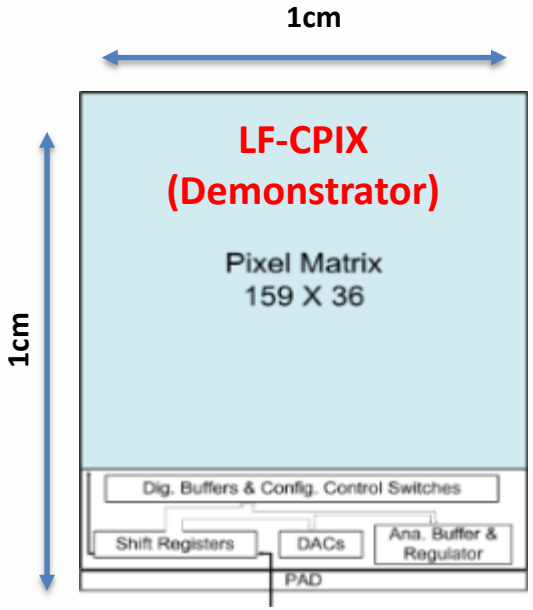




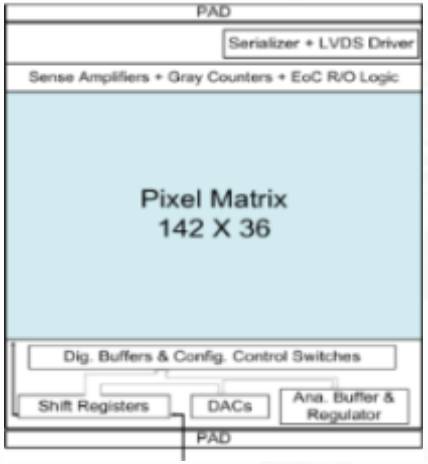
LFoundry timeline



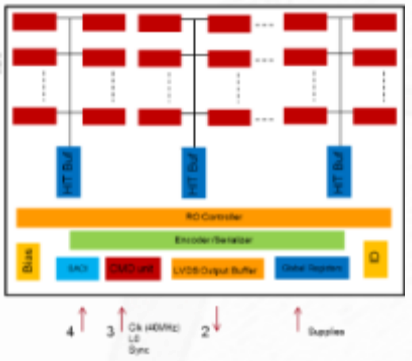
Bonn, CPPM ,KIT
CCPD_LF, ..(Aug. 2014)



Bonn, CPPM ,IRFU
LF-CPIX (April 2016)



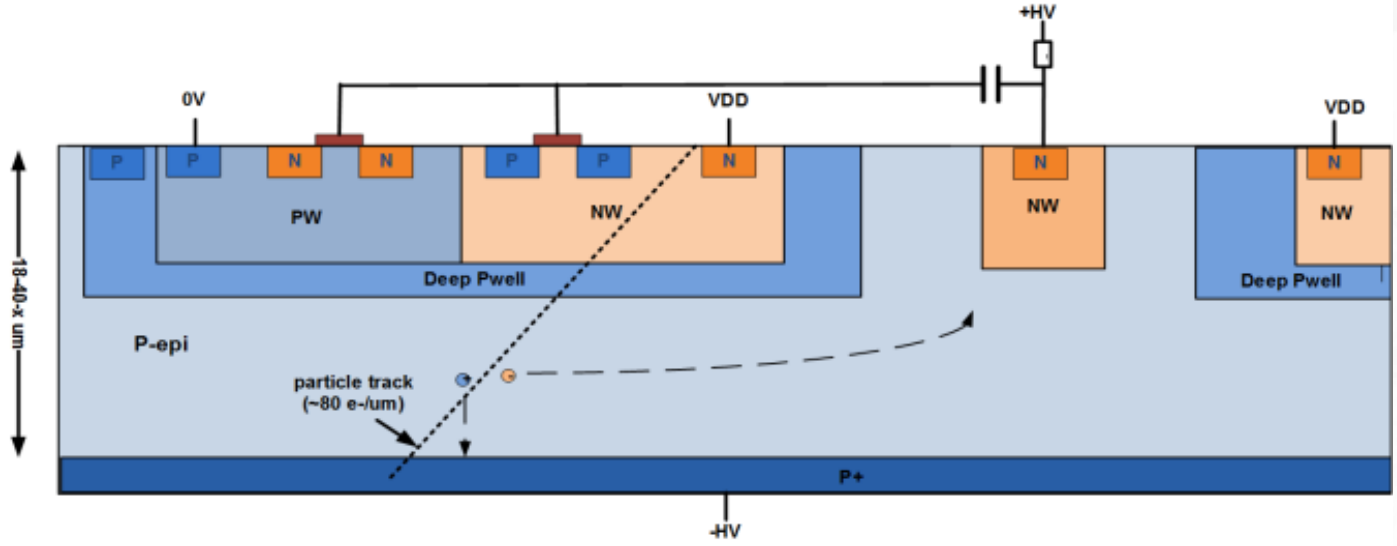
Bonn, CPPM ,IRFU
Monopix (Aug. 2016)



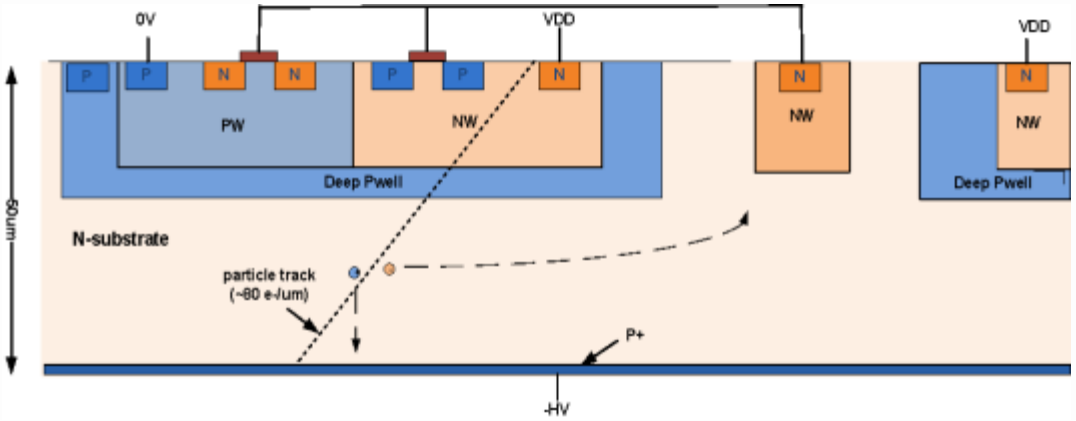
SLAC
COOL (Aug. 2016)

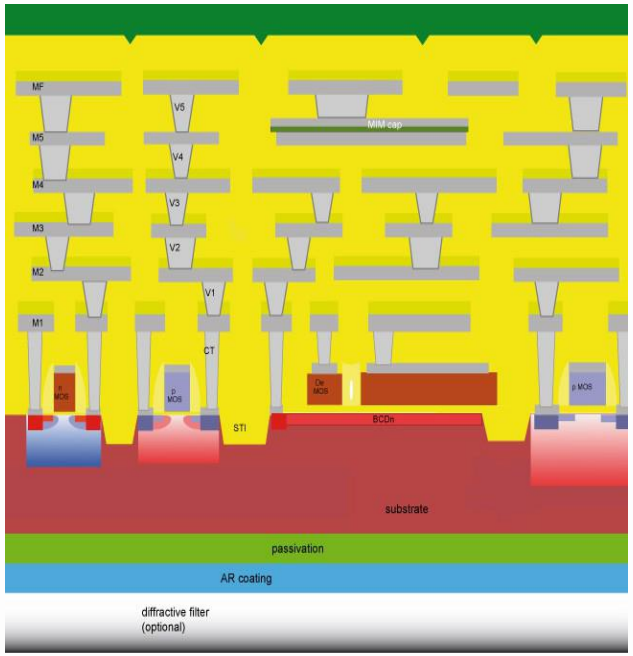
KIT, Liverpool, Barcelona,
Geneva
(Aug. 2016)

Logic outside collecting well



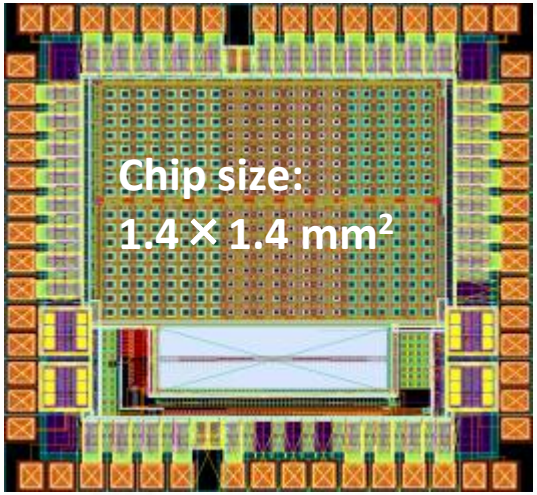
ESPROS Photonic CMOS™





OHC15L

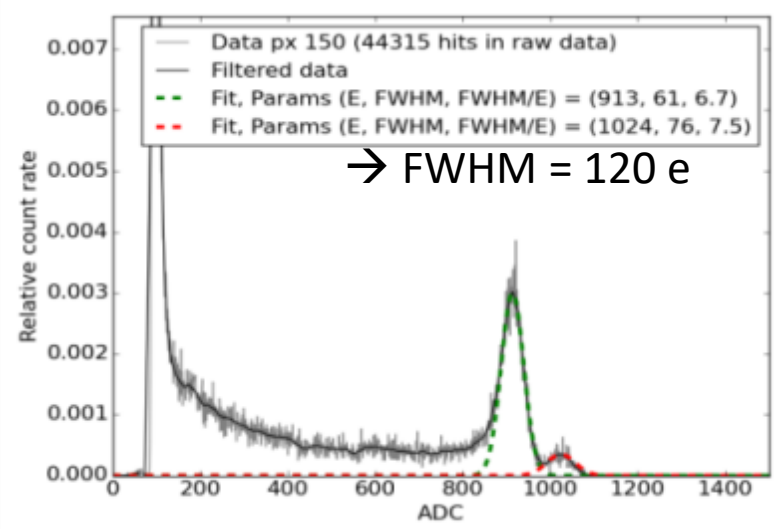
- 150 nm process (deep N-well/P-well)
- Up to 7 metal layers
- Resistivity of wafer (n-type): >2000 Ω·cm
- Backside processing
- **50um thin**
- Design: Bonn, Prag*



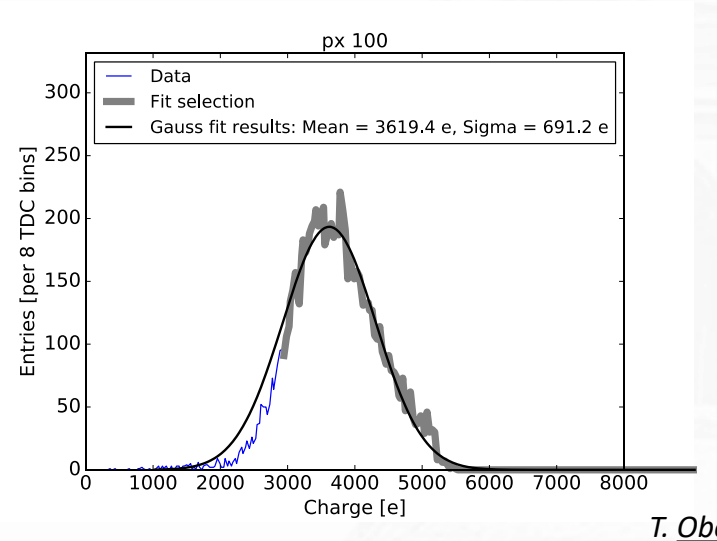
M. Havránek et al. JINST 10 (2015) 02, P02013

EPCB01

Fe^{55} spectrum

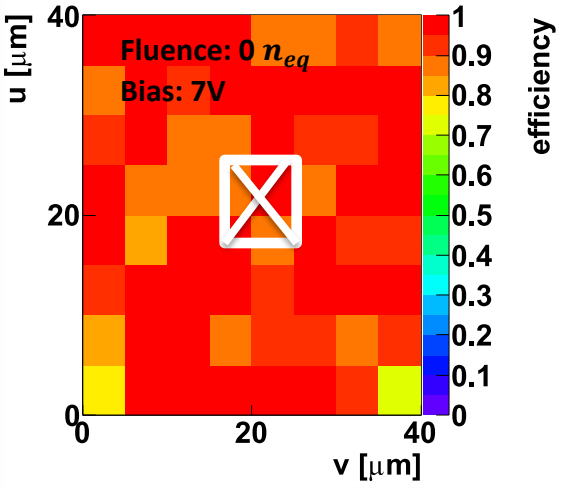


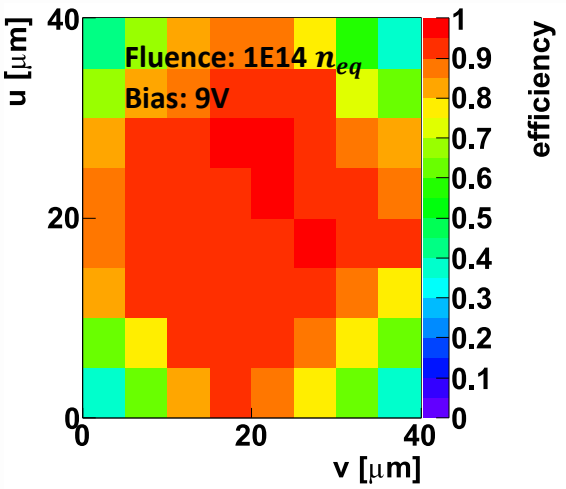
Calibrated single hit cluster spectrum Sr^{90}:

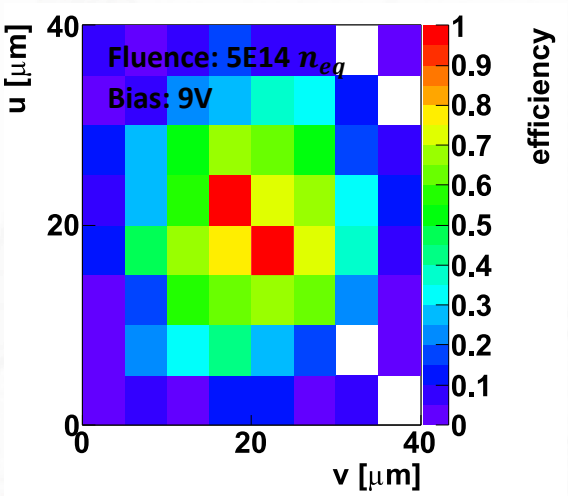


T. Obermann (Bonn)

In pixel efficiency

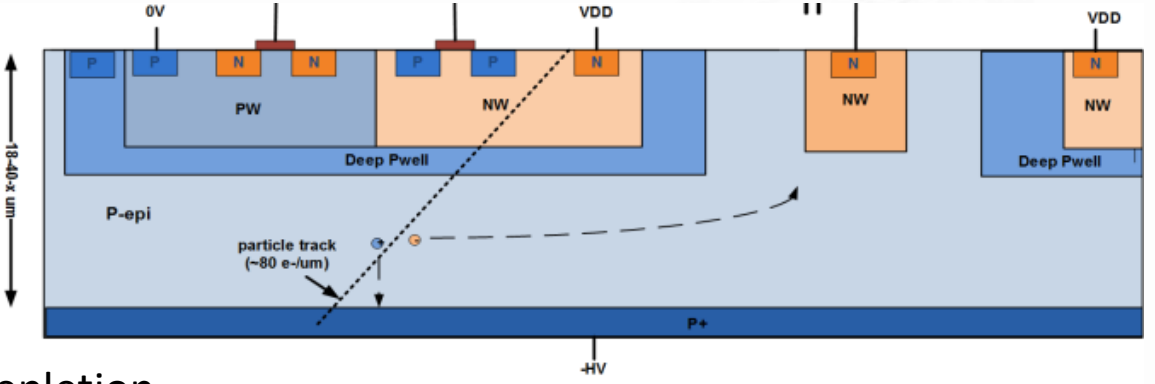


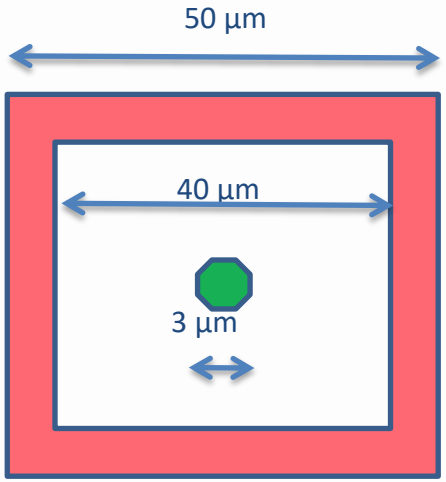




TowerJazz

- **TowerJazz** 180 nm CMOS CIS
- Deep Pwell allows full CMOS in pixel
- Gate oxide 3 nm good for TID
- Thickness: 18 – 40 µm
- High resistivity: 1 – 8 k Ohm-cm
- Reverse substrate bias
- **Modified process** to improve lateral depletion
- Derived from ALICE development (CERN) see: Miljenko Suljic „ALPIDE: the ”





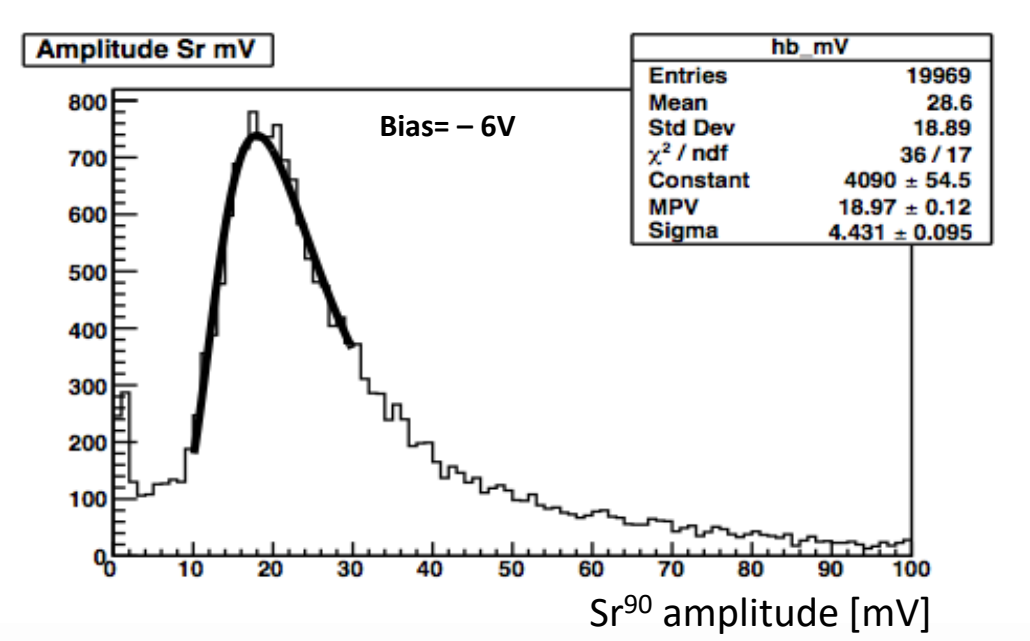
Pixel dimensions:

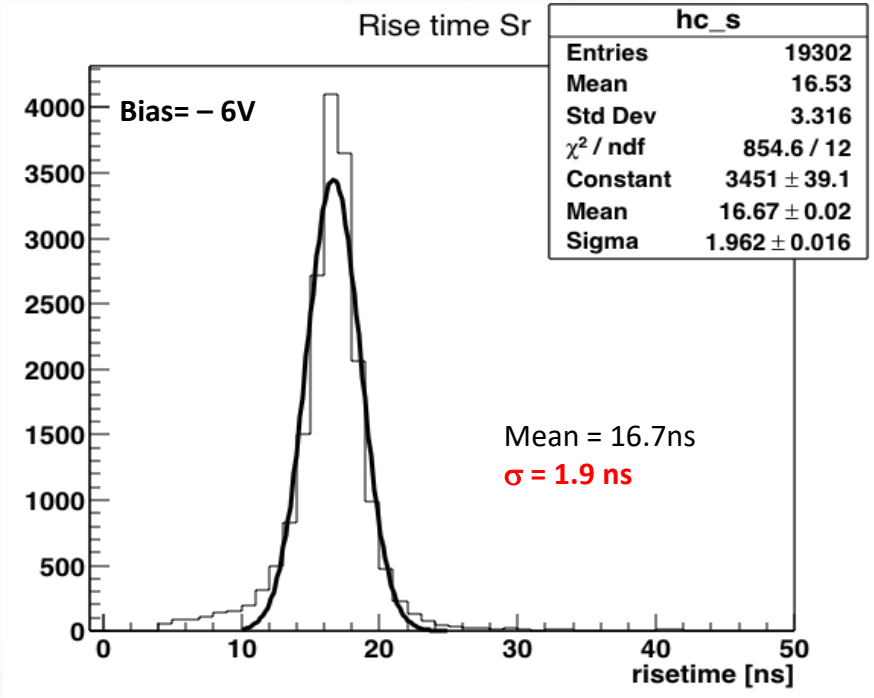
- 50x50um pixel size
- **3 µm diameter electrodes** and 40um Pwell opening
- 25um EPI layer
- **The pixels have a measured capacitance <5fF** (approximately factor 20 less than large fill-factor pixel) C. Gao et al., NIM A (2016) 831
- With this low capacitance, simulations indicate a front end similar to the one in the ALPIDE but compatible with 25 ns timing would consume ~ 200 nA)

Signal collection for small electrodes

- Normally small electrodes produce weak fields under p-well and charge gets lost after irradiation
- This usually means that efficiency drops significantly towards pixel edges
- **TJ modified its process to improve the efficiency after irradiation on pixel edges while keeping small capacitance** which makes this in particularly interesting for fast charge collection after irradiation
  - Pixel capacitance without process modification ~ 2-3fF with modification <5fC

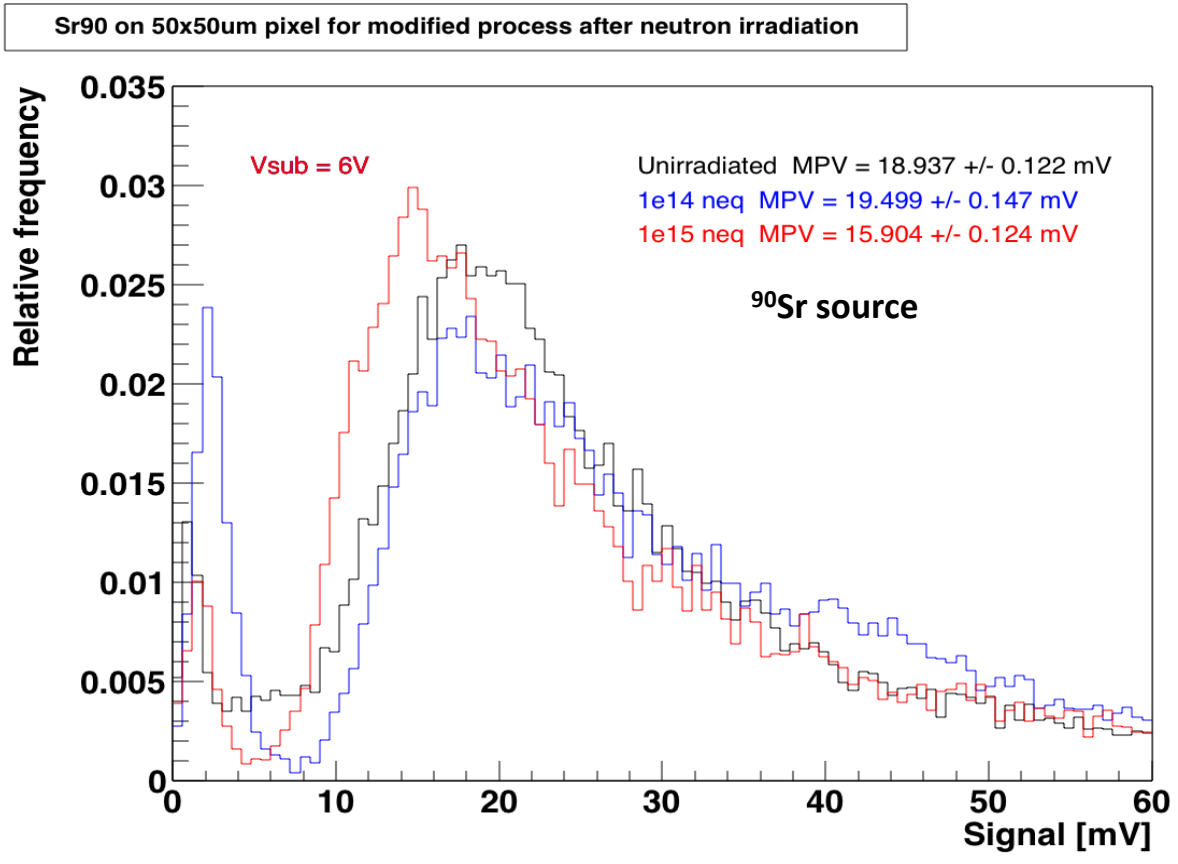
Modified process

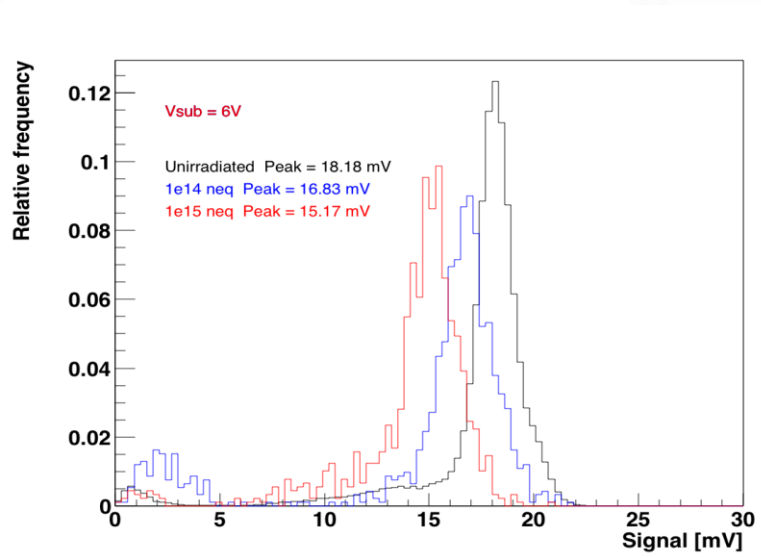




Neutron irradiation to 10^{14} and 10^{15} n/cm^2

- Investigator irradiated by IJS Ljubljana in several steps up to 10^{15}
- Irradiations up to 10^{16} ongoing
- This detector has received NIEL 10^{15} n/cm^2 and 1Mrad TID
- First test beam measurements indicate no efficiency loss on pixel boundaries after 10^{15} n_{eq}

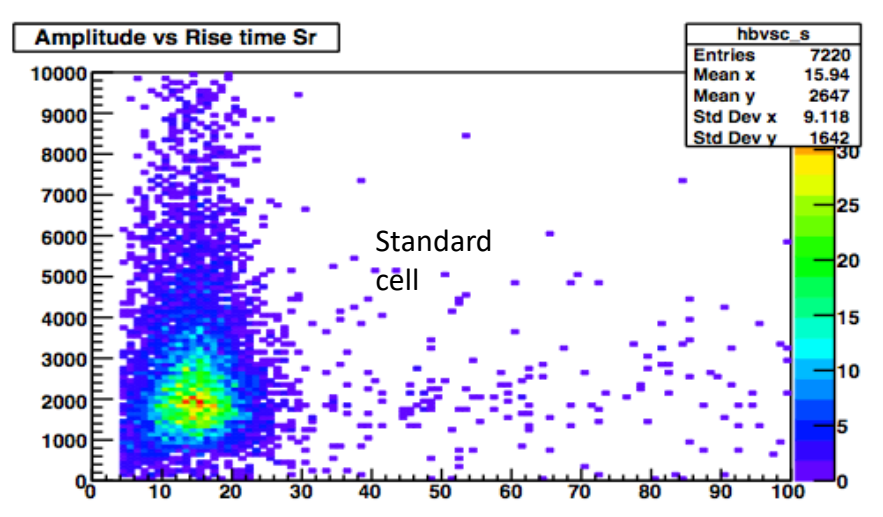


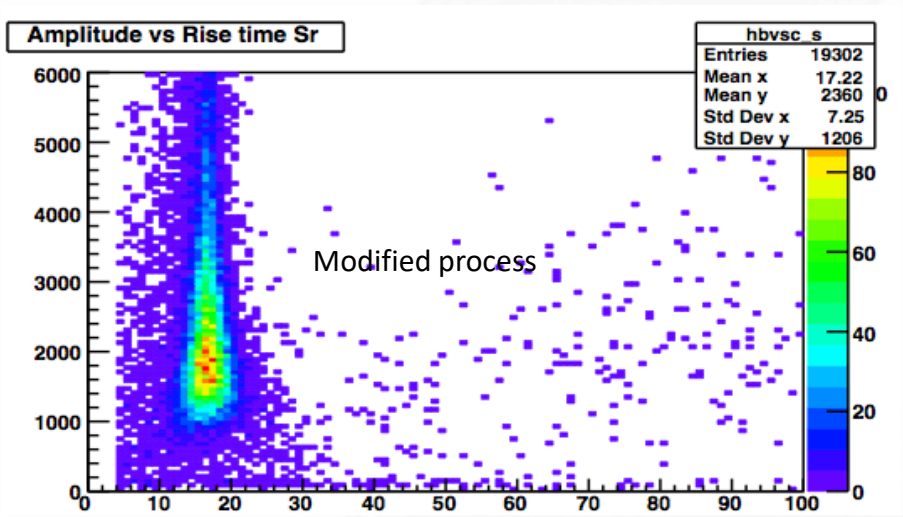


little change to signal (and capacitance !) after irradiation, -1 V is sufficient to observe a clear signal

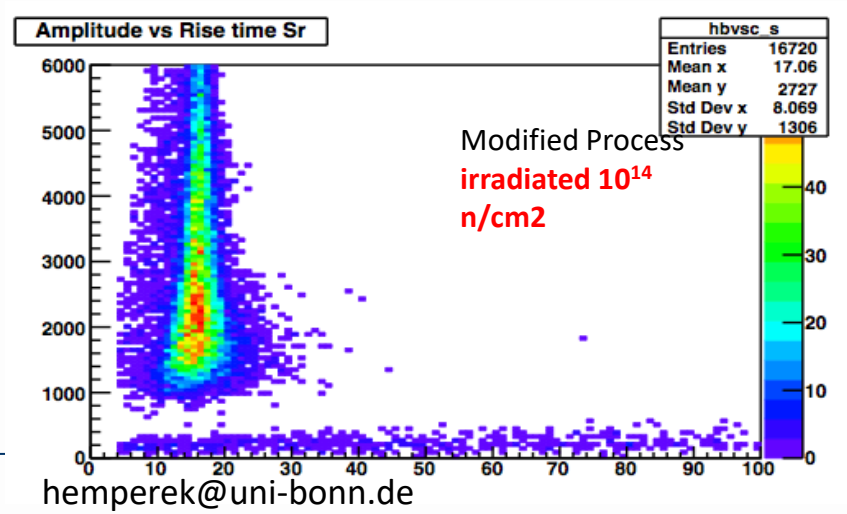
Signal versus collection time

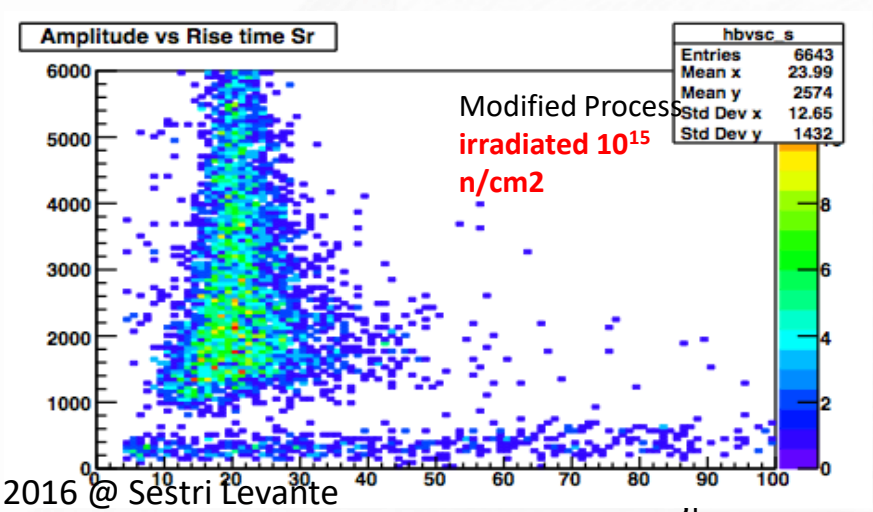
- Plot calibrated signal versus charge collection time
- Better timing with modified process (narrower collection time distribution)





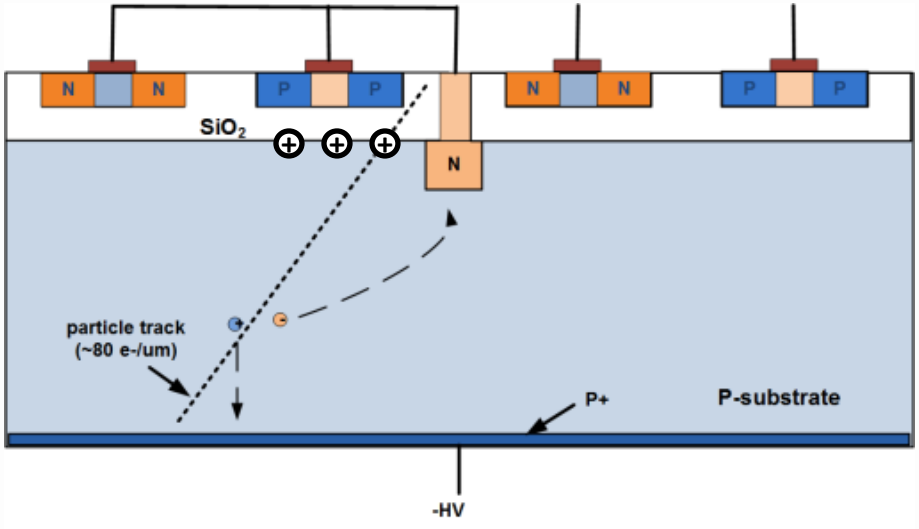
- Modified process after irradiation maintains charge collectionv



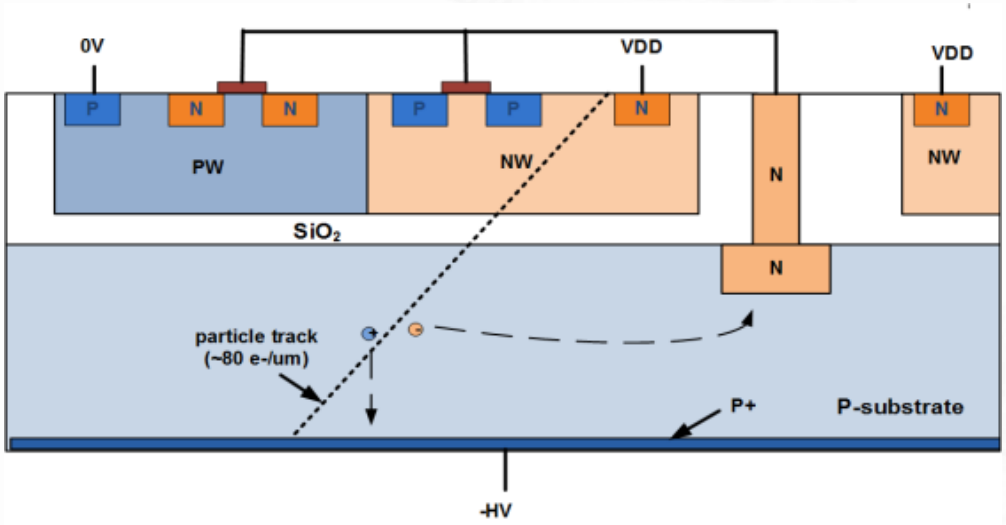


SOI

FD-SOI

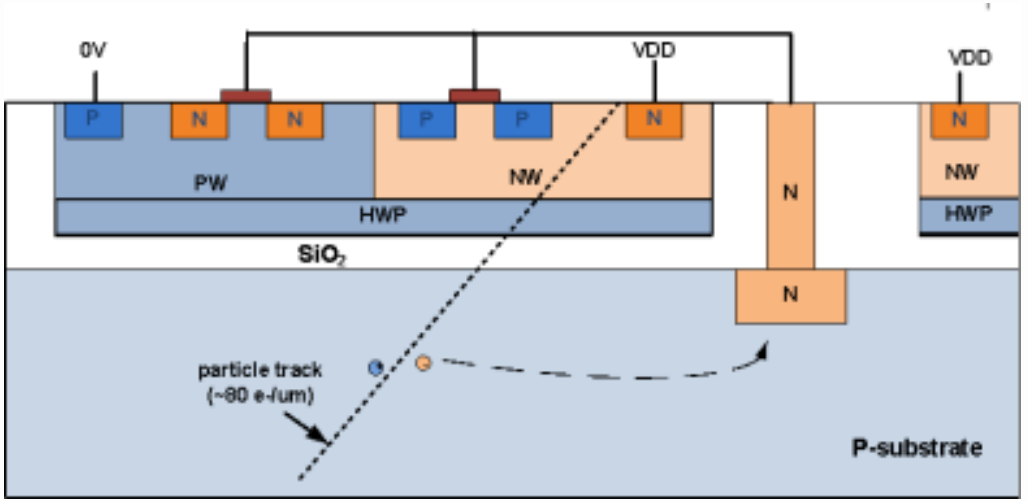


HV-SOI



see: S. Bugiel, “The performance …”
A. Takeda, ”Design and Development …”
R. Hashimoto, “Evaluation of”

XFAB XT180

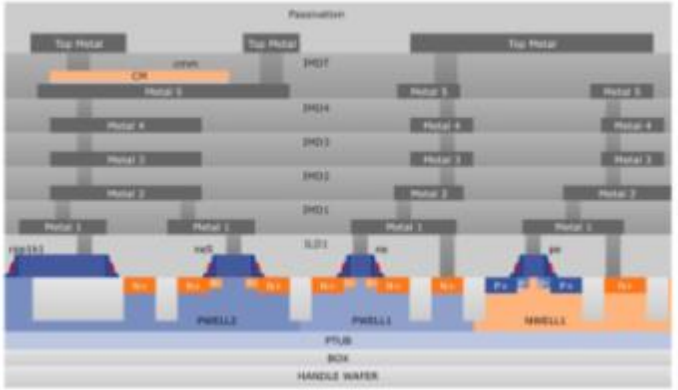


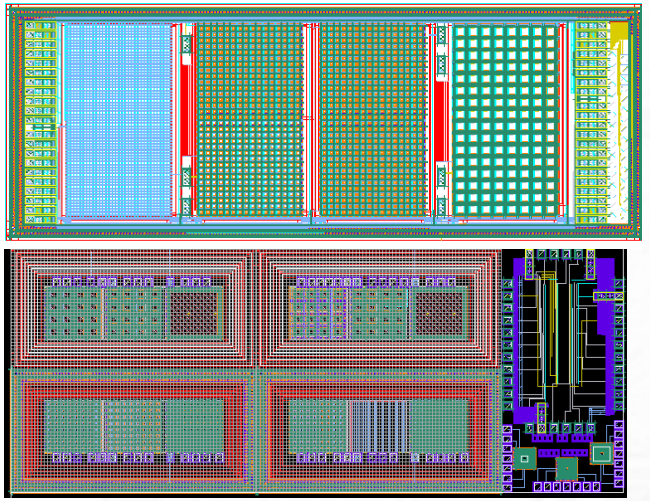
XT180:

- XFab 180 nm HV-SOI
- Up to 7 metal layers
- Resistivity of wafer: 100 Ω·cm

XTB01 and XT02 prototypes:

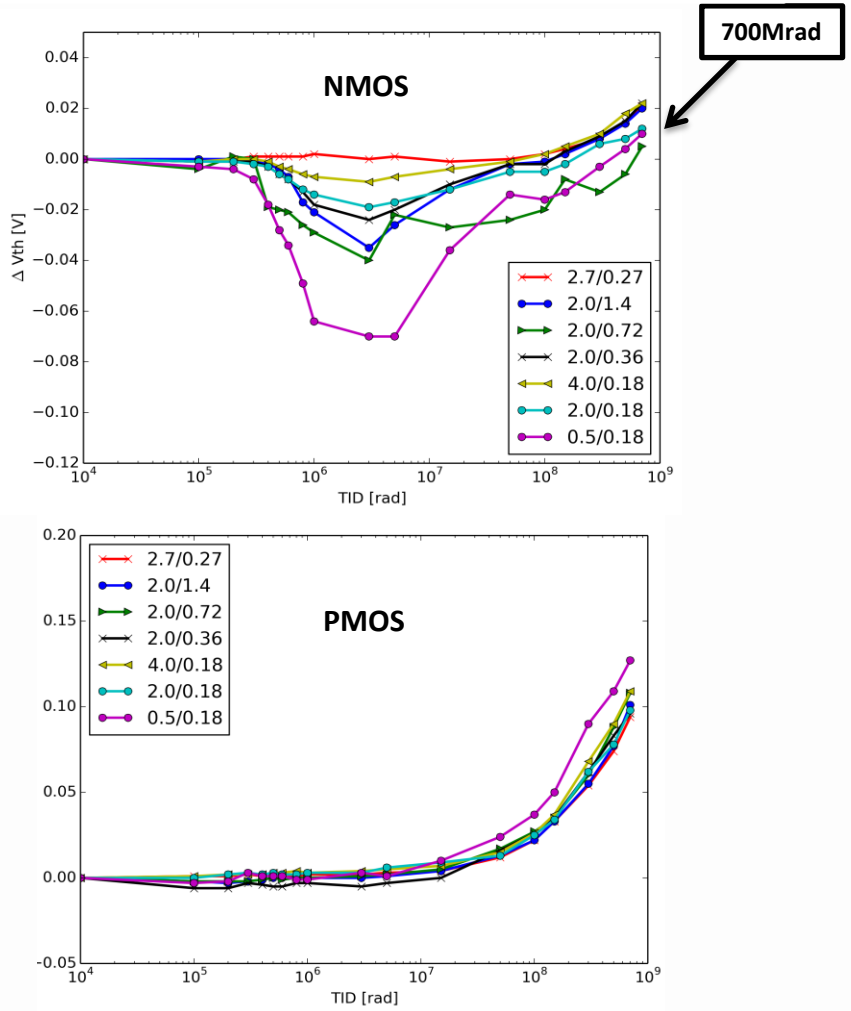
- Pixel pitch: 15, 50, 100um
- Chip size: 2.5 mm x 5 mm
- Design/Testing: Bonn, CERN, CPPM



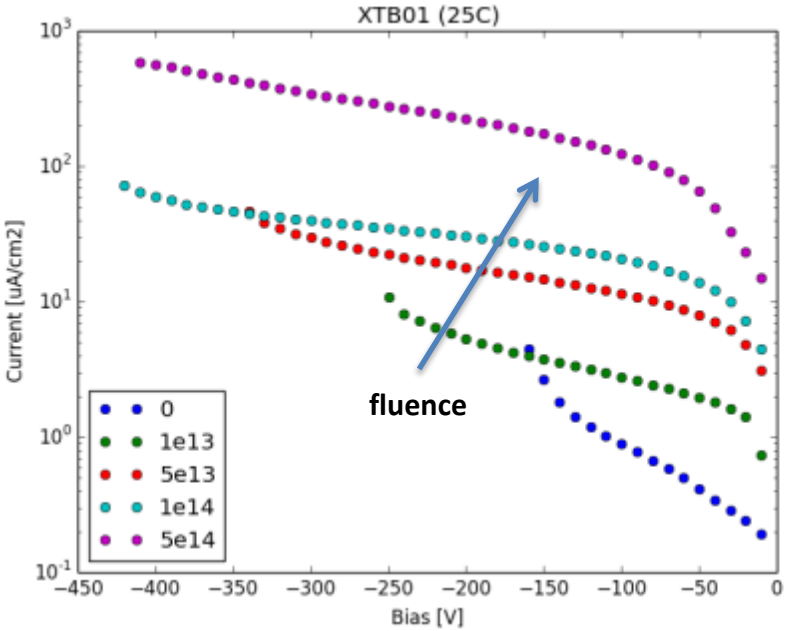


Sonia Fernandez-Perez et al. NIM A796 (2015) 13-18
Hemperek et al. JINST 10 (2015) no.03, C03047

Transistors threshold shift (TID)

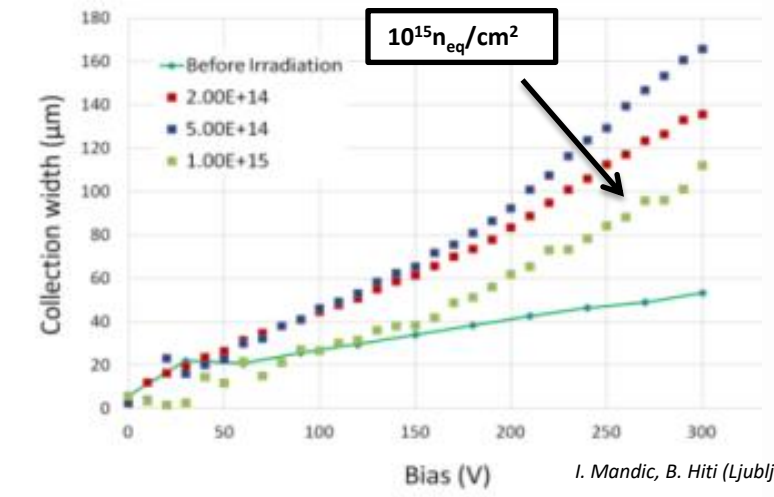


Leakage current (v1)



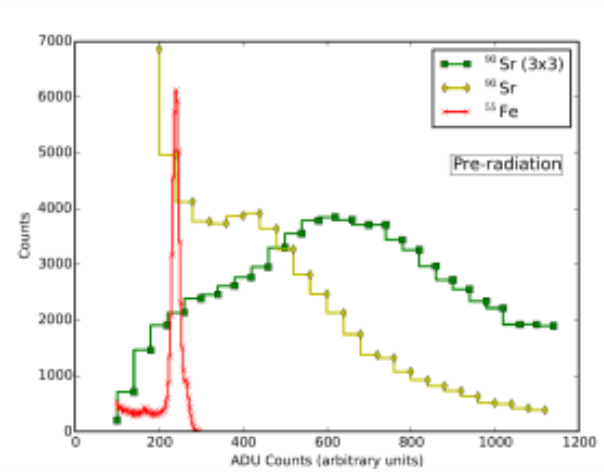
HV-SOI cd.

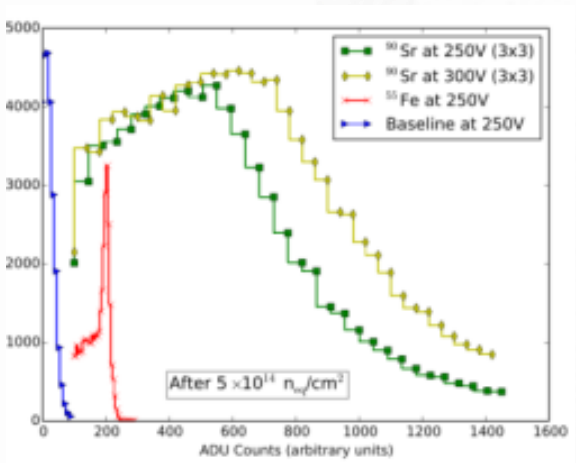
Collection with (edge-TCT) (v2)



I. Mandic, B. Hiti (Ljubljana)

Sepctrum of ^{55}Fe and ^{90}Sr before and after $5x10^{14}n_{eq}/cm^2$





Conclusions

Lots of encouraging results (high interest and large momentum in R&D)
Proven good radiation tolerance of sensors (and electronics)

Main asset for p-p HEP:

- Low(er) cost alternative to conventional hybrid sensors (as monolithic or cheaper hybrid)
- Coupling smart sensor and R/O chip can increase performance of hybrid sensors (e.g. position decoding)

Main asset for X-ray Imaging:

- Alternative to Fully Depleted CCD
- Increase performance of hybrid detectors (smaller pixels)

Ongoing:

- Large (fully monolithic) devices
- Fast timing measurements

CMOS Pixel Collaboration

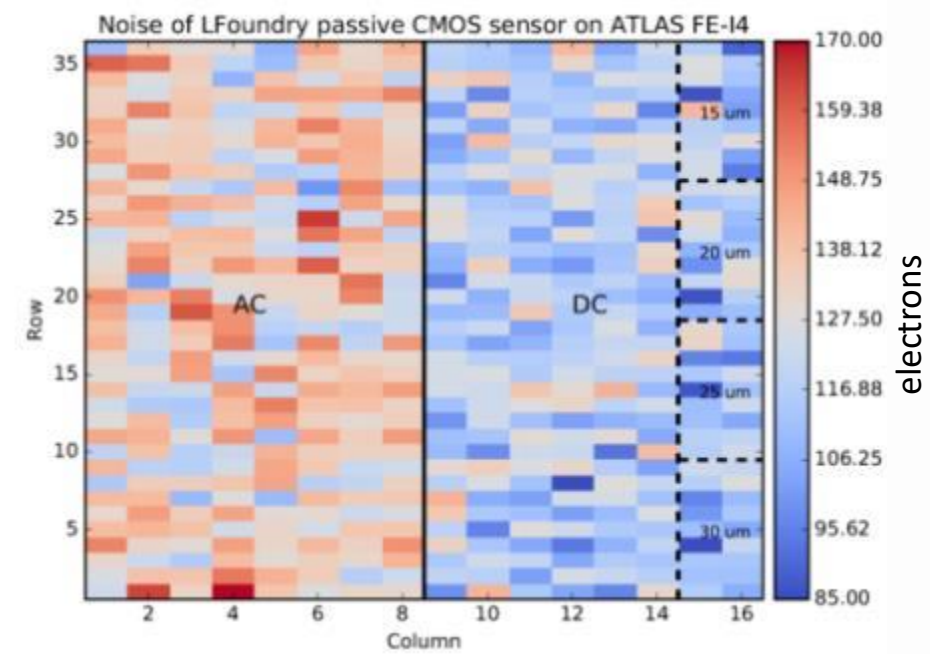
- ~20 ATLAS ITK institutions

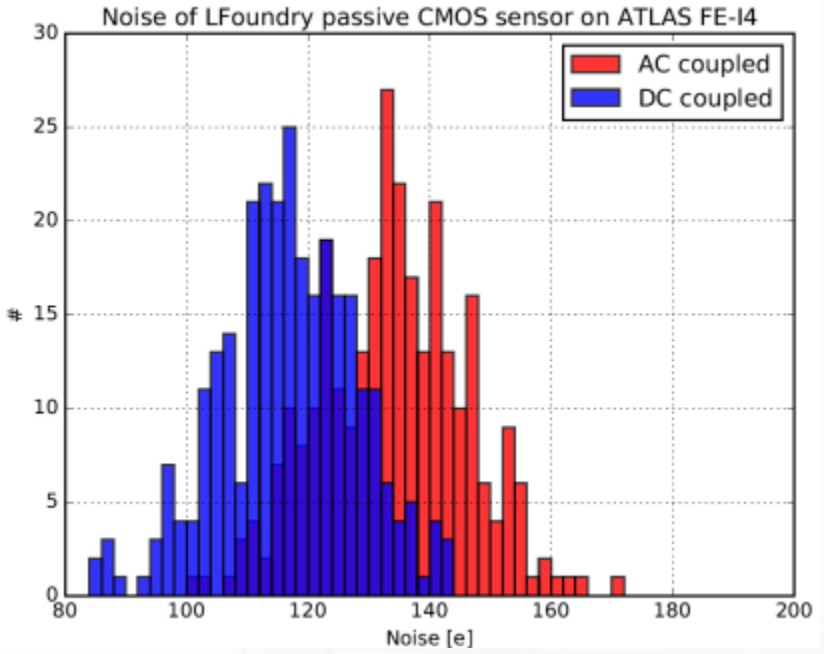
universitätbonn

SI LAB
Silizium Labor Bonn

Backup

Noise



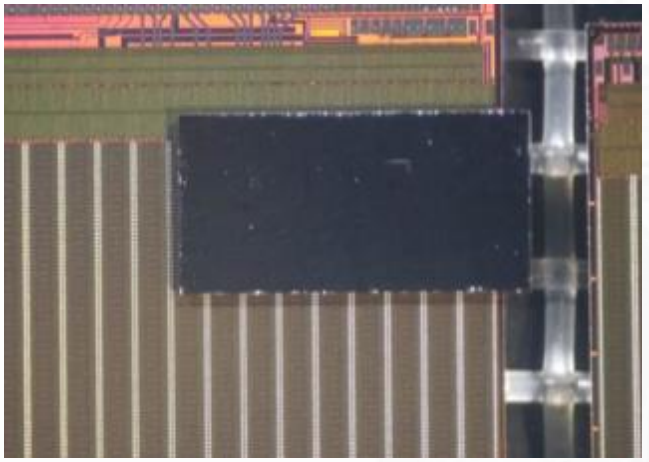


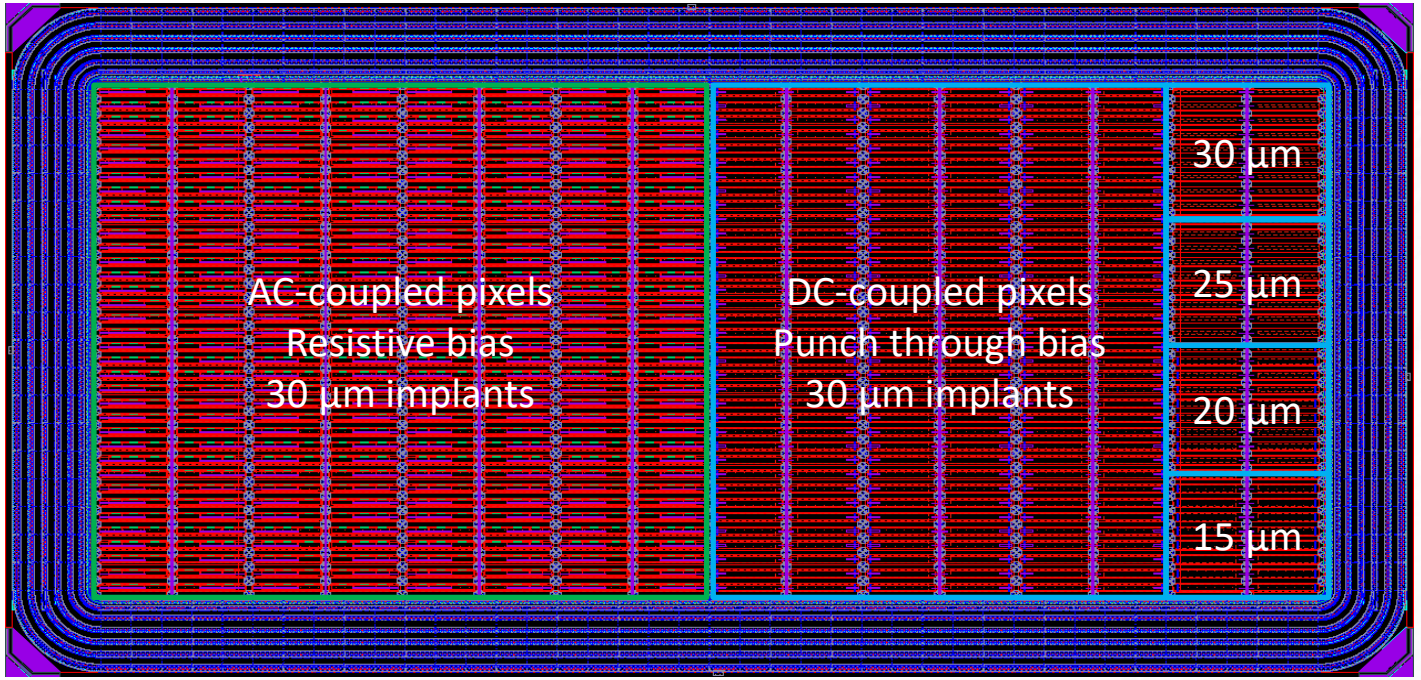
- **AC** couples pixels: **(133 ± 1) e⁻**
- **DC** couples pixels: **(117 ± 1) e⁻**
- *IBL n-in-n planar pixel: ~ 120 e⁻ @ 117 fF input capacitance*
- *IBL 3D pixel: ~ 150 e⁻ @ 180 fF*
- → **AC pixels: > 120 fF, < 180 fF; DC pixels: < 120 fF**
- First design: AC coupling R / C values and poly-silicon layer location not optimized!

Setup
- Threshold scan in pyBAR
- Bias voltage: 150 V
- FE-I4 direct powering

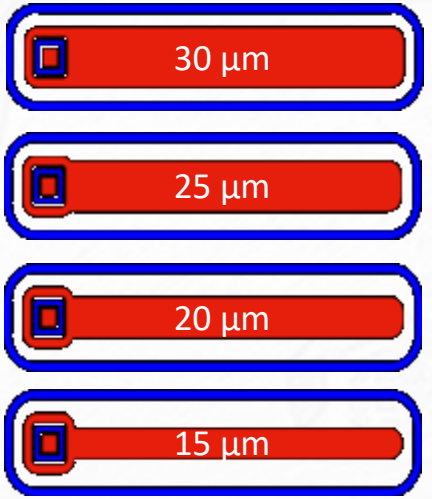
Passive LFCMOS sensor prototype

- LFoundry 150 nm CMOS technology
- 2 kΩ-cm p-type bulk, 8“
- 300 µm thick, backside processed
- Bump bonded to the ATLAS FE-I4
- Pixel size: 50 µm x 250 µm
- Matrix size: 16 x 36 pixels (1.8 mm x 4 mm)
- Bonn + MPI

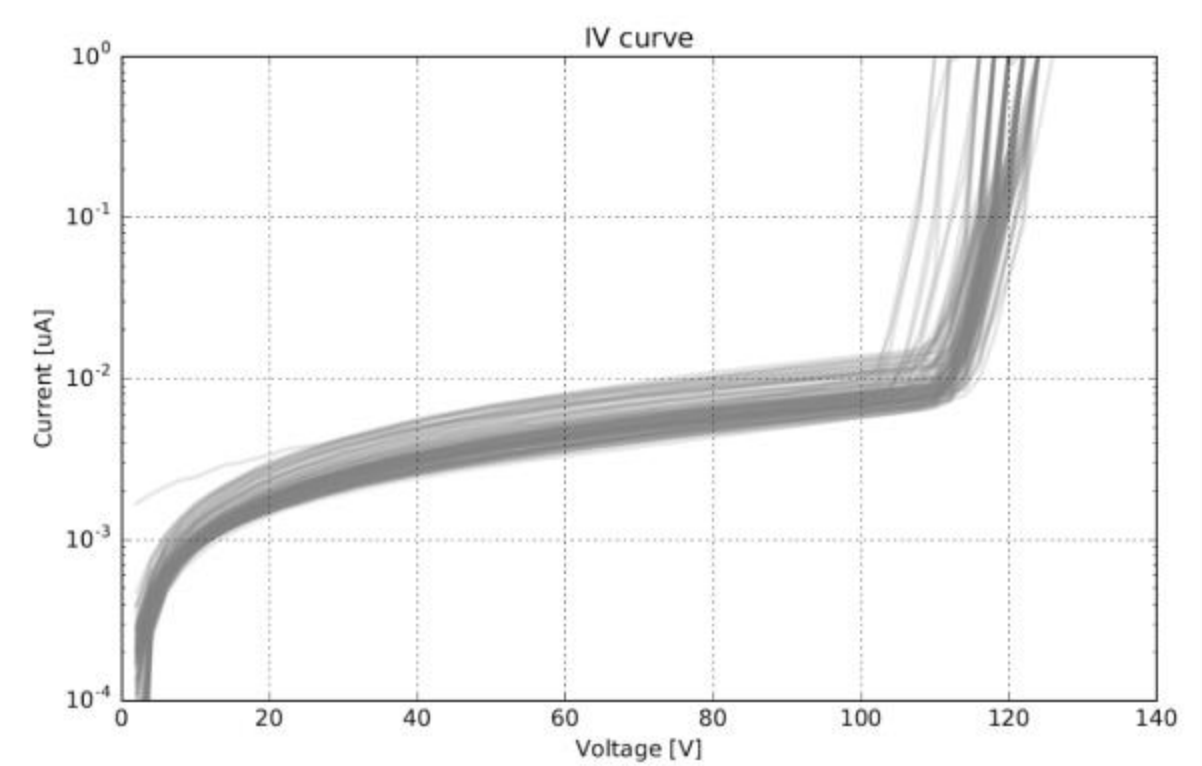




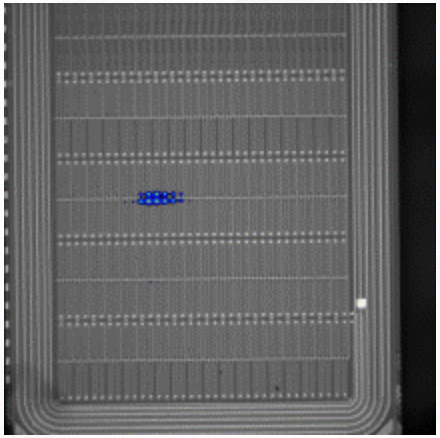
n-implant widths:
[30, 25, 20, 15] µm



Yield/Reliability



Breakdows at „bias dot”, DC version

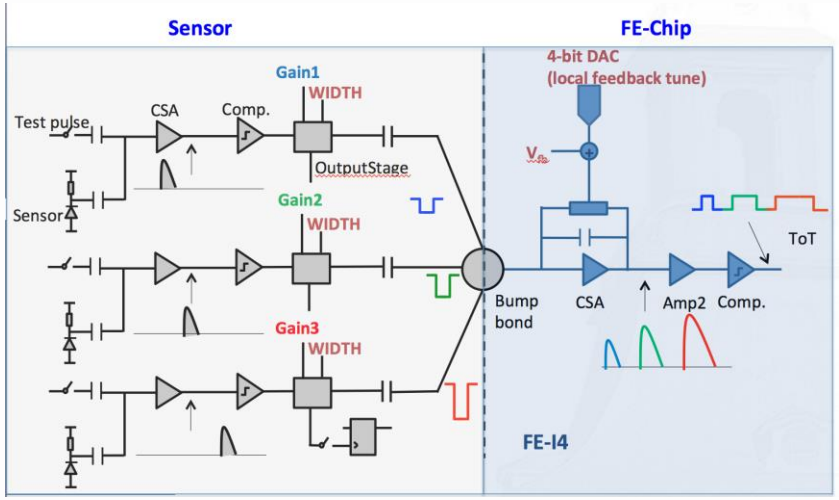


J. Segal (SLAC)

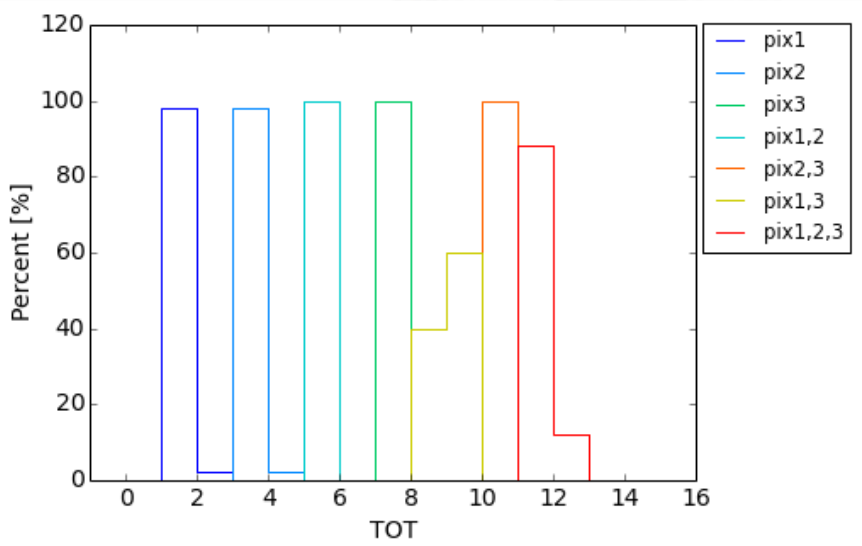
- 113 IV curves of the 300 µm LFoundry passive sensors
- 1 has short

Pixel Encoding

Readout of CCPD_LF and FEI4



ToT response of 3 CCPD_LF pixels



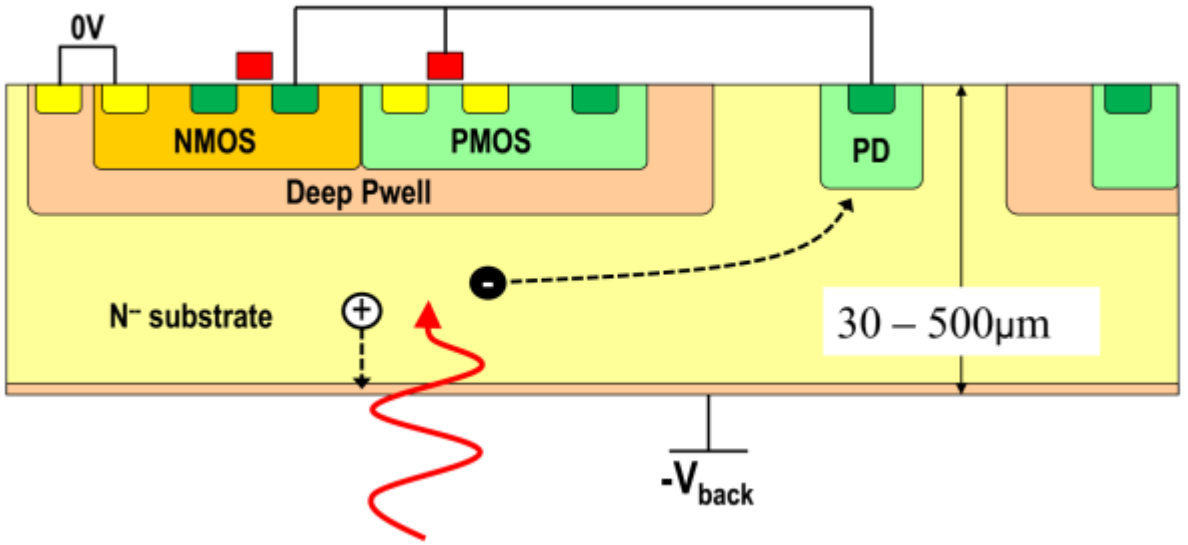
Monolithic Deep Depletion CMOS Image Sensor

universitätbonn

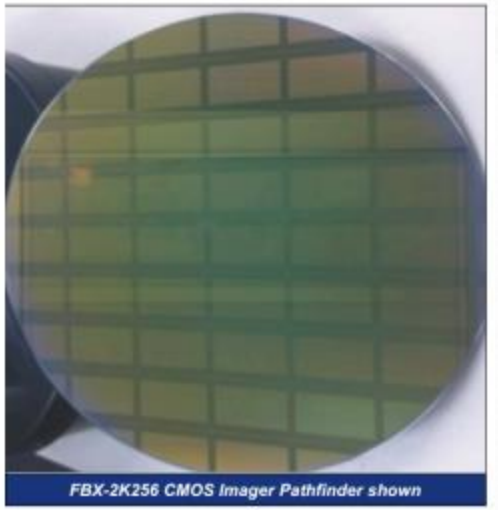
Sensor Creations

BRANDYWINE PHOTONICS

OPTICS	SPECIFICATION
Type	Fully-depleted, back-illuminated, eXtreme performance (FBX™)
Format	8192 columns x 512 rows
Pixel Size	7.5 µm x 15 µm
Full Well Capacity	Gain 0: 250,000 electrons Gain 1: 10,000 electrons
Read Noise	Gain 0: < 15 electrons Gain 1: 5 electrons
Maximum Frame Rate	> 500 Hz
Spectral Range	> 50% @ 380 nm 80% @ 400-900 nm > 30% @ 1000 nm
Exposure control:	Snapshot, Integrate While Read (IWR), Non Destructive Read (NDR) High Dynamic Range (HDR)
Dark Current	<0.5 nA/cm^2
Binning	1x2, 2x1, 2x2, 1x4
Output	16-bit Digital Interface, 128 outputs
Cooling	Single Stage Thermo-electric cooler
Power	< 12 Watts
Customization	Call for modifications to frame rate, well depth, or pixel pitch (other standard sizes available)

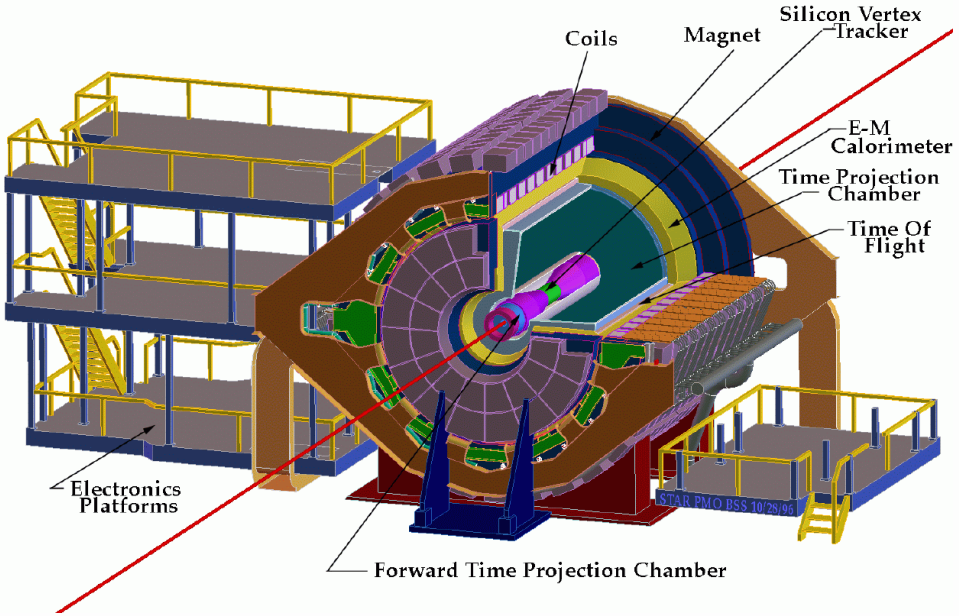


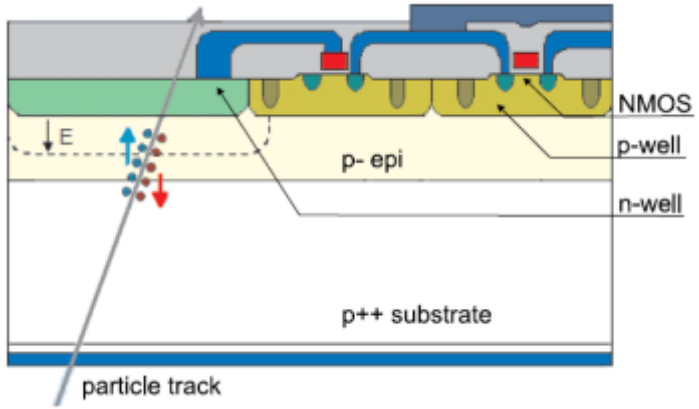
Quantum Efficiency



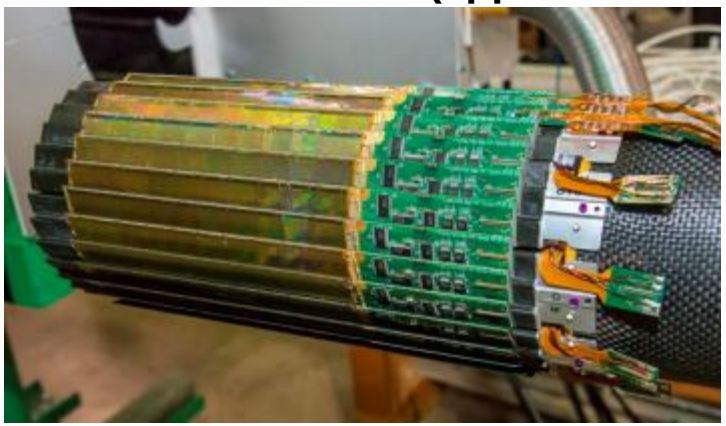
FBX-2K256 CMOS Imager Pathfinder shown

STAR Experiment

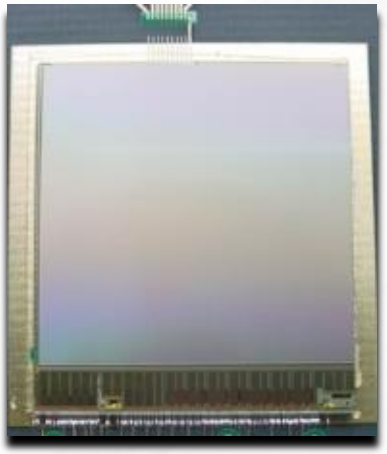




Ladders with 10 MAPS sensors (approx. 2×2 cm each)



Ultimate

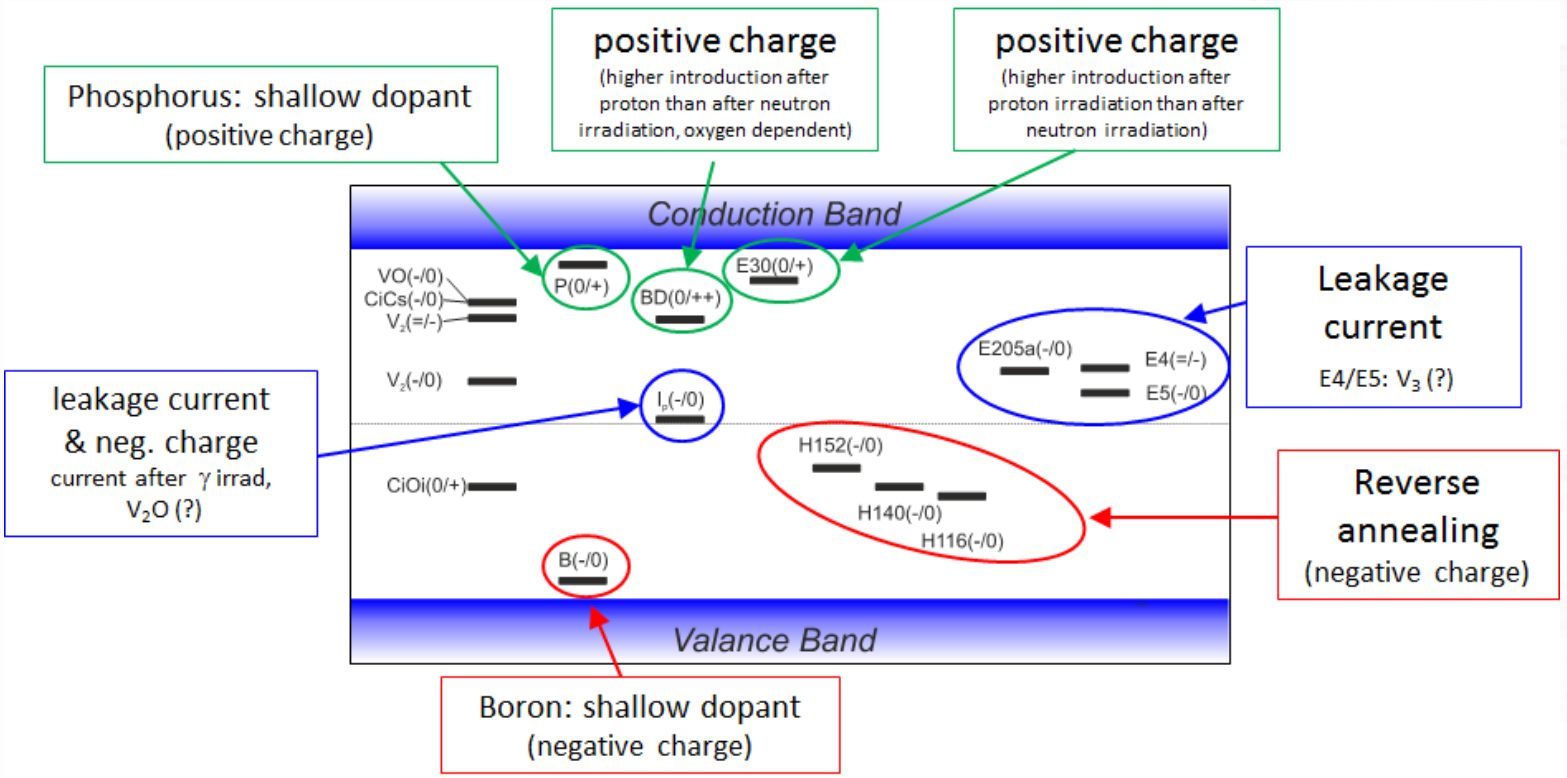


Reticle size (2x2 cm²)
Pixel pitch 20.7 µm
Array size: 928 x 960
Integration time: 185.6 µs
In pixel CDS
Sensors thinned to 50 µm
High Res Si option

Technology: AMS 0.35u
Design: IPHC

see: Giacomo Contin, "The STAR Pixel detector "

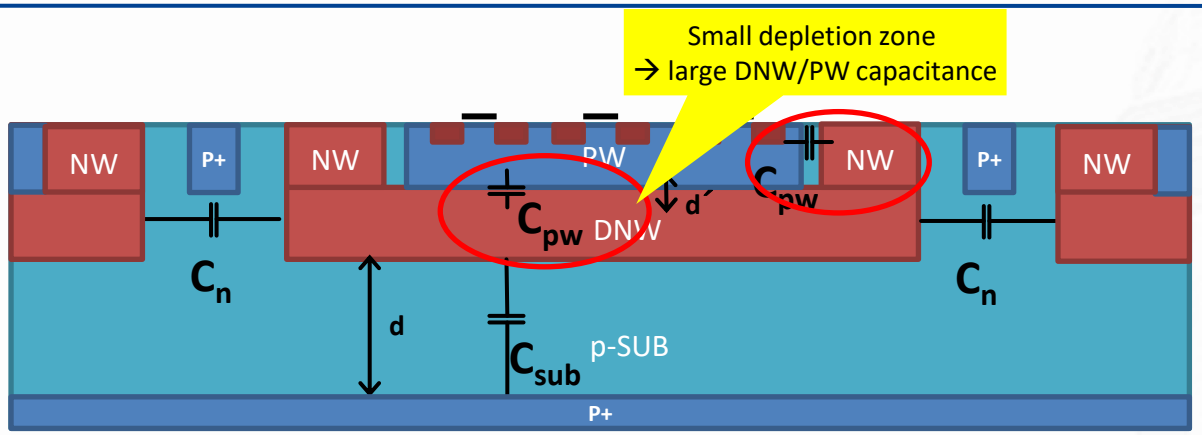
Trapping in irradiated silicon (NIEL)



RD50

Need to be as fast as possible!

Detector Capacitance



Large Fill Factor collecting node has a double junction: DNW/SUB and DNW/PW

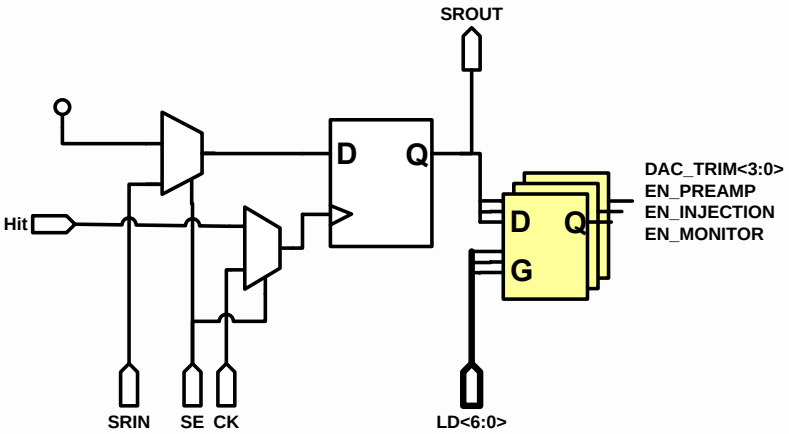
- Backplane capacitance C_{sub} (DNW to substrate)
  - Depends on depletion depth (substrate resistivity, bias voltage)
- Inter-pixel capacitance C_n
  - Depends on fill factor and p-implant ('p-stop') geometry

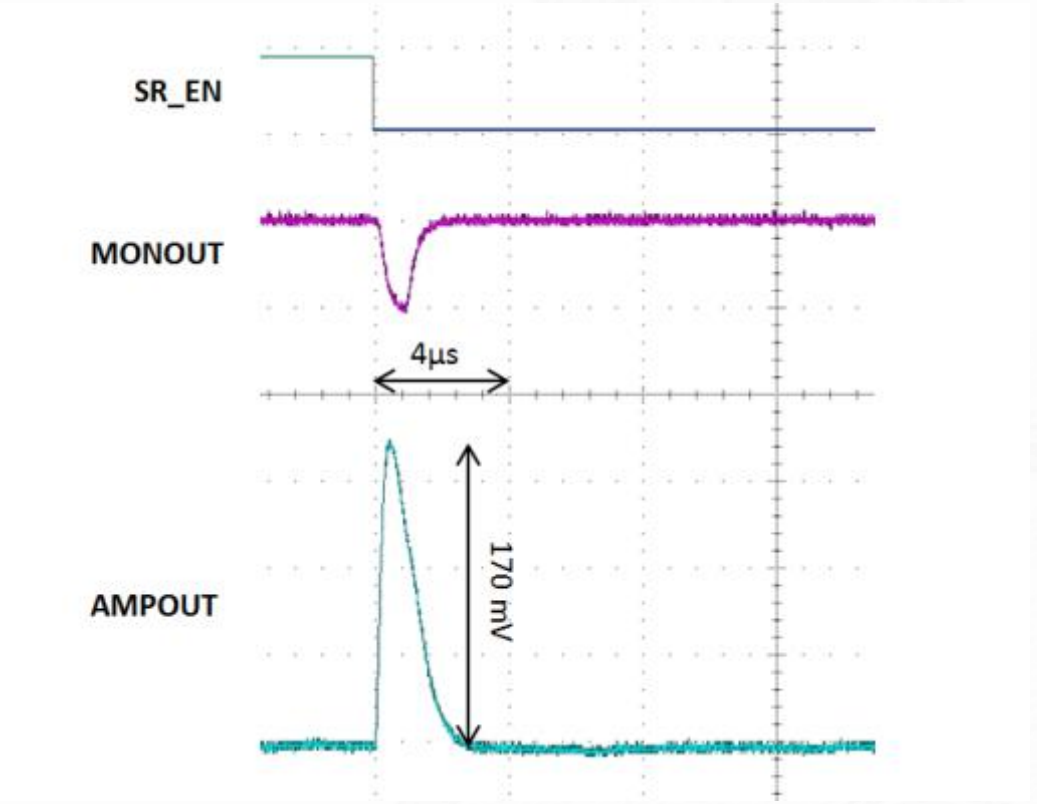
} same as for std. Hybrid Pixels

- DNW to P-well capacitance C_{pw}
  - Depends on **electronics circuit area** and **DNW/PW junction** width

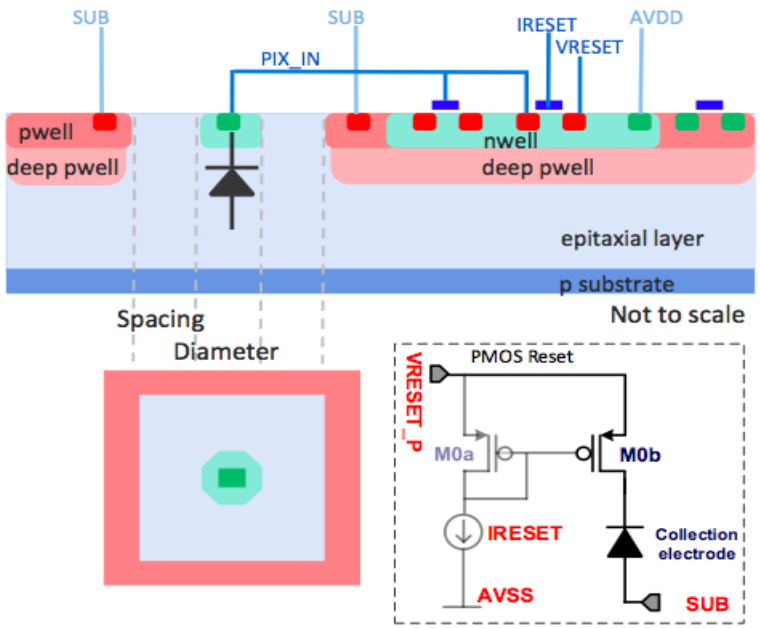
➔ additional capacitance for Active Pixels

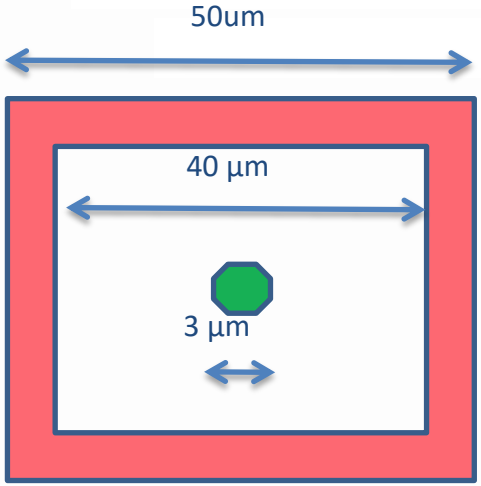
LF Noise


SROUT
Hit
D
Q
D
Q
G
DAC_TRIM<3:0>
EN_PREAMP
EN_INJECTION
EN_MONITOR
SRIN
SE
CK
LD<6:0>


SR_EN
MONOUT
4µs
AMPOUT
170 mV

TowerJazz 180nm Investigator





- **Pixel dimensions for these measurements:**
- 50x50um pixel size
- **3 µm diameter electrodes** and 40um Pwell opening
- 25um EPI layer

Designed as part of the ALPIDE development for the ALICE ITS upgrade

Emphasis is on small fill-factor and small capacitance

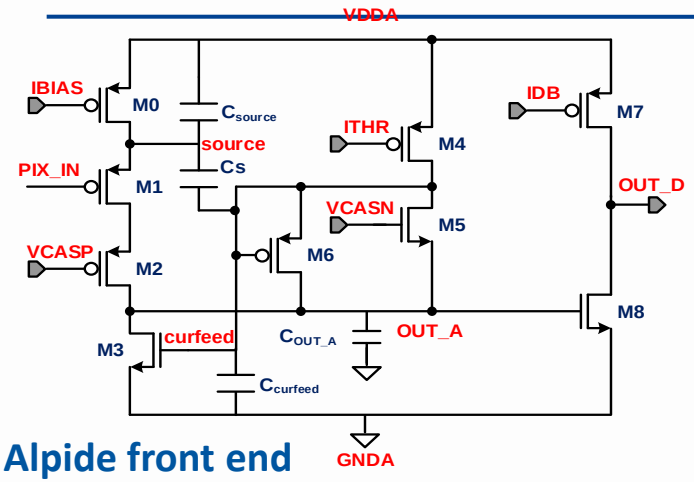
Small capacitance enables low analog power designs (and material reduction in consequence)

The pixels have a measured capacitance <5fF (approximately factor 20 less than large fill-factor pixel)

C. Gao et al., NIM A (2016) 831
http://www.sciencedirect.com/science/article/pii/S0168900216300985

Design: C. Gao, P. Yang, C. Marin Tobon, J. Rousset, T. Kugathasan and W. Snoeys
Measurements: C. Riegel, D. Schaefer, E. Schioppa, H. Pernegger, J. Van Hoorne

Impact of smaller capacitance



Alpide front end

D. Kim et al. TWEPP 2015

- Increased current in a similar front end from 20nA (Alpide) to 200 nA (= 50 mW/cm^2 for 28 µm pitch) and varied detector capacitance between 0.25 fF, 2.5 fF and 25 fF.
- For 2.5 fF compatible with 25 ns timing.

- Reducing the detector capacitance **increases amplitude and faster signal,** therefore less amplification is necessary
- This can be used to **reduce power consumption** (and therefore services and cooling material)