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Module and electronics developments for the ATLAS ITK pixel system

The entire tracking system of the ATLAS experiment will be replaced during the LHC Phase II shutdown around 2025 by an all-silicon detector (Inner Tracker, ITk).

The pixel detector will be composed by the five innermost layers, instrumented with new sensor and readout electronics technologies to improve the tracking performance and cope with the severe HL-LHC environment in terms of occupancy and radiation. The total area of the new pixel system could measure up to 14 m^2 , depending on the final layout choice that is expected to take place in early 2017

Different designs of planar, 3D, CMOS sensors are being investigated to identify the optimal technology for the different pixel layers. In parallel sensor-chip interconnection options are evaluated in collaboration with industrial partners to identify reliable technologies when employing 100-150 μm thin chips.

While the new read-out chip is being developed by the RD53 Collaboration, the pixel off detector read-out electronics will be implemented in the framework of the general ATLAS trigger and DAQ system. A readout speed of up to 5 Gb/s per data link (FE-chip) will be needed in the innermost layers going down to 640 Mb/s for the outermost. Because of the very high radiation level inside the detector, the first part of transmission has to be implemented electrically with signals to be converted for optical transmission at larger radii.

Extensive tests are being carried out to prove the feasibility of implementing serial powering chosen as the baseline for the ITK pixel system, given the reduced material in the servicing cables foreseen for this option.

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