The performance measurements of INTPIX6 SOI pixel detector

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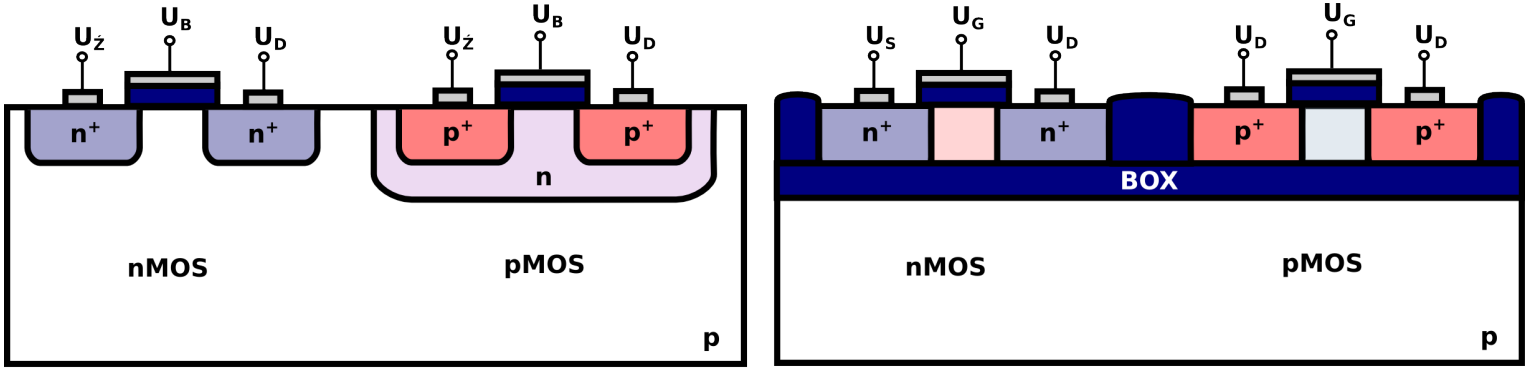
Outline

SOI Technology - short overview

Silicon-On-Insulator

SOI is CMOS technology, which implements an insulator layer between handle wafer and epitaxial layer.



a) MOS transistors in standard bulk CMOS

b) MOS transistors in standard SOI CMOS

FOR ELECTRONICS:

- reduction of parasitic capacitances → power saving, higher speed,
- reduction of leakage currents → power saving,
- elimination of latch-up effects,
- better resistivity for Single Event Upsets
- smaller area - no guard rings,

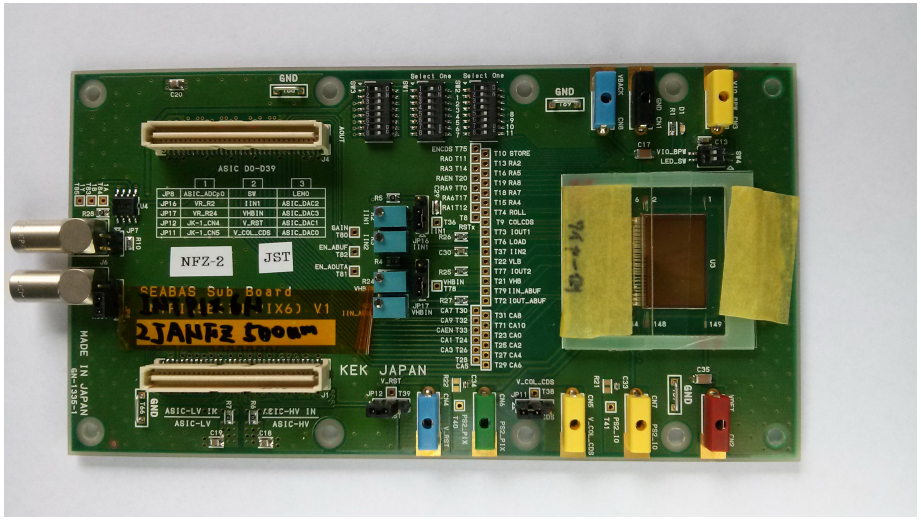
FOR SENSORS:

- **Possibility of designing monolithic pixel detectors**
- Pitch down to few μm
- Small sensor capacitance (good SNR)
- Double SOI → may improve radiation hardness
- Wide temperature range $(4 - 400K)$
- Cheaper then hybrid

INTPIX6 - detector overview

INTPIX6

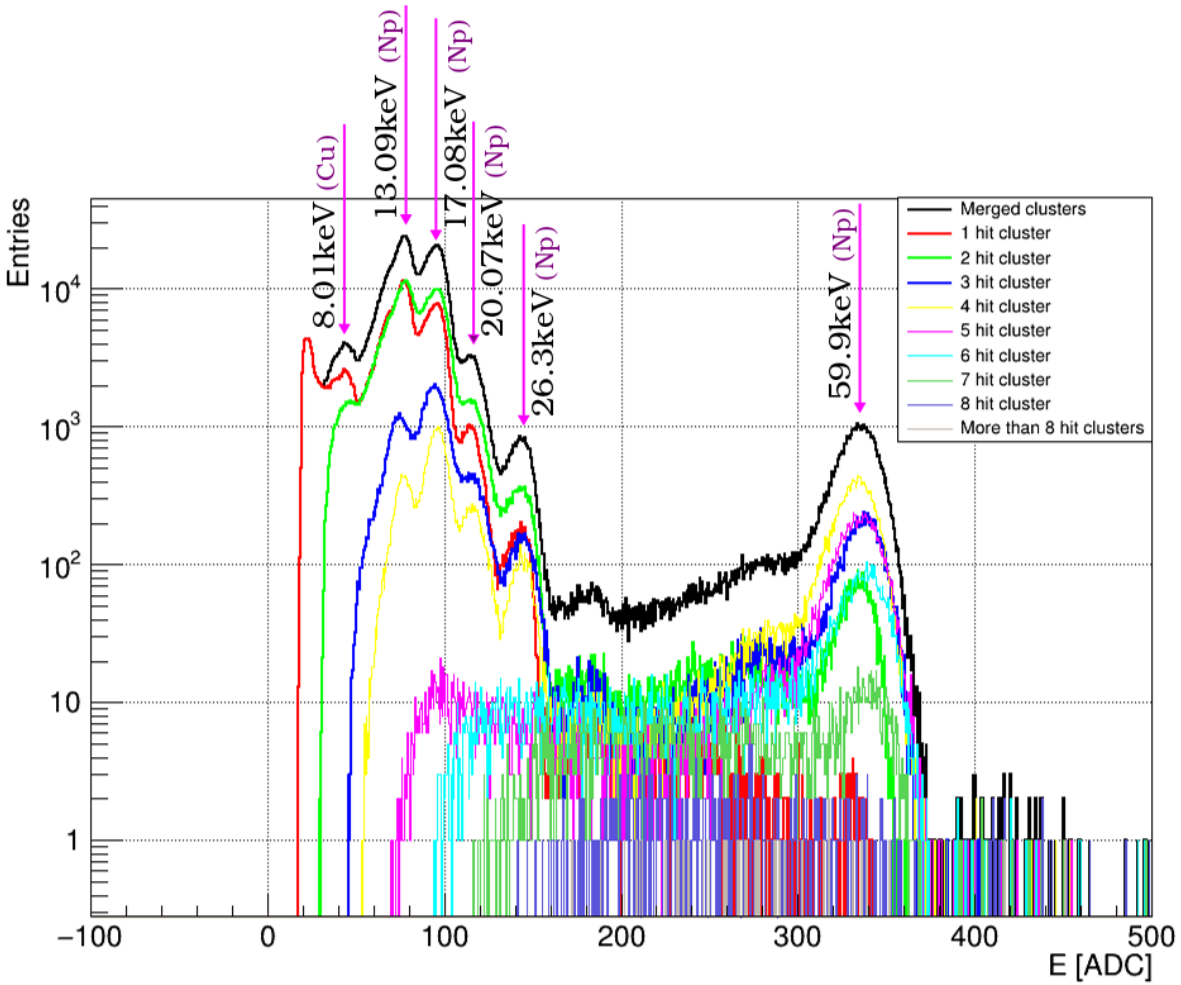
Large format integrating type sensor designed in 200nm Lapis SOI by group from KEK.

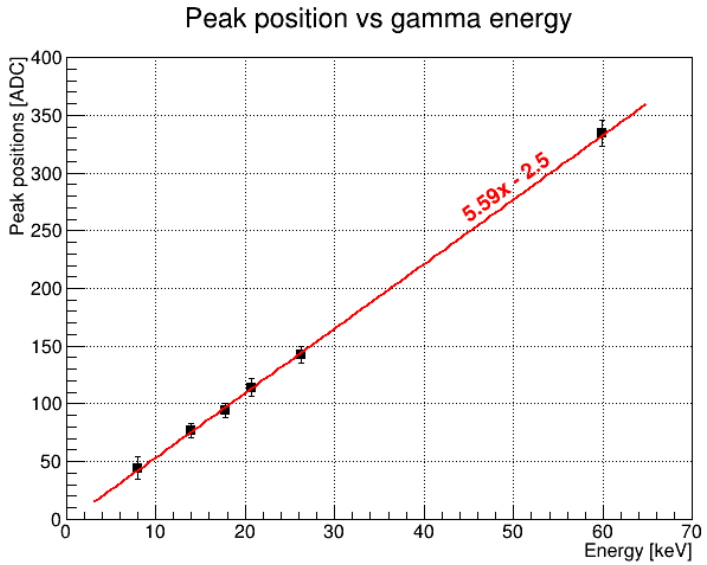


- available on various wafers (CZ(n), FZ(n), FZ(p))
- architecture based on source-follower
- 1408×896 pixel matrix, 12 × 12 μm^2 pixel size
- 11 parallel analog outputs
- rolling shutter readout mode

241-Am measurements for CZ(n) sensor

241-Am measurements - CZ(n) sensor



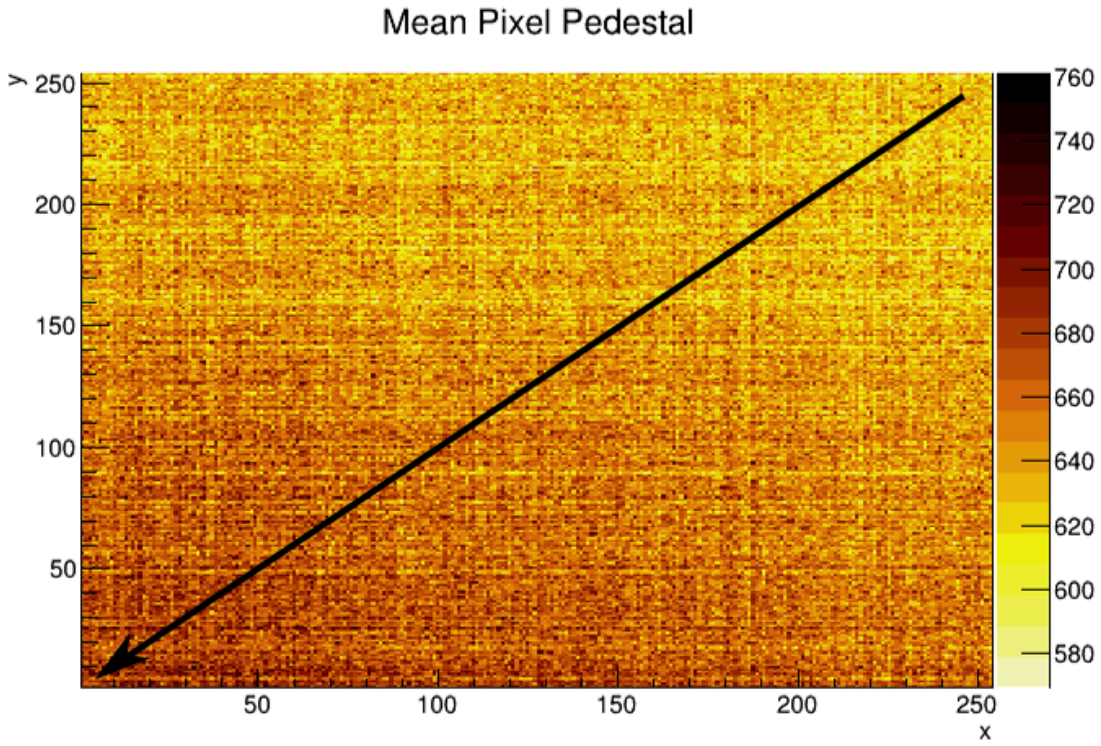


- measurements in room temperature
- mainly 1-2 hit clusters
- linear up to 60 keV

Pixel noise: ENC = 70.2 e^-

55-Fe measurements for FZ(n) sensor

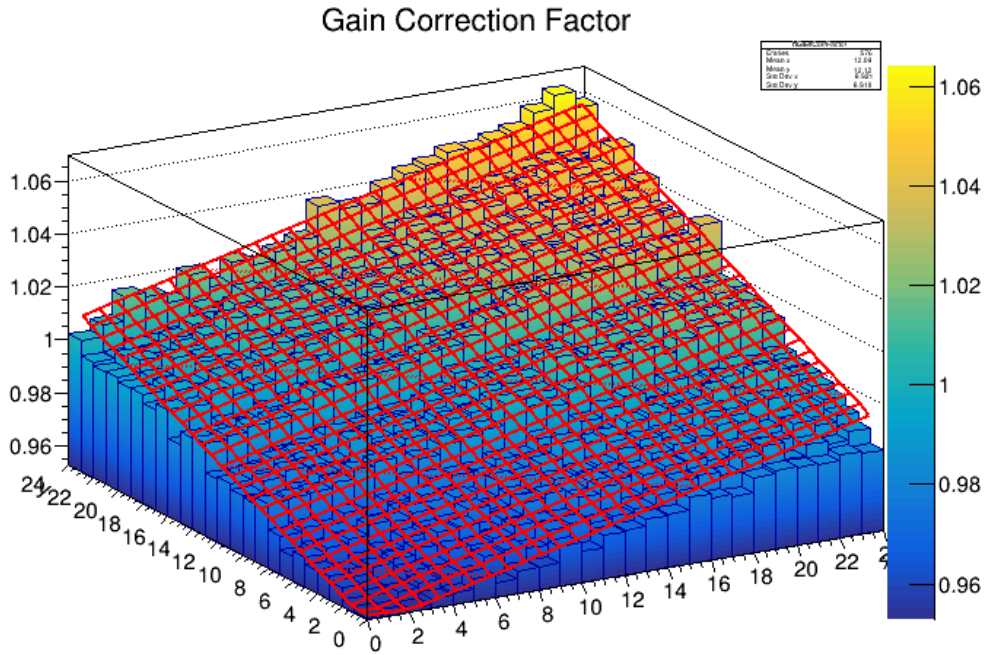
Gain variations - FZ(n)

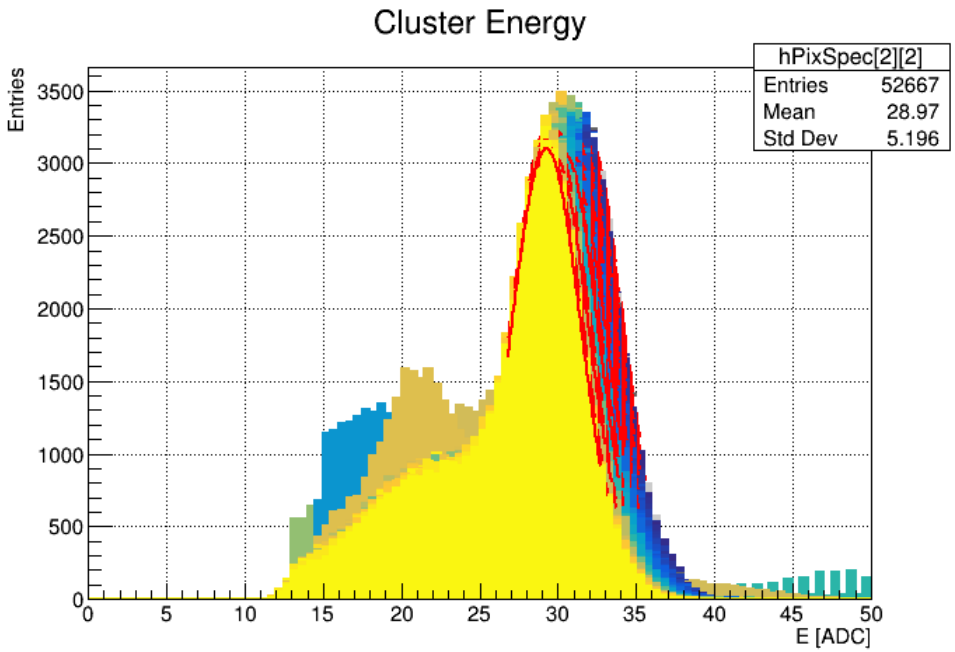


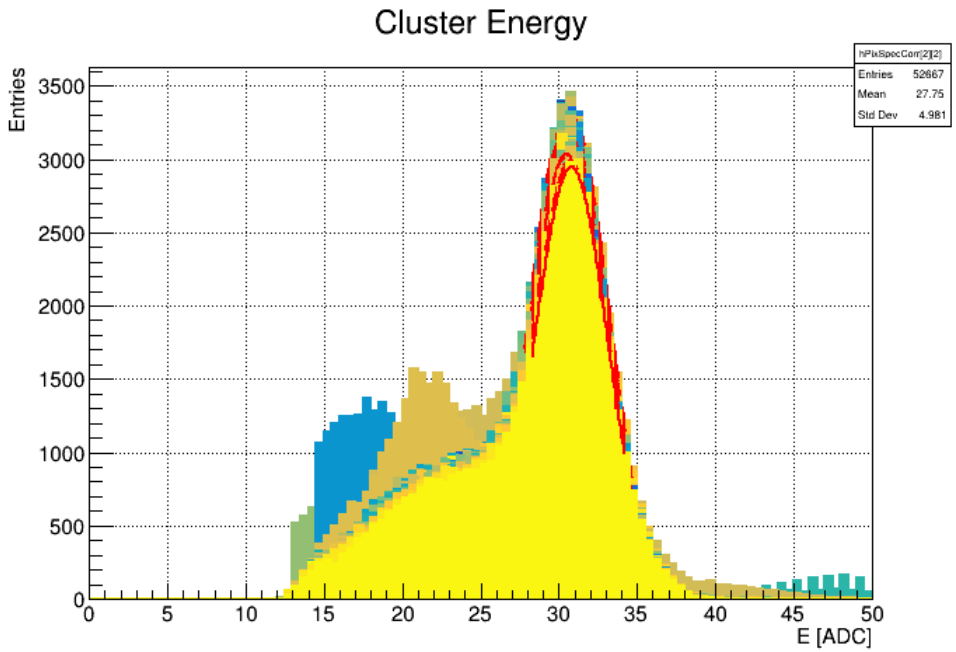
- Probably there is some leakage: the longer we wait to read the pixel, the lower pedestal is observed
- Affects not only pedestal but also gain.

Gain correction

- Having gain for 10×10 pixel blocks we estimate gain correction factor for the whole matrix
- After including the correction factor the spread of peak position was eliminated

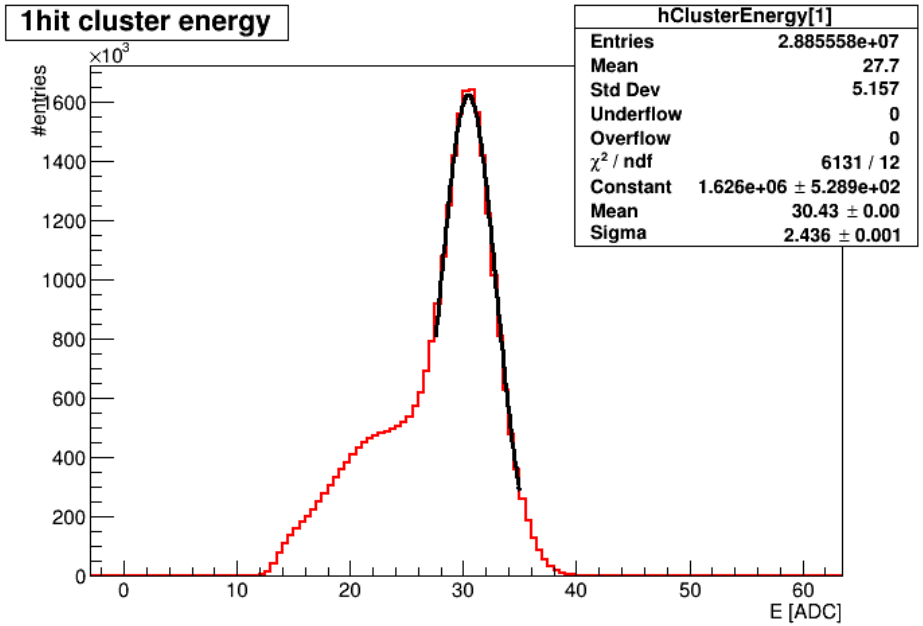






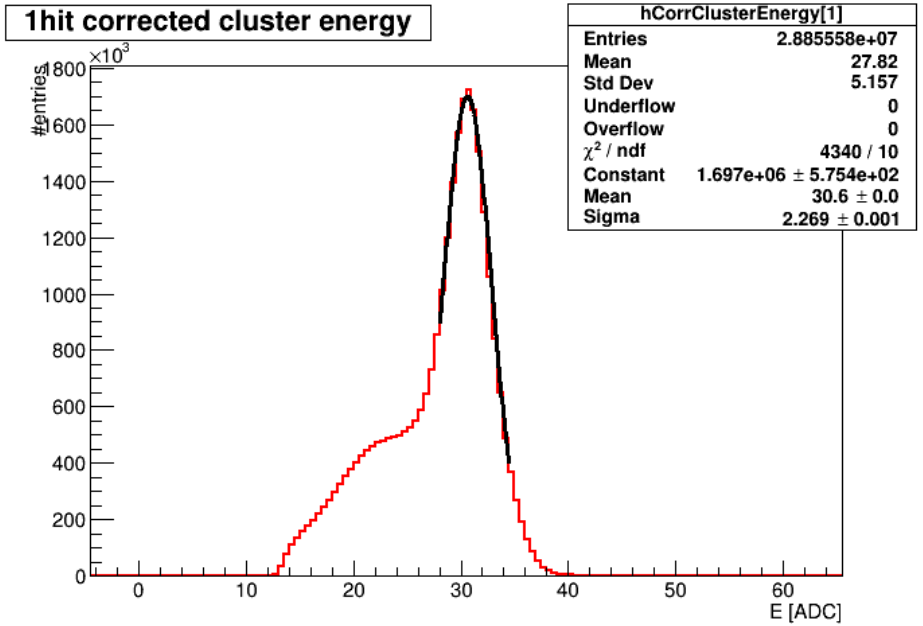
Iron spectrum - results

BEFORE CORRECTION



$\sigma_{bc} = 2.44$ [ADC]

AFTER CORRECTION



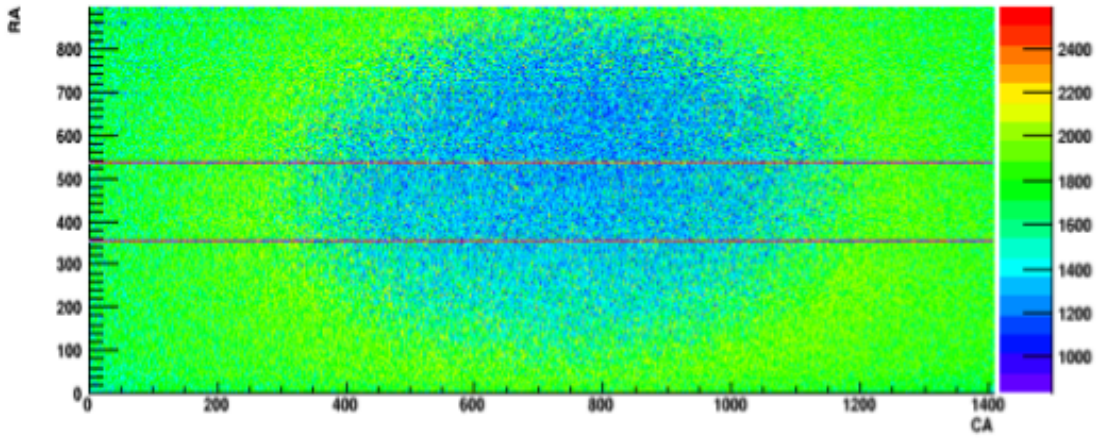
$\sigma_{ac} = 2.27$ [ADC]

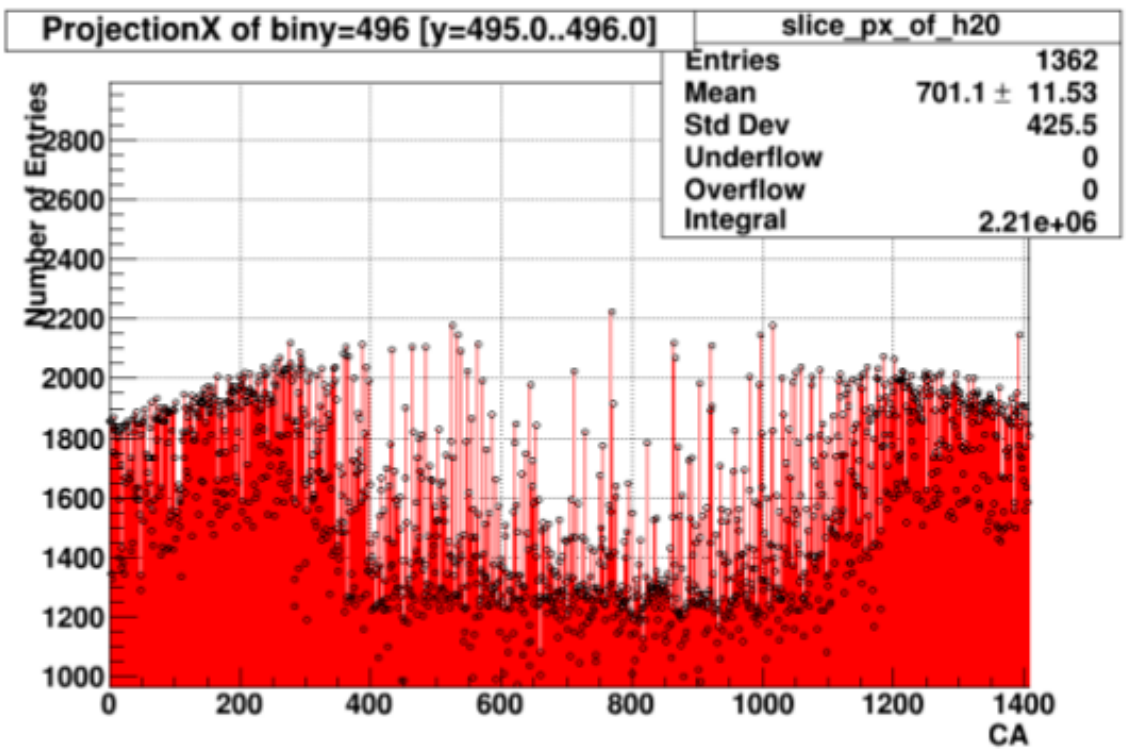
The noise ENC:

from pixel fluctuations: $\approx$ **70 e$^-$.**
from peak width: $\approx$ **100 e$^-$.**

radiation hardness

Pedestal after irradiation





High dose is obtained irradiating the chip with high intensity (425 MBq) 55-Fe Xray source.

- The plots show pedestal after irradiation at 60 krad dose.
- The visible pattern is due to the X-ray source size.

Dose in SiO_2 recalculation

From the data analysis we know the number of hits in detector. From this value the BOX-dose can be calculated.

$$\Delta I_n = I_{n+1}(e^{\frac{x_{BOX}}{x_0}} - 1)$$

$$\Delta I_n = 7 \ \frac{particles}{\mu s} \cdot (e^{\frac{0.2\mu m}{55\mu m}} - 1)$$

$$\Delta I_n = 0.14 \ \frac{particles}{\mu s}$$

Mass and dose recalculation:

$$D = \frac{\Delta I \cdot E_\gamma \cdot t}{m}$$

$$m = 2830\mu m \cdot 2830\mu m \cdot 0.2\mu m \cdot \rho = 3.7 \ nkg$$

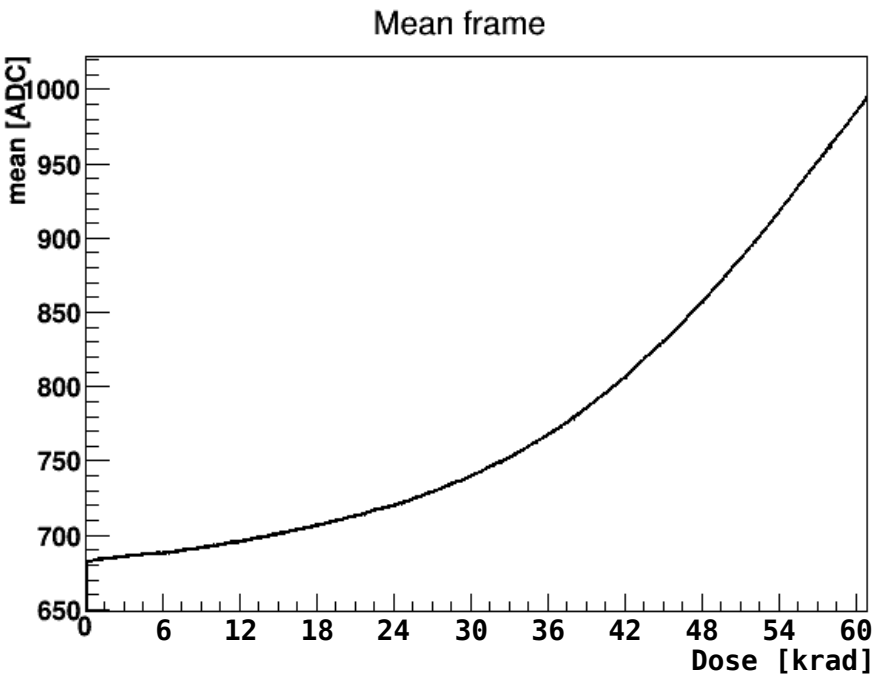
$$D = 60 \ krad \ (24 \ h)$$

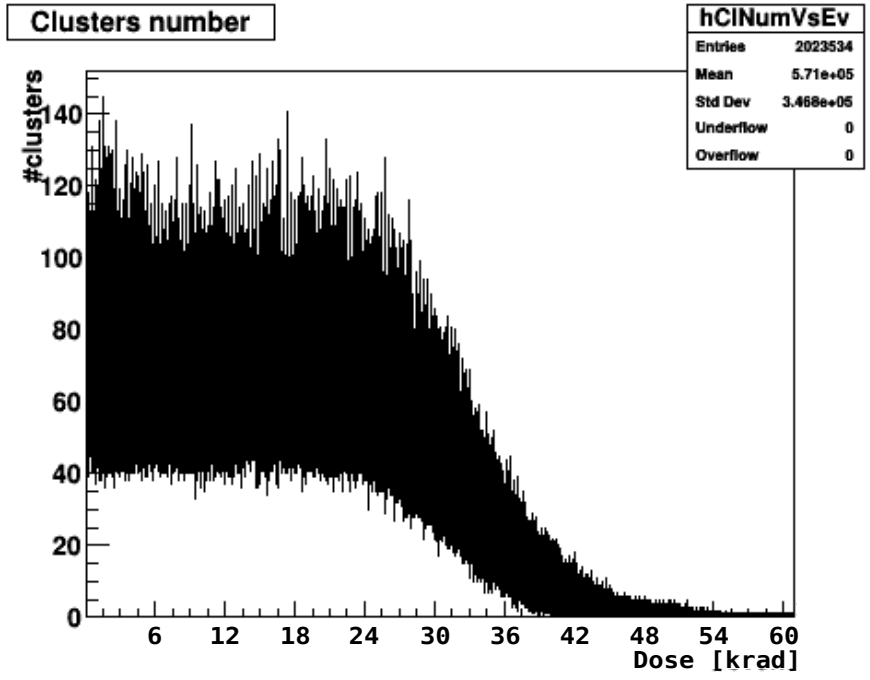
Final dose

The dose after 24h is:

$$D = 60 \ krad$$

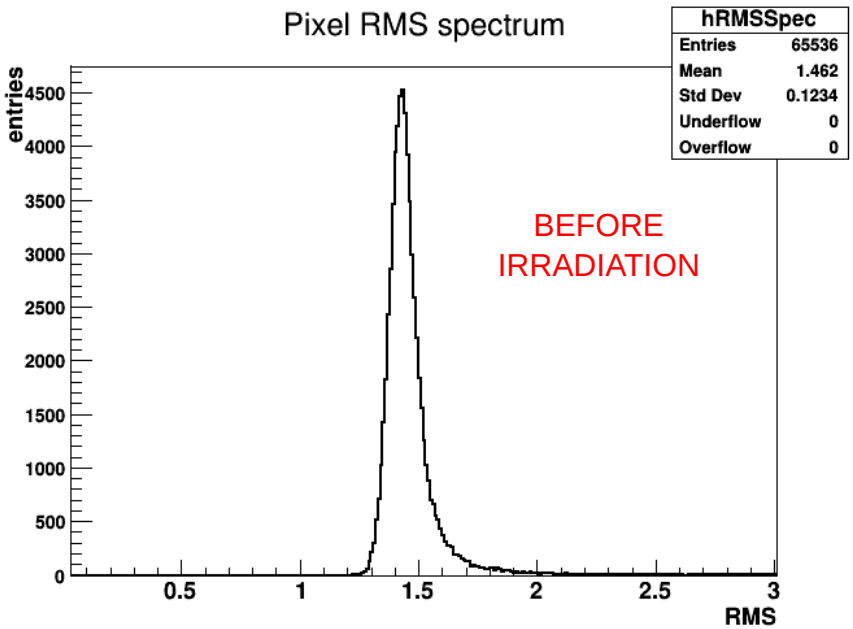
Data analysis from irradiated detector

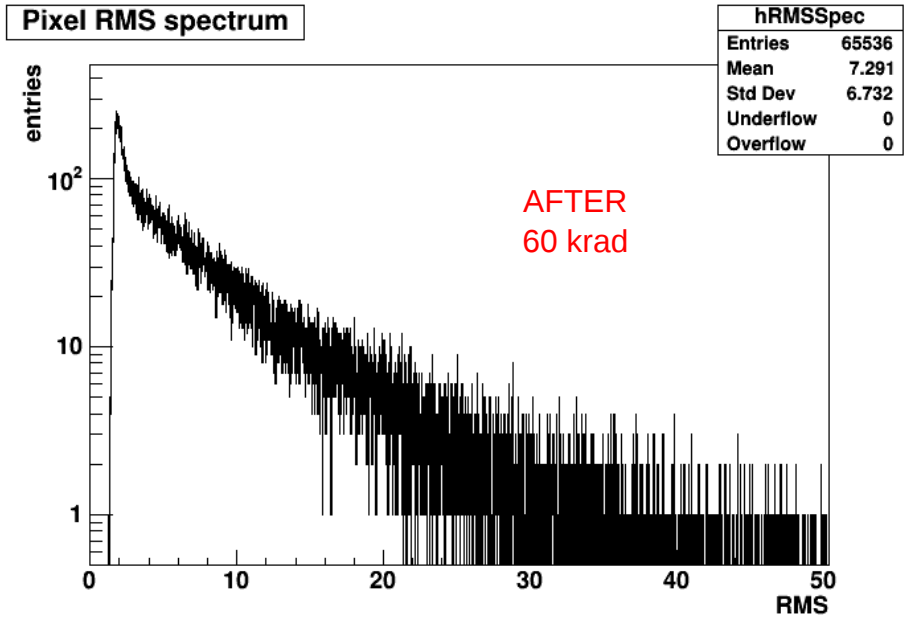


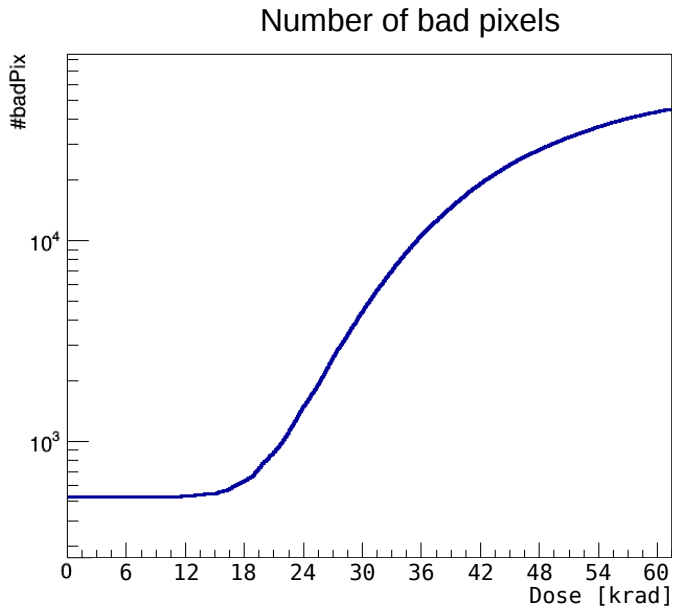


- Up to ∼30 krad detector works properly
- Above ∼30 krad the efficiency drops but energy resolution remains on the same level

Data analysis from irradiated detector

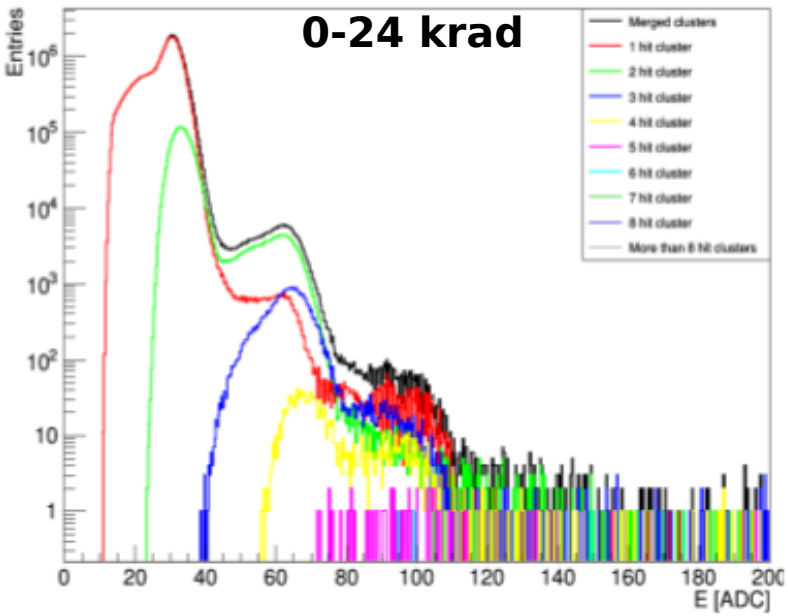


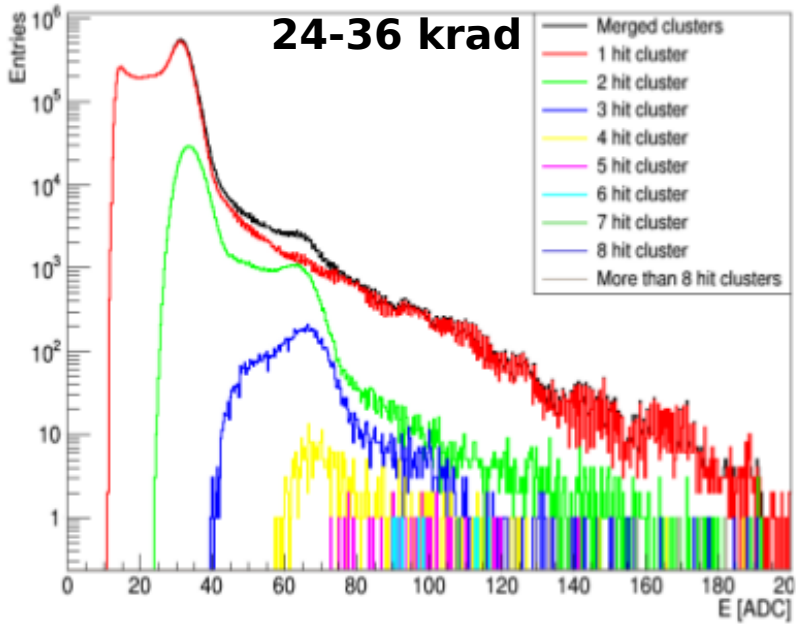


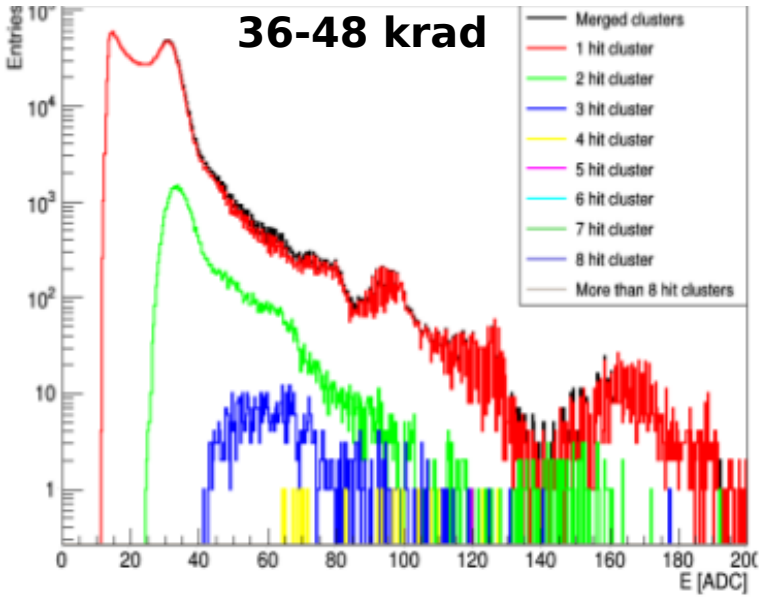


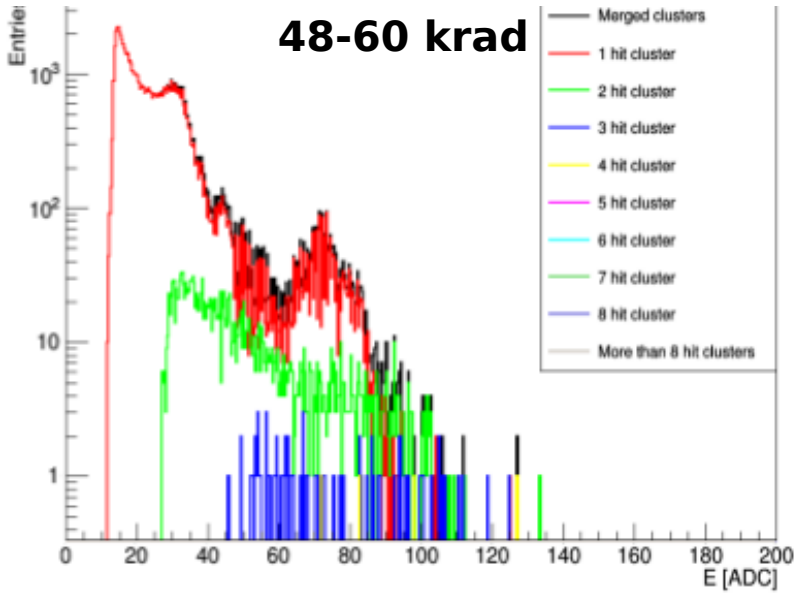
- The pixel RMS spectrum after irradiation changes because more pixels pass the criteria for bad pixel
- Up to ∼30 krad number of bad pixels below 1%
- Above ∼30 krad number of bad pixels (highly fluctuating) is rapidly increasing

Iron spectrum during irradiation

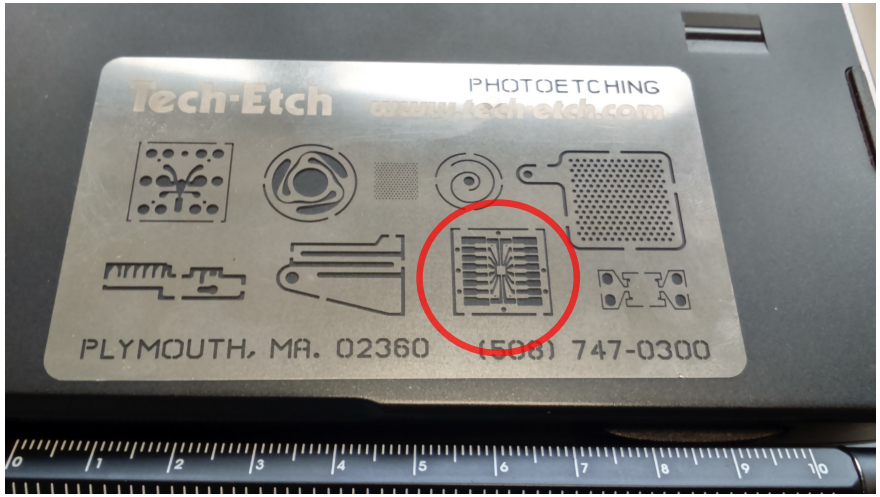


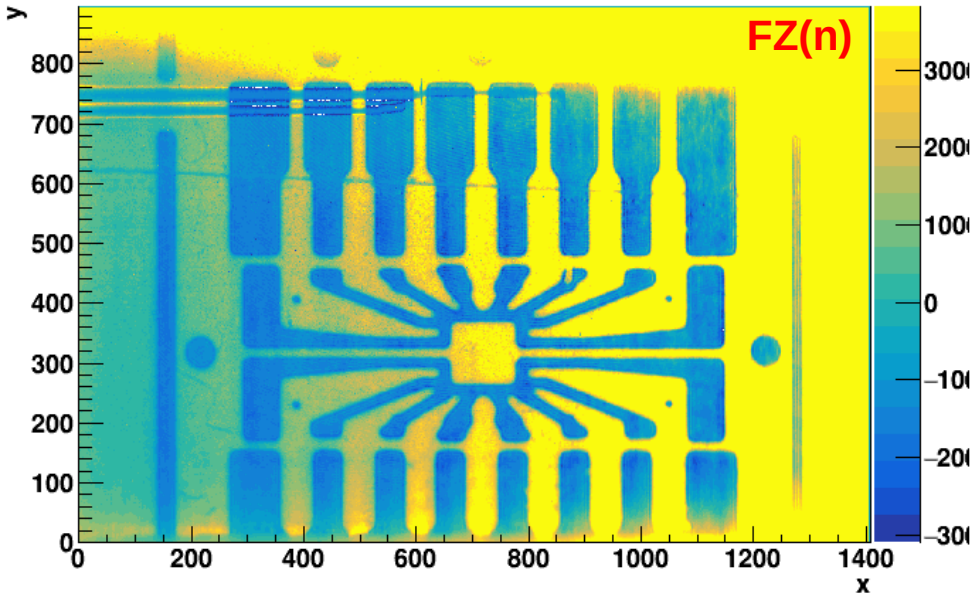


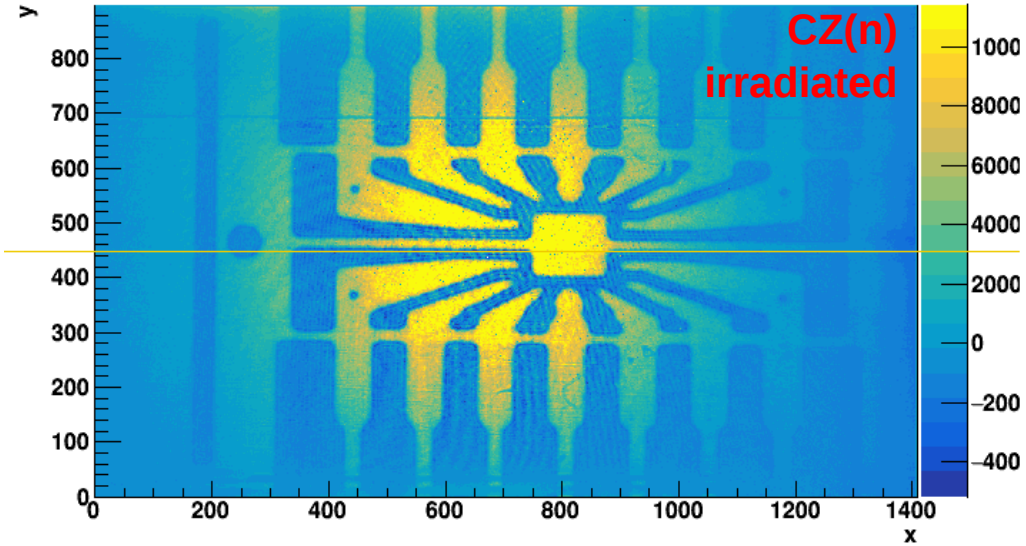




Patterns







- defocused laser 1060 nm
- average of 100 frames
- **pattern visible even after 60 krad irradiation on CZ(n)**

Summary

- Large (1408×896) INTPIX6 SOI detector with very small ($12\times12\mu m^2$) integrating type pixels is fully functional
- ENC of about 70 electrons ($100e^-$ from FWHM) is obtained at room temperature
- The detector is operating up to at least 60 krad dose
- Good S/N ratio is maintained up to 30 krad
- For higher doses S/N decreases and number of bad pixels increases rapidly, however the imaged pattern is seen well
- **With recent modification in SOI transistor LDD dose and introduction of double SOI wafer, radiation tolerance more than 10 Mrad is foreseen now.**