ALPIDE: the Monolithic Active Pixel Sensor for the ALICE ITS upgrade

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on behalf of ALICE collaboration

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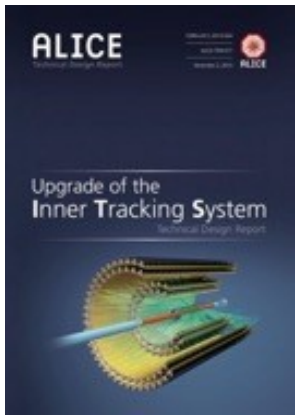
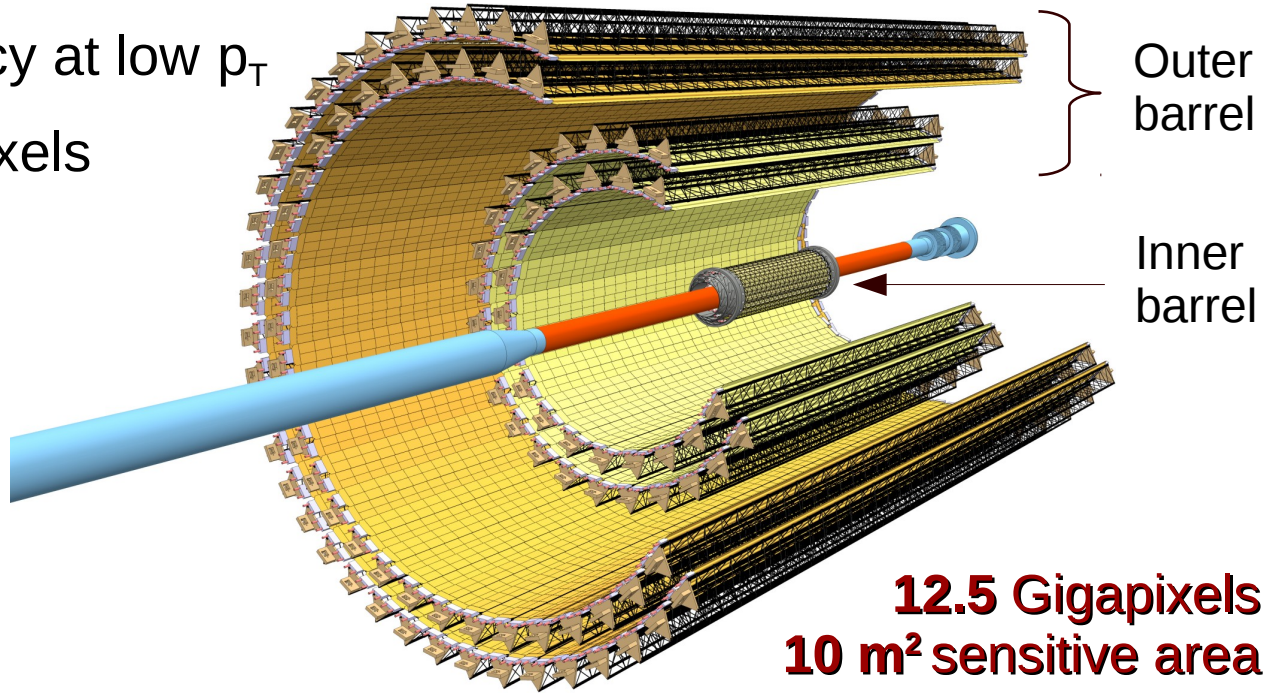
Inner Tracking System upgrade

- Aimed to replace ALICE ITS during the LHC Long Shutdown 2 in 2019/20
- Increase readout speed → Readout Pb-Pb collisions at 100 kHz
- Improve impact parameter resolution
  - Reduce pixel size: O(50 x 425 μm^2) → O(30 x 30 μm^2)
  - Reduce distance from the IP: 39 mm → 23 mm
- Reduce inner layers X_0: ~1.14% → ~0.3%
- Improve tracking efficiency at low p_T
- All 7 layers with binary pixels



TDR approved (2014)



12.5 Gigapixels
10 m^2 sensitive area

ITS requirements

Parameter	Inner Barrel	Outer Barrel	ALPIDE
Chip size	15 mm x 30 mm		✔
Chip thickness	50 µm	100 µm	✔
Spatial resolution	5 µm	10 µm	~5 µm
Detection efficiency	> 99 %		✔
Fake hit rate	< 10^{-6} pixel^{-1} event^{-1}		<<< 10^{-6} pixel^{-1} event^{-1}
Integration time	< 30 µs		~ 2 µs
Power density	< 300 mW cm^{-2}	< 100 mW cm^{-2}	< 40 mW cm^{-2}
TID radiation hardness*	2700 krad	100 krad	Tested at 350 krad
NIEL radiation hardness*	1.7×10^{13} 1MeV n_{eq} cm^{-2}	10^{12} 1MeV n_{eq} cm^{-2}	✔

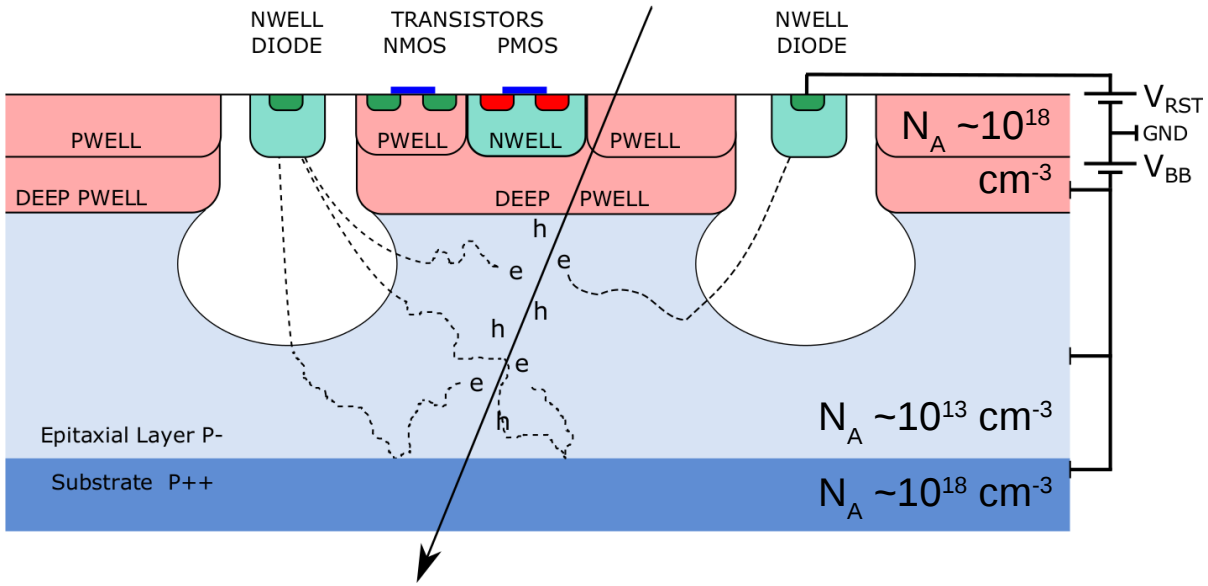
* This includes a safety factor of ten.

For comparison STAR HFT ULTIMATE sensor:

- Integration time 190 µs
- Fake hit rate ~ 10^{-6}
- Power density 170 mW cm^{-2}
- Radiation environment up to 90 krad and 10^{12} 1MeV n_{eq} cm^{-2}

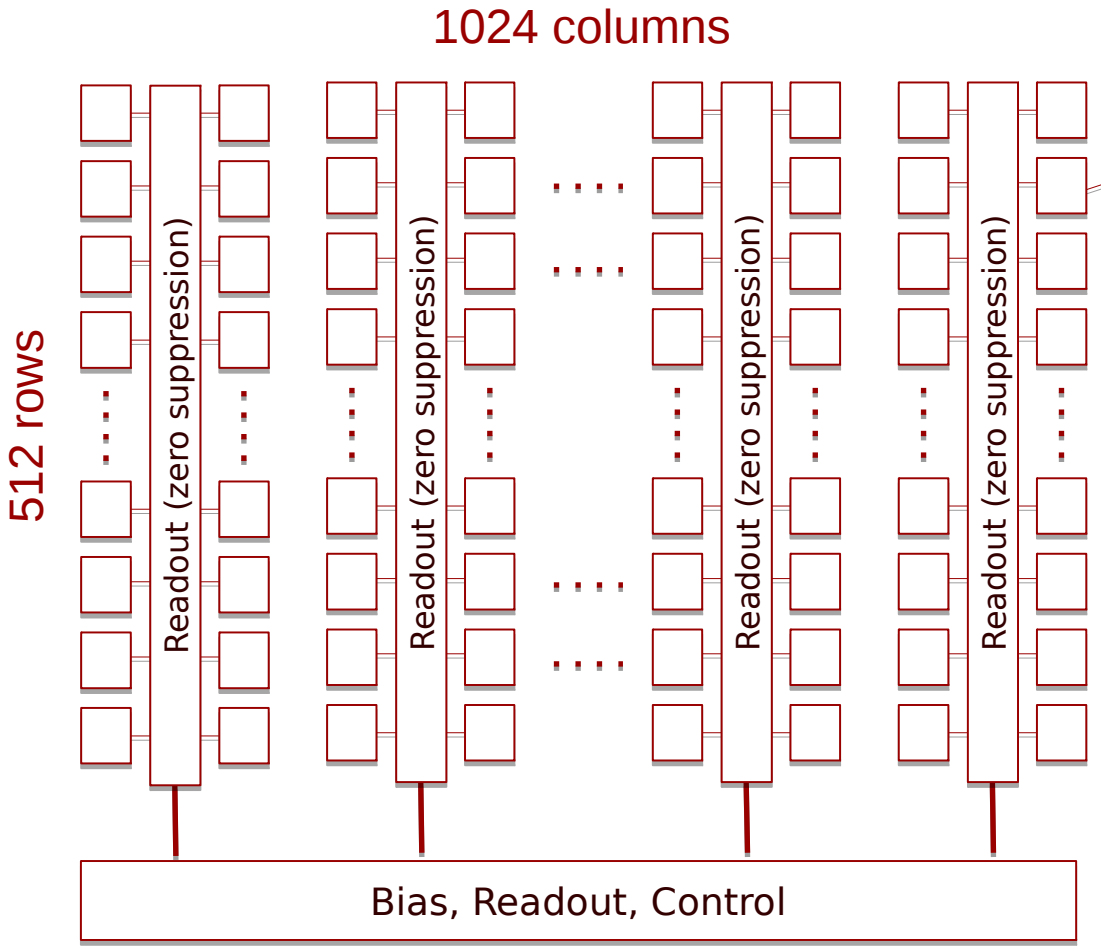
Technology

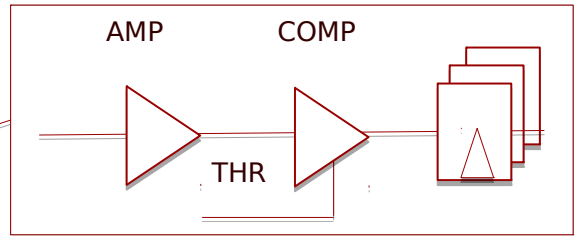
- TowerJazz 180 nm CMOS imaging sensor process
- Deep p-well shielding n-well allowing in-pixel PMOS
  - More complex in-pixel circuitry
- High-resistivity (> 1 kΩ cm) p-type epitaxial layer (18 to 30 µm) on p-type substrate
- Substrate bias → Increase of depletion volume



- Larger charge collected by seed pixel
- Lower input capacitance → better S/N ratio
- Short collection time
- Better non-ionising radiation tolerance

ALPIDE design



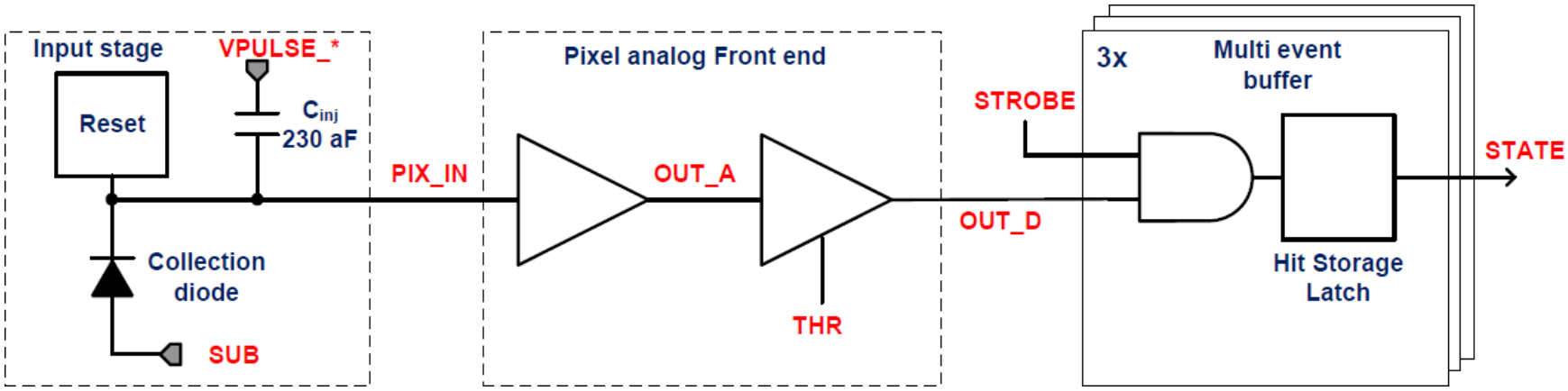


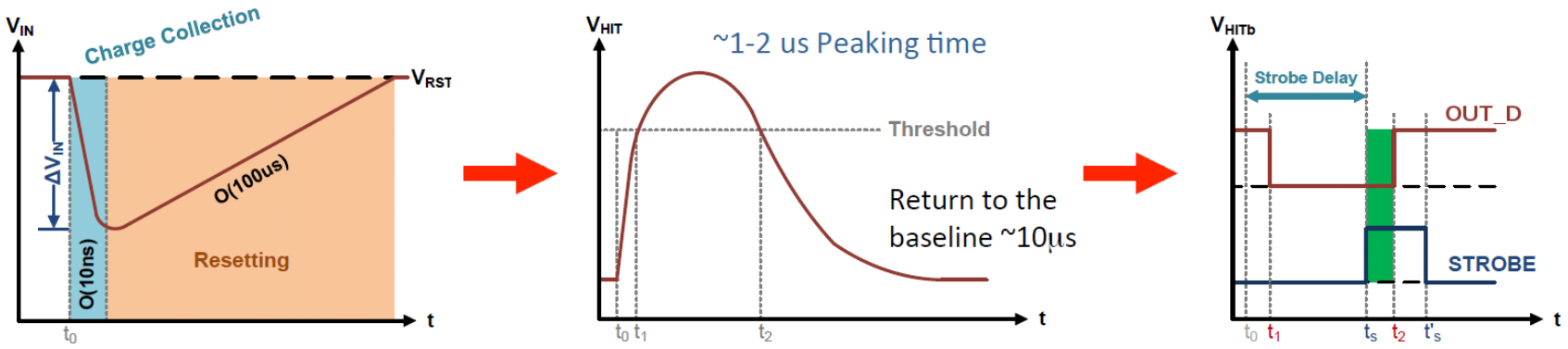
Features:

- In-pixel amplification
- In-pixel discrimination
- In-pixel multi event buffer
- In-matrix zero suppression (priority encoding)
- Triggered or continuous acquisition (global shutter)

Very low power front end ~40 nW/pixel
Total power consumption <40 mW/cm^2

Principle of operation

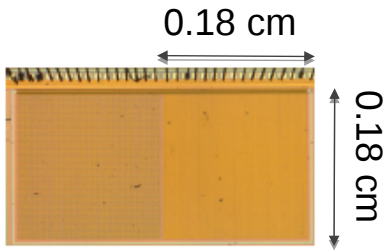




- Charge created in epitaxial layer is collected
- Signal is shaped and compared to threshold
- Signal is strobed into an in-pixel memory
- Hit pixels are read out asynchronously (priority encoding)

ALPIDE development

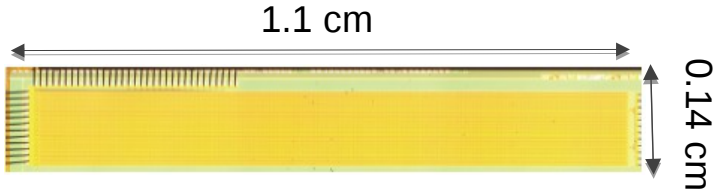
2012
Explorer
(analogue)



Pixels:

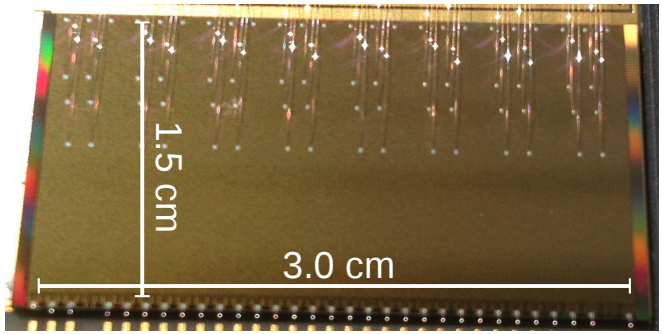
90 × 90 (20μm × 20μm)
60 × 60 (30μm × 30μm)

2013
pALPIDEss
(digital)



512 × 64 (22μm × 22μm)

May 2014
pALPIDE-1
(full scale)



512 × 1024 (28μm × 28μm)

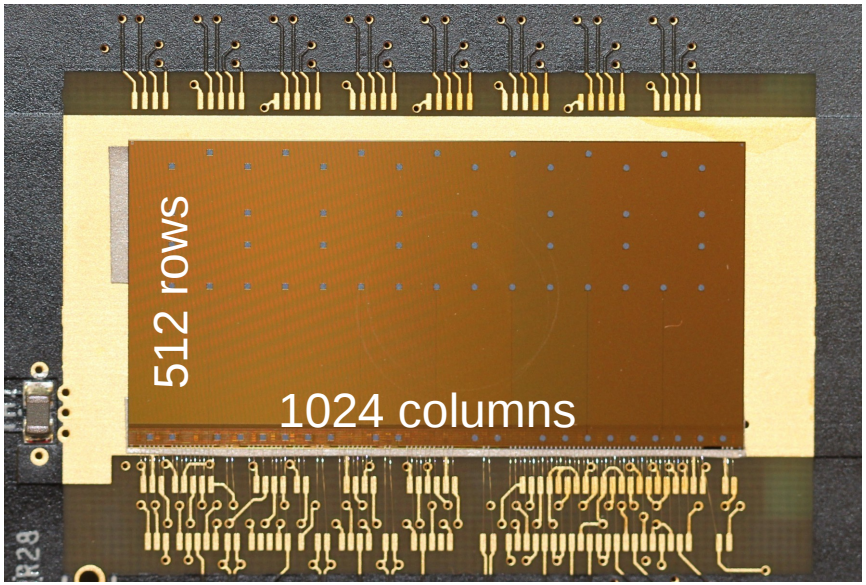
May 2015
pALPIDE-2
(full scale)

Oct 2015
pALPIDE-3
(full scale)

August 2016
ALPIDE
(final)

pALPIDE-3 specifications

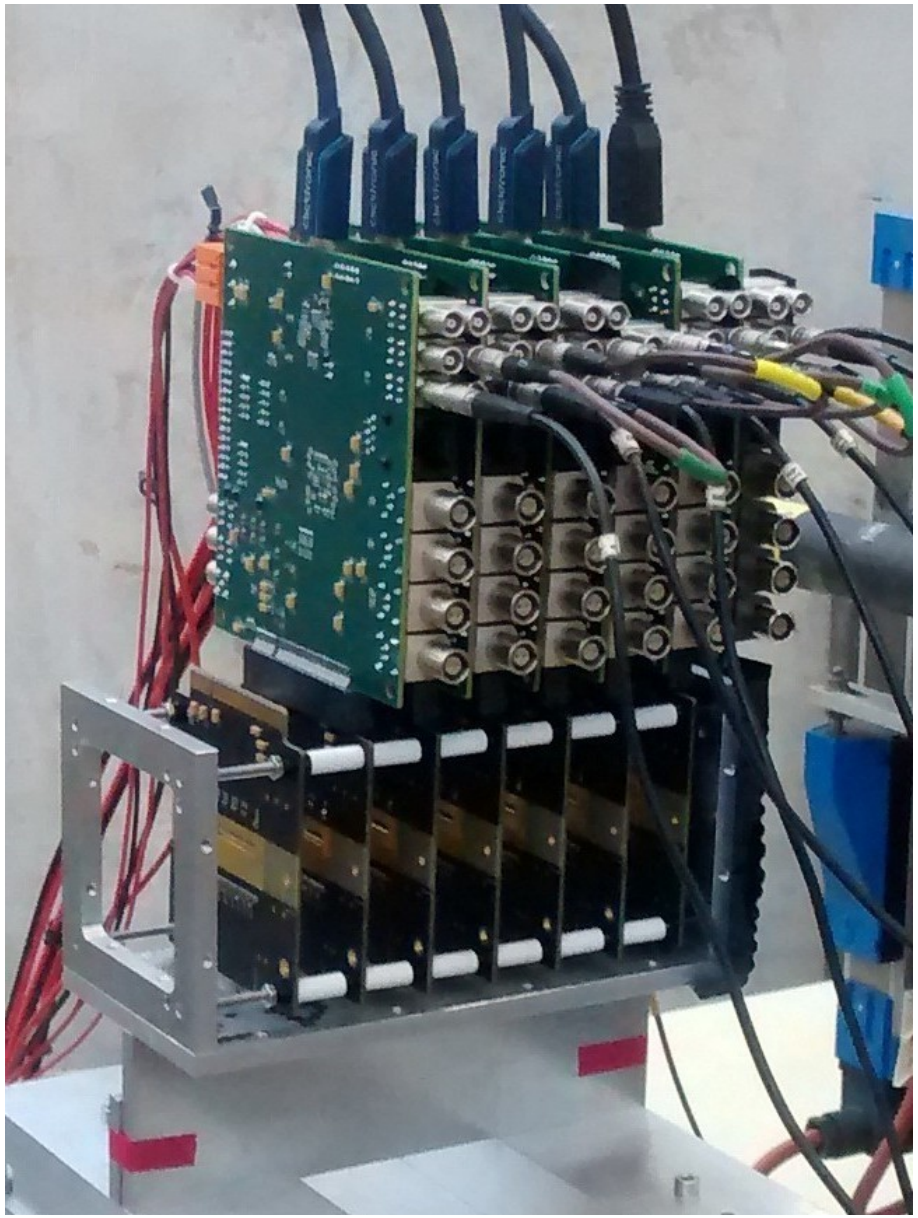
- Pixel pitch:
  - 29.24 x 26.88 μm²
- 8 pixel flavours
  - Different collection diodes and reset mechanisms
- Different epitaxial thickness
  - 18 μm, 25 μm and 30 μm



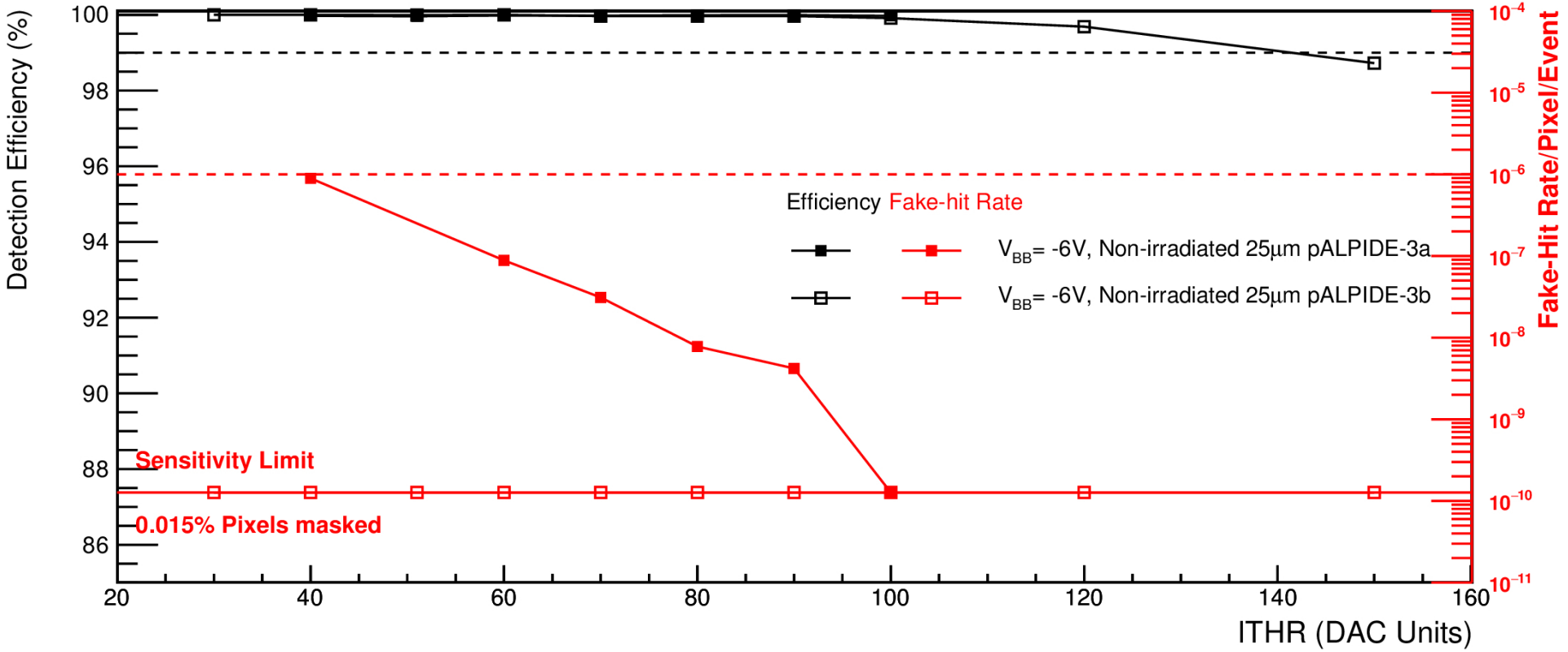
- 2 varieties of input transistor
  - pALPIDE-3a: W = 0.22 μm, L = 0.18 μm
  - pALPIDE-3b: W = 0.92 μm, L = 0.18 μm
  - Same noise level but different fake hit rate → RTS noise
  - Larger input transistor size reduces significantly RTS noise

Test beam results

- Test carried out using telescope made entirely of ALPIDE prototypes
- Campaigns at PS (CERN), BTF (Frascati), DESY (Hamburg), Pohang (Korea) and SLRI (Thailand)
- Measured performance:
  - Different varieties of pALPIDE-3 (a & b)
  - Before and after both ionising and non-ionising radiation

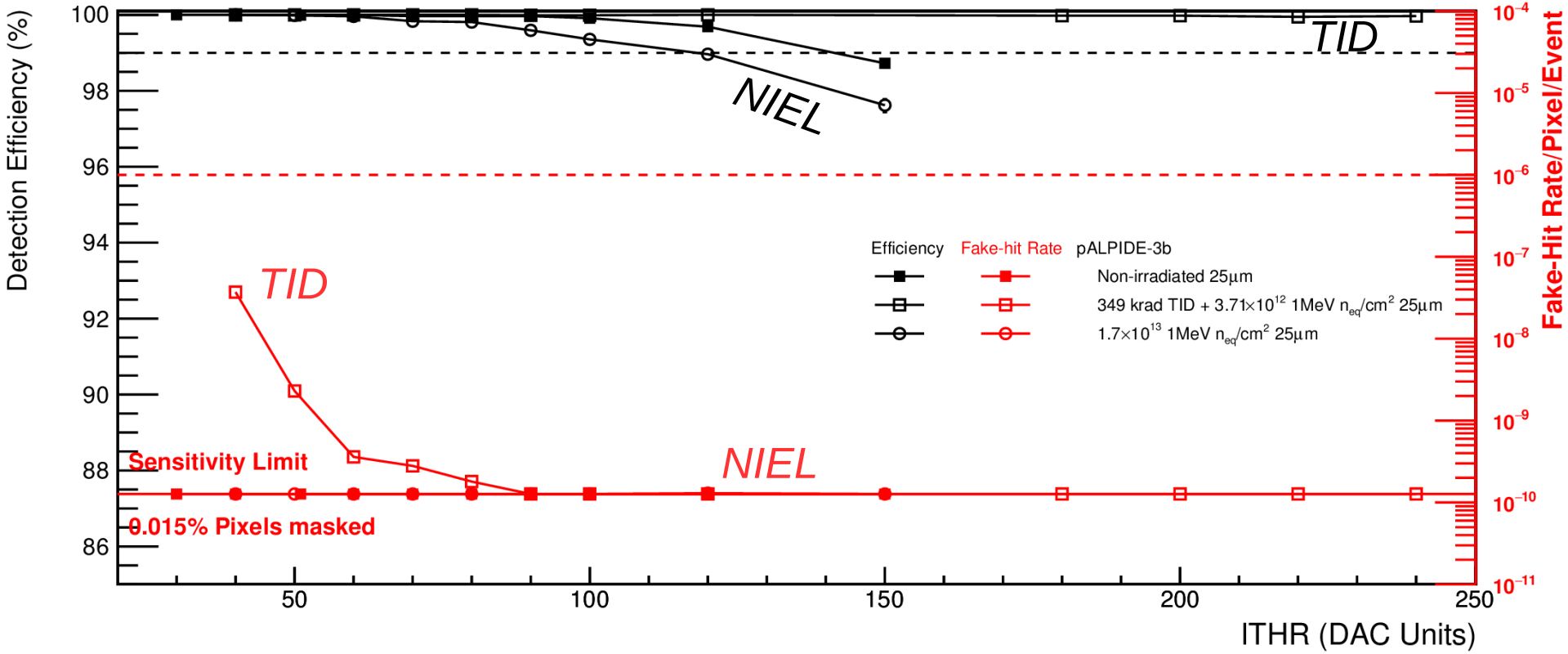


Efficiency and fake hit rate I



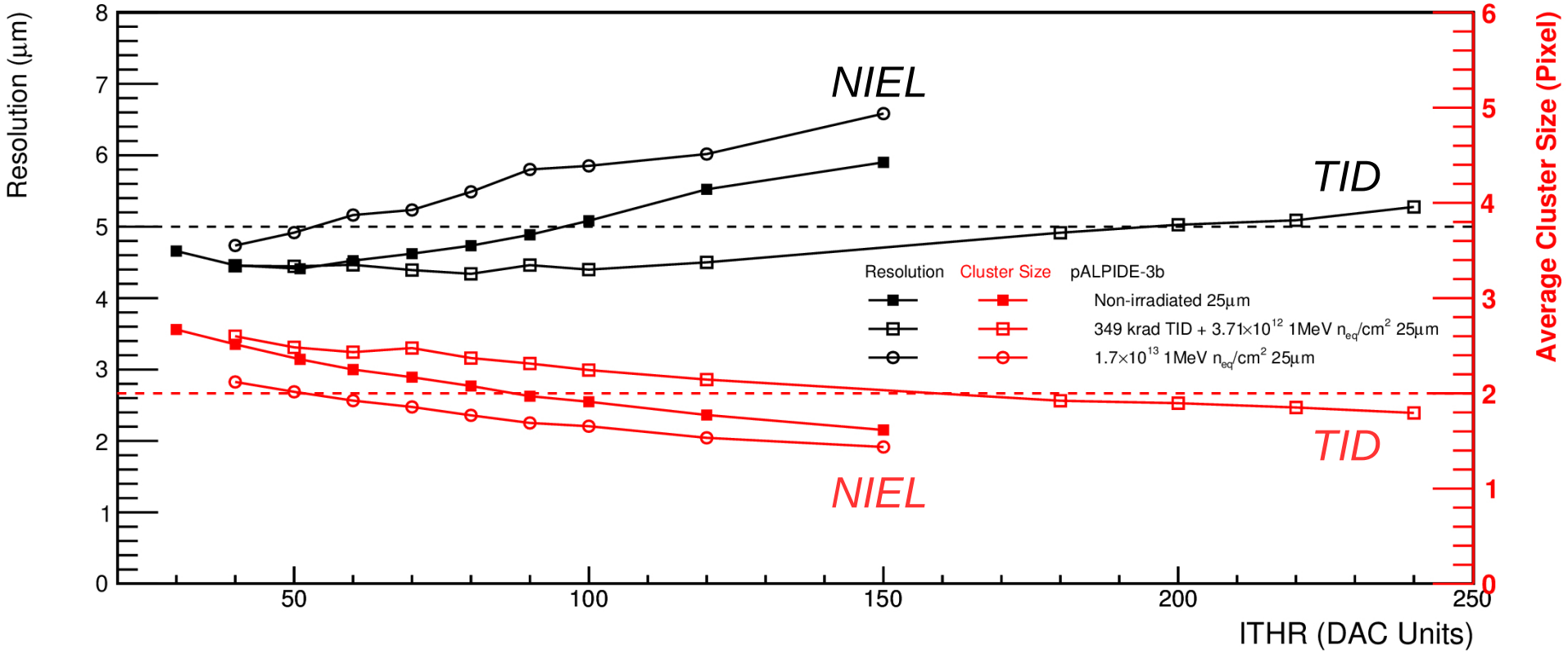
Larger input transistor → lower fake hit rate

Efficiency and fake hit rate II



Large margin for efficiency > 99% even after irradiation

Spatial resolution



Spatial resolution still at ~5 μm after irradiation

Summary and outlook

- ALPIDE is the state of the art MAPS to be installed in the new ALICE Inner Tracking System
  - Asynchronous and sparse readout
  - Very low power consumption
- Final prototype version performed up to specifications in extensive test beam campaign

  (ε > 99%, fake hit rate << 10^{-6} $pix^{-1}evt^{-1}$, spatial resolution ~ 5 μm)
- ALPIDE final design submitted in May 2016

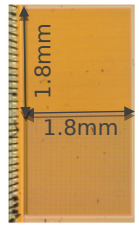
  → delivered end of August
- Validation of ALPIDE started

  → production starting soon

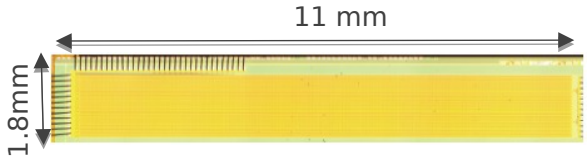
Backup slides

ALPIDE development

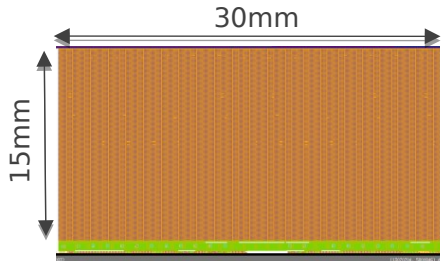
2012 — Explorer
- 20μm x 20μm and 30μm x 30μm pixels (analogue readout)
- pixel geometry, starting material, sensitivity to radiation



2013 — pALPIDEss-0
- Matrix with 64 columns x 512 rows
- 22μm x 22μm pixels
- (in-pixel discrimination and buffering)
- zero suppression within pixel matrix



May-2014 — pALPIDE-1
- **Full-scale prototype:** 1024 x 512
- 4 sectors with different pixels
- pixel pitch: 28μm x 28μm
- 1 register/pixel, no final interface

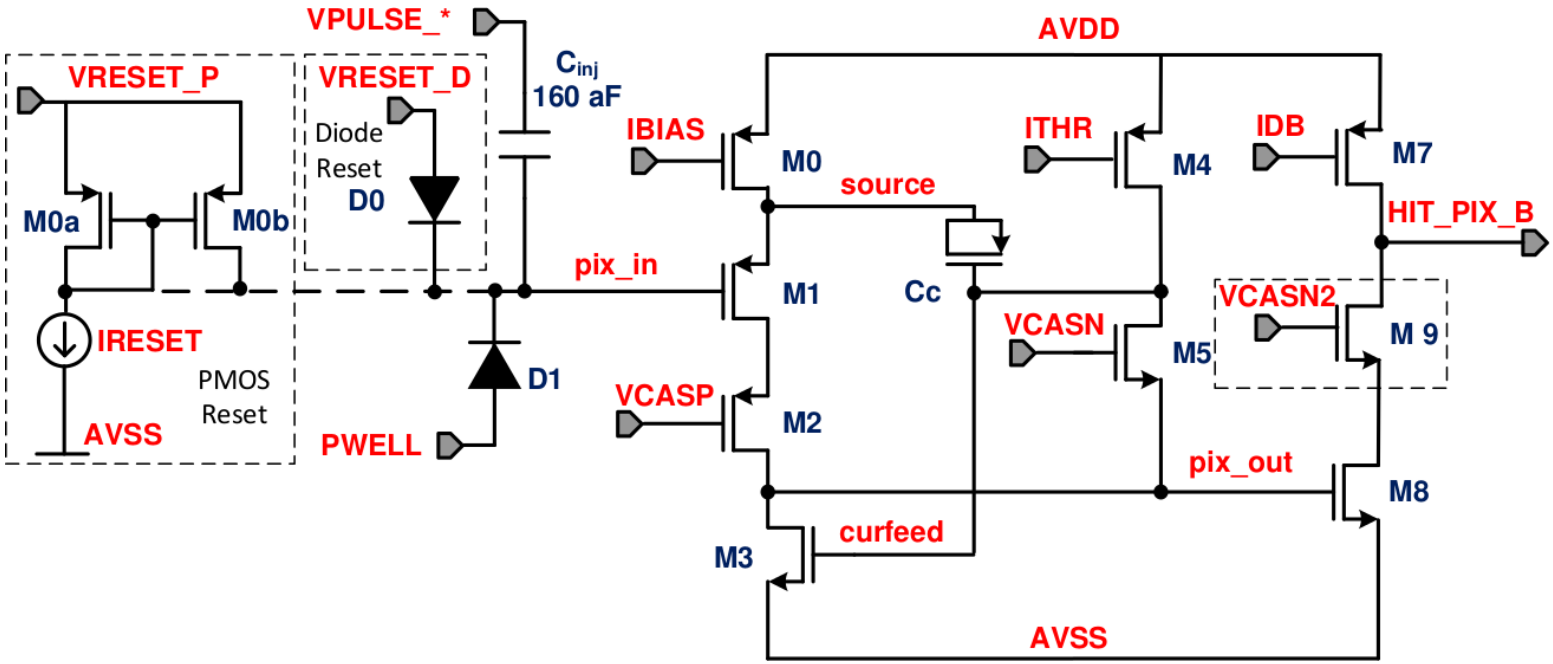


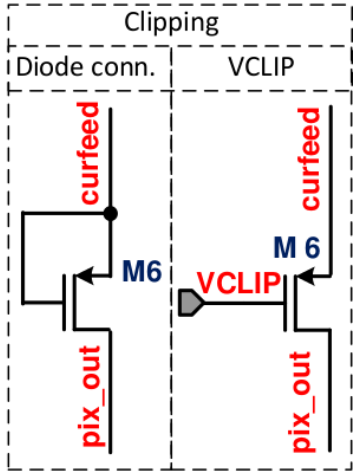
May-2015 — pALPIDE-2
- Optimization of several circuit blocks
- final interface: allows integration into ITS modules
- NO high-speed output link (1.2 Gbit/sec replaced by a 40Mb/s)

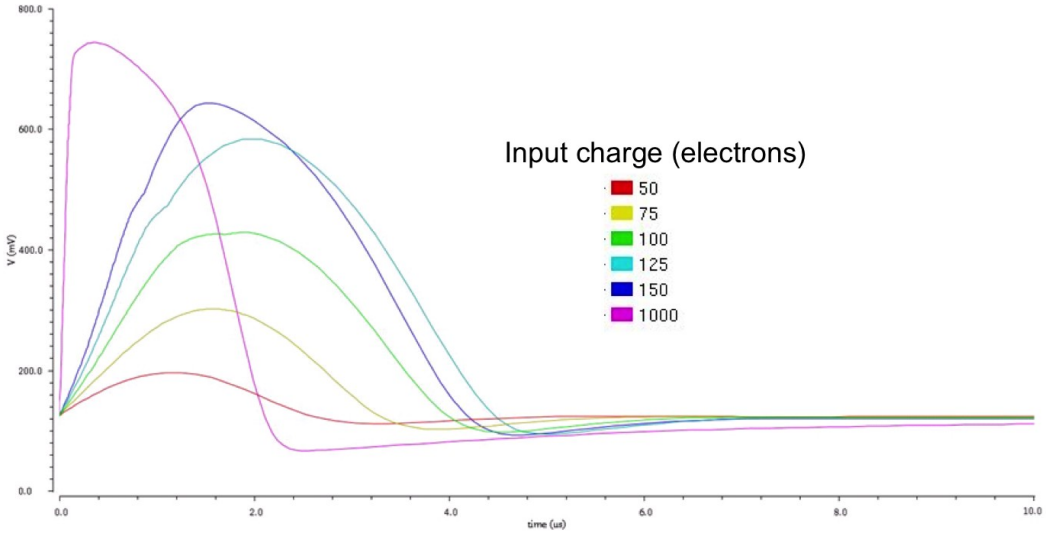
Oct-2015 — pALPIDE-3
- 8 sectors with different pixel variants, 3 registers / pixel
- Final interfaces, more features including 1.2 Gbit/s output serial link
- Some optimization for yield improvement

Aug-2016 — ALPIDE
- Final version

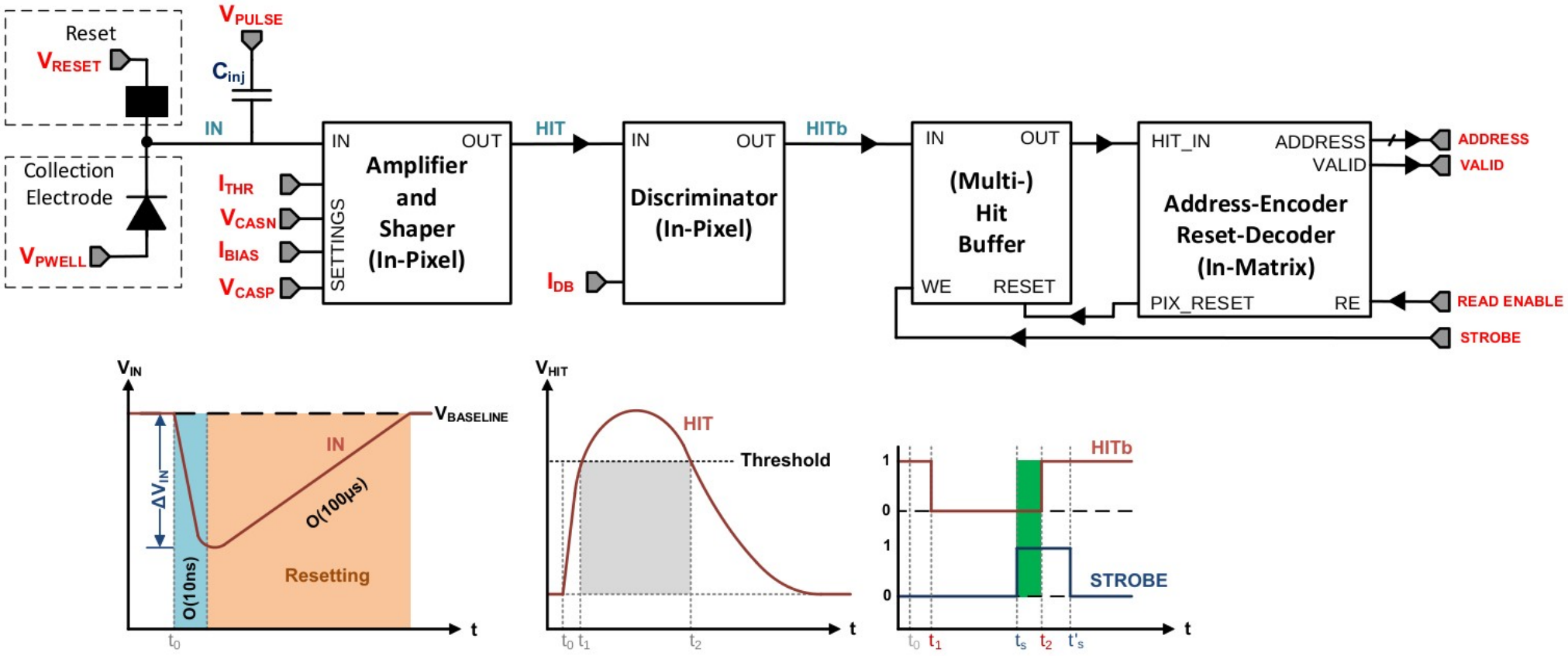
Front end circuit



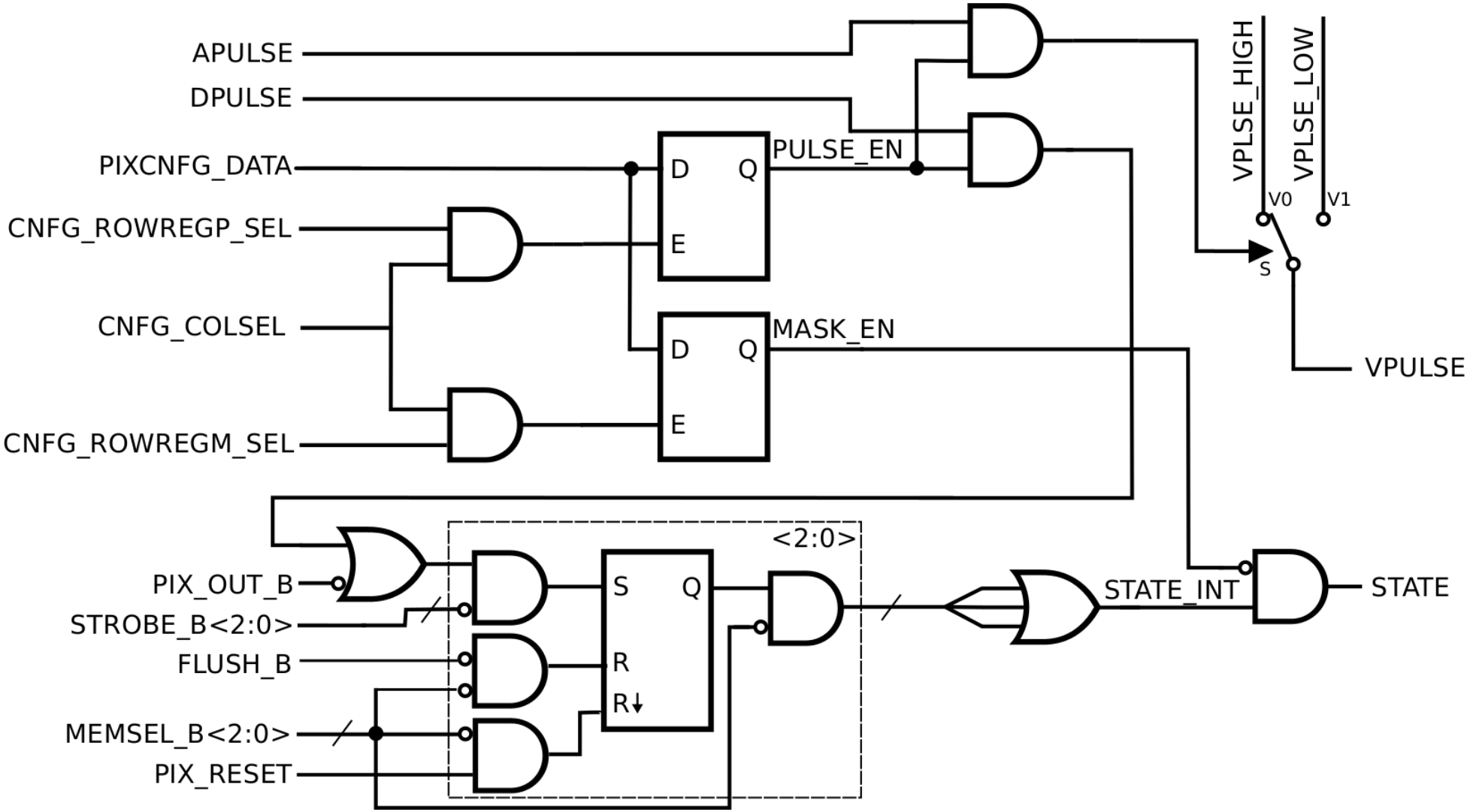




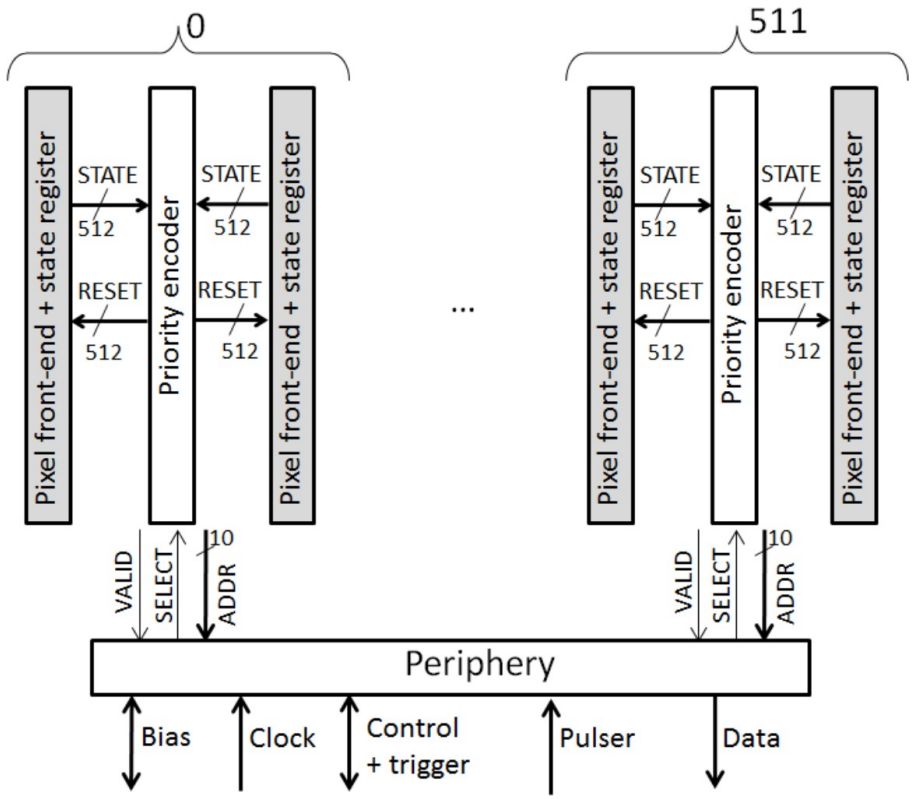
Principle of operation II



Digital circuit

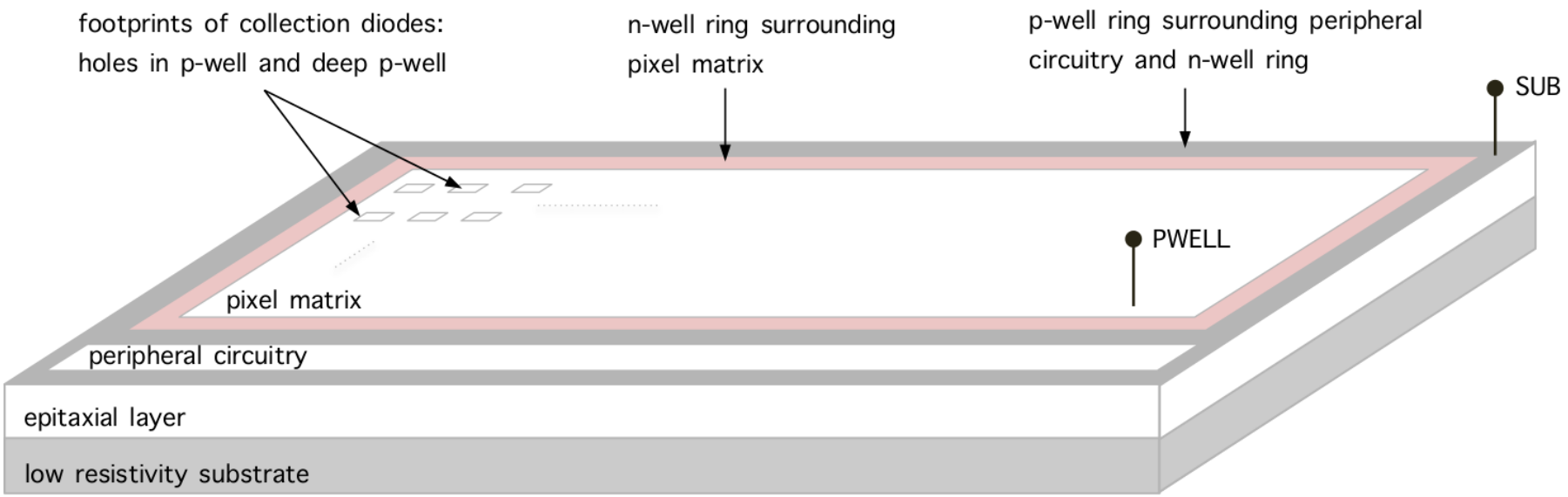


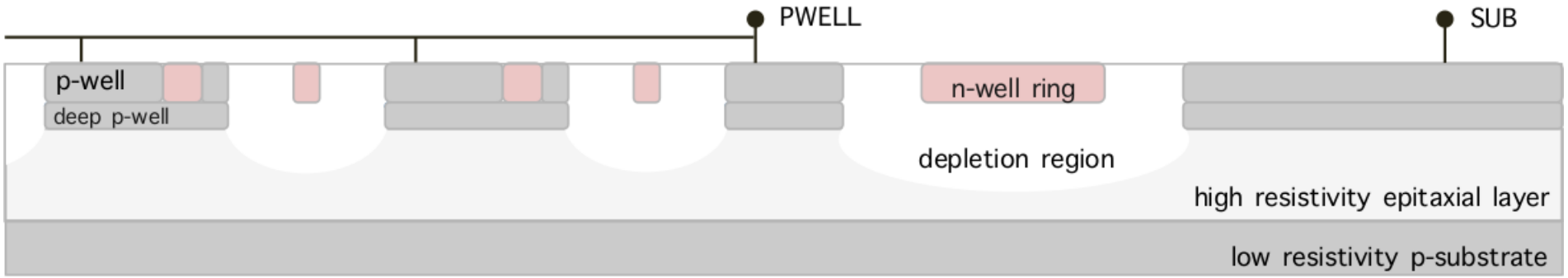
Readout



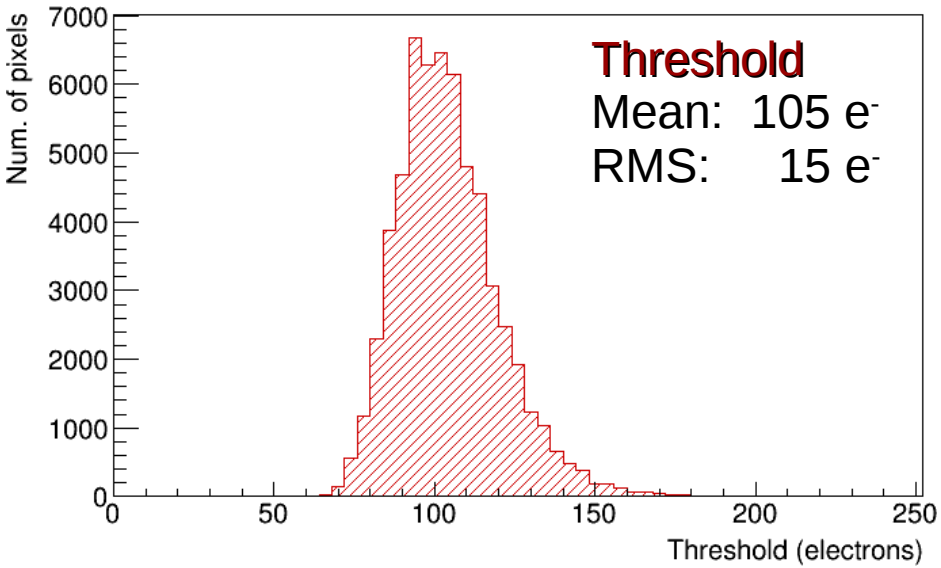
- The matrix is read out asynchronously by use of 512 priority encoders
- Serial bus for configuration and triggering (≈40 MHz)
- High speed serial link with up to 1.2 Gb/s for data readout

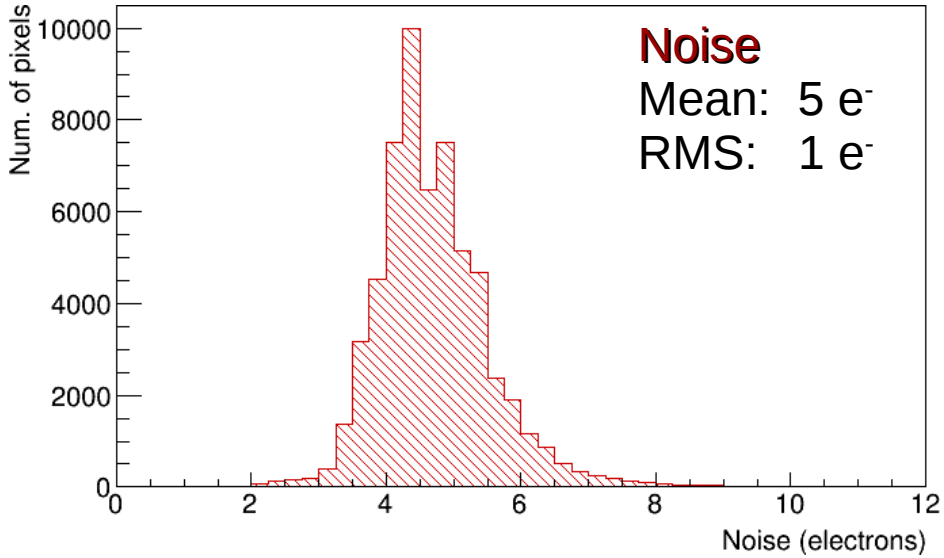
Substrate bias





Threshold and noise





- Threshold set globally → pixel to pixel variations
- Pulsing capacitance in each pixel

  → S-curve scan

  → Parameter extraction (threshold and noise)
- Threshold to noise ratio > 10 σ_{noise}
- MIP signal ~ 1000 e-