

8th International Workshop on Semiconductor Pixel Detectors for Particles and Imaging.

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Book of Abstracts

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Development of Pixel Detectors for X-ray Space Science and use in terrestrial applications

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The ALICE Pixel Detector Upgrade

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The ALICE experiment at the CERN LHC is designed to study the physics of strongly interacting matter, and in particular the properties of the Quark-Gluon Plasma, using proton-proton, proton-nucleus and nucleus-nucleus collisions. The ALICE Collaboration is preparing a major upgrade of the experimental apparatus to be installed during the second long LHC shutdown in 2019-2020. A key element of the ALICE upgrade is the new, ultra-light, high-resolution Inner Tracking System. With respect to the current detector, the new ITS will significantly enhance the pointing resolution, the tracking efficiency at low transverse momenta, and the read-out rate capabilities. This will be obtained by seven concentric detector layers based on a Monolithic Active Pixel Sensors with a pixel pitch of about $30\mu\text{m}\times 30\mu\text{m}$. A key feature of the new ITS, which is optimised for high tracking accuracy at low transverse momenta, is the very low material budget of 0.3% X_0 per layer for the innermost three layers. This contribution presents the design goals and layout of the upgraded ALICE ITS, summarises the R&D activities focussing on the technical implementation of the main detector components, and the projected detector and physics performance.

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JUNGFRAU: a pixel detector for Photon Science at free electron laser facilities.

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JUNGFRAU (adJUstiNg Gain detector FoR the Aramis User station) is a 75um pitch pixel detector developed at the Paul Scherrer Institut for photon science applications at free electron laser (FEL) facilities, with particular focus on the in house project SwissFEL.

JUNGFRAU is a hybrid pixel detector with a charge integrating readout ASIC (Application Specific Integrated Circuit), characterized by single photon sensitivity and a low noise over a dynamic range of 10^4 12keV photons. The dynamic range and the noise performance (~ 52 .e.n.c. rms in high gain) are enabled by a three gain, automatic switching preamplifier in each pixel, which dynamically

adjusts, pulse by pulse and pixel by pixel, its internal gain to the amount of input charge. Each JUNGFRÄU module, which can be tiled to assemble multi-megapixel cameras, is composed of 8 readout ASICs and has a total active area of $4 \times 8 \text{ cm}^2$ for a pixel count of 1024×512 . The module can be readout at a maximum frame rate of 2kHz. The design of the readout ASIC and of the module front-end electronics will be presented, together with the final detector setup at the SwissFEL endstations. The results of the module characterization, performed with X-Ray tube, synchrotron radiation and laser illumination will be reported.

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iPadPix - A Novel Educational Tool to Visualise Radioactivity Measured by a Hybrid Pixel Detector

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With the ability to attribute signatures of ionising radiation to certain particle types, pixel detectors offer a unique advantage over the traditional use of Geiger-Mueller tubes also in educational settings. We demonstrate in this work how a Timepix [1] readout chip combined with a standard $300 \mu\text{m}$ pixelated silicon sensor can be used to visualise radioactivity in real-time and by means of augmented reality. This chip family is the result of technology transfer from High Energy Physics at CERN and facilitated by the Medipix Collaboration. In the described prototype, a small Timepix detector assembly [2] is mounted next to the camera on the back of a tablet computer. The fields of view of both imaging sensors overlap such that traces of traversing particles recorded by the hybrid pixel detector can be shown as an overlay on the camera's live video feed. Particles with energies above $\sim 4 \text{ keV}$ are able to produce a signal in the detector and often create clusters consisting of several pixels. The cluster shapes and energies are evaluated in a classification process, which the iPadPix application uses to calculate count rates for identified alpha particles, electrons, photons and muons. Drawings of individual pixel clusters are animated and accompanied with particle type and energy information on the display.

This article summarizes the technical setup of the developed prototype based on an iPad mini and open source software [3]. Appropriate experimental activities that explore natural radioactivity and every-day objects are described to demonstrate the use of this new tool in educational settings.

[1] Xavier Cudie Llopart et al., Timepix, a 65k programmable pixel readout chip for arrival time, energy and/or photon counting measurements, Nucl. Instr. and Meth. A 581 (2007) 485–494

[2] Zdenek Vykydal et al., USB Lite - Miniaturized readout interface for Medipix2 detector, Nucl. Instr. and Meth. A 633 (2011) 48–49

[3] Oliver Keller, Visualisation of Radioactivity in Real-Time on a Tablet Measured by a Hybrid Pixel Detector, (2015) CERN-THESIS-2015-169

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A Prototype of a New Generation Readout ASIC in 65nm CMOS for Pixel Detectors at HL-LHC

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This paper describes a readout ASIC prototype designed by CHIPIX65 project, part of RD53, for a pixel detector at HL-LHC. A 64x64 matrix of 50x50 μm^2 pixels is realised. A digital architecture has been developed, with particle efficiency above 99.5 % at 3GHz/cm² pixel rate, 1MHz trigger with 12.5 μsec latency. Two analog front end designs, one synchronous and one asynchronous, are implemented. Charge is measured with 5-bit, analog dead-time below 1%. IP-blocks (DAC, ADC, BandGap, SER, sLVDS-TX/RX) and very front ends are silicon proven, irradiated to 600Mrad.

Summary:

The HL-LHC accelerator will constitute a new frontier for particle physics after year 2024. Major experimental challenge resides in inner tracking detectors: here the dimension of sensitive area (pixel) has to be scaled down with respect to LHC detectors.

This paper describes a readout ASIC in 65nm CMOS with a matrix of 64x64 pixels each of dimension 50x50 μm^2 , designed by CHIPIX65 project, part of RD53 Collaboration. It is a demonstrator of a Pixel Phase 2 chip, with compact design, low power and in-time threshold below 1000e⁻. All IP-blocks and analog front ends are designed by CHIPIX65 project in the framework of RD53 Collaboration: they have been produced, tested and several have already proven to be radiation hard up to 5-800 Mrad. The chip implements two different analog front end designs, one with asynchronous the other with synchronous comparator designs, but with main common characteristics: compact design; ENC below 100 e⁻ for 50 fF input capacitance; below 5 μW /pixel power consumption; fast rise time, allowing correct time-stamp; signal digitisation using Time Over Threshold; leakage current compensation up to 50nA per pixel.

All global biases and voltages are programmed in the chip periphery, for each value a 10-bits current steering global DAC is used; a band gap circuit provides a stable reference voltage. The adopted strategy is very robust, easily scalable and mismatch effects are kept to a negligible level. Bias voltages and current are monitored by a 12-bit ADC.

A novel digital architecture has been designed in order to maintain a high efficiency (above 99%) at pixel hit rate of 3 GHz/cm² , trigger of 1 MHz rate and latency of 12.5 μsec . The digital architecture is organized into pixel regions: in order to have a very compact and low power architecture, a large pixel region consisting of 4x4 pixels has been used. A 5-bit ToT charge is stored in a centralised latency buffer: at the arrival of a trigger, a matching logic selects eventually the right memory location and sends the data to the End of Column logic. The particle inefficiency due to this architecture is about 0,1% for an area occupation of of 65% and a low power consumption. The readout is obtained using a column drain protocol with a FIFO for each pixel region column, connected to a global dispatcher FIFO that after a 8b10b encoding splits the data into 20-bit trunks and sends them to a serialiser. Data are sent out from the chip using a differential transceiver converting the CMOS into SLVDS JEDEC 400mV standard. Given the small size of the chip, an output rate of 320 MHz for the serialised data can be used, but higher output rates are possible., since SER and sLVDS-TX are designed to sustain up to 1.2 Gb/s. Chip configuration is performed through fully-duplex synchronous SPI-master/slave transaction. CHIPIX65 demonstrator will be submitted in June 2016.

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Signal simulation under the bias rail in n⁺-in-p pixel sensors before and after irradiation

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We have developed n⁺-in-p pixel sensors with biasing network to provide the reverse bias voltage to individual pixels without bumpbonding a readout ASIC. This is a part of quality control of the pixel sensors in the sensor fabrication process to eliminate those having defective pixels, e.g. inducing the microdischarge. The pixel sensor that has a design with a conductive trace, called the bias rail, running at the boundary between the pixels has shown a loss of track-finding efficiency at the boundary under the bias rail when the device is irradiated with protons. The device has shown little efficiency loss initially. It was shown qualitatively and visually that the loss of efficiency is due to the interplay of electric field in the silicon bulk and the induction of charge to the electrode of constant voltage. In this signal simulation, we have imported the electric fields and the weighting potentials from TCAD calculations. We have evaluated the charges lost to the bias rail from the distribution and drifting of the charge carriers in the silicon. A comparison of the results with or without radiation damage has confirmed quantitatively the loss or little loss of efficiency, respectively.

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The entire tracking system of the ATLAS experiment will be replaced during the LHC Phase II shutdown around 2025 by an all-silicon detector (Inner Tracker, ITk).

The pixel detector will be composed by the five innermost layers, instrumented with new sensor and readout electronics technologies to improve the tracking performance and cope with the severe HL-LHC environment in terms of occupancy and radiation. The total area of the new pixel system could measure up to 14 m², depending on the final layout choice that is expected to take place in early 2017

Different designs of planar, 3D, CMOS sensors are being investigated to identify the optimal technology for the different pixel layers. In parallel sensor-chip interconnection options are evaluated in collaboration with industrial partners to identify reliable technologies when employing 100-150 μm thin chips.

While the new read-out chip is being developed by the RD53 Collaboration, the pixel off detector read-out electronics will be implemented in the framework of the general ATLAS trigger and DAQ system. A readout speed of up to 5 Gb/s per data link (FE-chip) will be needed in the innermost layers going down to 640 Mb/s for the outermost. Because of the very high radiation level inside the detector, the first part of transmission has to be implemented electrically with signals to be converted for optical transmission at larger radii.

Extensive tests are being carried out to prove the feasibility of implementing serial powering chosen as the baseline for the ITK pixel system, given the reduced material in the servicing cables foreseen for this option.

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The CT-PPS tracking system with 3D pixel detectors

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The CMS-TOTEM Precision Proton Spectrometer (CT-PPS) detector will be installed in Roman pots (RP) positioned on either side of CMS, at about 200 m from the interaction point. This detector will measure forward leading protons, allowing detailed studies of diffractive physics and central exclusive production in standard LHC running conditions. An essential component of the CT-PPS apparatus is the tracking system, which consists of two detector stations per arm equipped with six 3D silicon pixel-sensor modules, each read out by six PSI46dig chips. The front-end electronics has been designed to fulfill the mechanical constraints of the RP and to be compatible as much as possible with the readout chain of the CMS pixel detector. The tracking system is currently under construction and will be installed by the end of 2016. In this contribution the final design and the expected performance of the CT-PPS tracking system will be presented. A summary of the studies performed, before and after irradiation, on the 3D detectors produced for CT-PPS will be given.

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Role of Pixel Detectors in High Energy Physics

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A number of new types of pixel detectors have been pioneered in the last few years. This includes new types of sensors as well as new electronics to allow much higher performance. At the same time new experiments are being planned or nearing completion covering a broad range of physics topics in flavor physics as well as large major upgrades at the LHC. These are planning to make use of the advances in pixel detectors in important ways. In this review both the pixel advances and how they enable the physics will be presented.

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Characterization of Time over Threshold based X-ray and Gamma-ray detector with pixelated GAGG coupled to SiPM array

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Silicon photomultipliers (SiPMs) are promising photo detectors for Positron Emission Tomography (PET) and X-ray/Gamma-ray imaging system because of its high gain and photon counting capability. The individual readout is necessary to achieve a better spatial resolution especially in high flux applications.

In this study a prototype of photon counting pixel detector using SiPMs and Time over Threshold (ToT) ASIC was designed and fabricated for sub-mm PET and X-ray/Gamma-ray applications. The fabricated photo detector consists of 12 x 12 pixels with the pitch of 1.9 mm using KETEK PM1150 SiPMs individually coupled with Cerium doped GAGG scintillators. All channels are individually coupled to ToT ASIC through micro-coaxial cables. The TOT outputs of all channels are connected to data acquisition (DAQ) FPGA in parallel.

48 channels TOT-ASIC consists of current buffers and current comparators with internal DACs (digital-to-analog converter) of the 6 bit resolution. The ASIC was fabricated with 0.25 μm CMOS TSMC process using 2.5 V where power consumption is approximately 200 mW per chip. The first transmission image was successfully acquired with individual energy spectrum.

In this study various characteristics, such as timing resolution, energy resolution and count rate of fabricated pixel detector will be presented.

Summary:

In this study a prototype of photon counting pixel detector using SiPMs and Time over Threshold (ToT) ASIC was designed and fabricated for sub-mm PET and X-ray/Gamma-ray applications.

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3D sensors for the HL-LHC

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3D silicon detectors, with cylindrical electrodes that penetrate the sensor bulk perpendicular to the surface, have recently undergone a rapid development from R&D, to industrialization, to their first operation in a high-energy-physics experiment. Since June 2015, the ATLAS Insertable B-Layer is taking collision data with 3D pixel sensors. At the same time, 3D devices have been installed in February 2016 as part of the ATLAS Forward Proton detector. The next challenge for tracking detectors is the high-luminosity LHC (HL-LHC) tracker upgrades, where fluences of up to $1.4\text{E}16$ neq/cm² are expected for the innermost layer. The 3D technology is a firm candidate for the innermost pixel layers given its excellent radiation hardness at low operational voltages and power dissipation. This paper will give an overview on the recent developments of the HL-LHC generation of 3D sensors.

Summary:

The talk will briefly review the development and performance of 3D sensors for the ATLAS IBL and the AFP detectors. The challenges presented by the HL-LHC require new technological improvements to accommodate the larger radiation doses and smaller pixel sizes. The strategy to develop 3D sensors for the HL-LHC era will be discussed. Results from laboratory and testbeams of irradiated and non-irradiated devices with new pixel geometries will be presented.

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Impact of the Belle II Pixel Detector on CP -Violation Measurements

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The new asymmetric electron positron collider SuperKEKB in Tsukuba, Japan, is currently being commissioned. With a design luminosity of $8 \cdot 10^{35} \text{ cm}^{-2} \text{ s}^{-1}$ and an expected integrated luminosity of about 50 ab^{-1} , it will surpass the world record reached by its predecessor KEKB by a factor 50. In order to reach the high instantaneous luminosity, the beam energy asymmetry has to be reduced, resulting in a lower boost. This, together with the expected increase of machine background, sets high requirements to the new Belle-II detector, which is under construction.

In order to fully exploit the high luminosity, a new Belle-II pixel vertex detector has been developed. Consisting of two layers of thin, monolithic pixel sensors in DEPFET technology, mounted at 14 mm and 22 mm from the interaction point, it will cope with the strongly increased machine background, providing excellent precision for three-dimensional vertex measurements of particles decaying inside the beam pipe.

The physics performance of the Belle-II pixel vertex detector and its impact on the reduction of experimental uncertainties will be treated with focus on the measurement of the *CP*-Violating parameters in various *B* and *D* decay modes.

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Optimization of thin n-in-p planar pixel modules for the ATLAS upgrade at HL-LHC

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The ATLAS experiment will undergo around the year 2025 a replacement of the tracker system in view of the high luminosity phase of the LHC (HL-LHC) with a new 5-layer pixel system.

Thin planar pixel modules are promising candidates to instrument the innermost region of the new pixel system, thanks to the reduced contribution to the material budget and their high charge collection efficiency after irradiation. 100-150 μm thick sensors, interconnected to FE-I4 read-out chips, have been characterized with radioactive source scans and beam tests. Their performance up to a fluence of $10^{16} \text{ 1 MeV neq}$ will be compared in terms of charge collection and hit efficiency.

New designs of the pixel cells, with an optimized bias structure, have been implemented in n-in-p planar pixel productions, and the possible gain in the hit efficiency investigated as a function of the received irradiation fluence. The outlook for future planar pixel sensor productions will be discussed, with a focus on sensor design at the pixel pitches (50x50 and 25x100 μm^2) foreseen for the ATLAS read-out chip in 65 nm CMOS technology. First results of the characterization on planar sensors produced with these pixel cell sizes will be shown. Highly segmented sensors will represent a challenge for the tracking in the forward region of the pixel system at HL-LHC. In order to reproduce the performance of 50x50 μm^2 pixels at high eta, FE-I4 compatible planar pixel sensors have been studied before and after irradiation in beam tests at high incidence angle with respect to the short pixel direction. Results on cluster shapes, charge collection and hit efficiency will be shown.

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Total Ionization Dose effects in the FE-I4 front-end chip of the ATLAS Pixel IBL detector

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The ATLAS Pixel Insertable B-Layer (IBL) detector was installed into the ATLAS experiment in 2014 and

has been in operation since 2015.

During the first year of IBL data taking an increase of the LV current produced by the FEI4 chip was observed,

and this increase was traced back to the radiation damage in the chip. The dependence of the current from the

Total Ionizing Dose (TID) and temperature has been tested with X-ray and proton irradiations and will be

presented in this talk

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MuPix7 –a fast monolithic HV-CMOS pixel chip for Mu3e

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The MuPix7 chip is a monolithic HV-CMOS pixel chip, thinned down to 50 μm . It provides continuous self-triggered, non-shuttered readout at rates up to 30 Mhits/chip of 3 x 3 mm² active area and a pixel size of 103 x 80 μm^2 . The hit efficiency depends on the chosen working point. Settings with a power consumption of 300 mW/cm² allow for a hit efficiency >99.5%. A time resolution of 11 ns (Gaussian sigma) is achieved. We are going to present the latest results from 2016 test beam campaigns and will cover the roadmap towards the final chip for Mu3e.

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Tracking and flavour-tagging performance for HV-CMOS sensors in the context of the ATLAS ITK pixel simulation program

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The HV-CMOS pixel technology has recently risen interest in the ATLAS community in view of its possible usage for the ATLAS pixel detector upgrade towards the High Luminosity LHC phase. HV-CMOS sensors can be employed in the pixel outer layers given the reduced radiation hardness at high radius and their cheap technology. However, the largest impact on physics performance, vertexing, tracking and flavour tagging, could be achieved if exploited in the innermost layers due to their very fine granularity and small depletion depth that can result in improved tracking resolution and better characterisation of the cluster size for tracks in the large pseudorapidity region.

Summary:

An overview of the studies on the tracking performance resulting from the usage of HV-CMOS sensors in the Innermost Pixel Layer will be presented. Full simulations based on Geant4 and ATLAS reconstruction are used to assess the typical gain of the various detector designs. Different pixel granularities and depletion depths are explored and the typical resolution of the tracking residuals and impact parameters is compared to the present pixel technology in the Innermost Pixel Layer (IBL). In addition, the expected impact of this technology is also verified on tt events in order to disentangle pure resolution effects from pattern recognition issues, with a particular emphasis on b-tagging performance gauged by the improvement of the light-flavour and c-jet rejection for a given b-jet efficiency. A detailed study on the specific pixel clustering algorithm to be used in the simulation will be discussed as well.

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Design and Development of an Event-driven SOI Pixel Detector for X-ray Astronomy and Light Dark Matter Search

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We have been developing monolithic active pixel detectors, named “XRPIX” based on the silicon-on-insulator (SOI) pixel technology, for future X-ray astronomical satellite missions. Our objective is to replace X-ray Charge Coupled Devices (CCD), which are now standard detectors in the field. The XRPIX series offers good time resolution ($\sim 1 \mu\text{s}$), fast readout time ($\sim 10 \mu\text{s}$), and a wide energy range (0.5–40 keV) in addition to having imaging and spectroscopic capability comparable to CCDs. XRPIX contains a comparator circuit in each pixel for hit trigger (timing) and two-dimensional hit-pattern (position) outputs. Therefore, signals are read out only from selected pixels. X-ray readout by this function is called “event-driven readout”.

In our previous studies, we successfully demonstrated X-ray detection by the event-driven readout. We improved the X-ray spectral performance by introducing in-pixel charge-sensitive amplifier circuit in the frame readout mode, which an analog signal from all pixels periodically. We achieved an energy resolution of 320 eV (FWHM) for 5.9 keV X-rays with which Mn-K α and -K β lines are

resolved for the first time in the XRPIX series. Recently, we designed the first prototype to achieve a large-area device for satellite loading. The detector is 24.6 mm × 15.3 mm in size and consists of 608 × 384 pixels. The pixel size and the imaging area are 36 μm × 36 μm and 21.9 mm × 13.8 mm, respectively. Moreover, We propose a light dark matter search experiment using the XRPIX. In this presentation, we report on the design and evaluation results of the new device, and the plan about a light dark matter search experiment.

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4D pixel detectors

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In this contribution we will review the progresses toward the construction of a tracking system able to measure the passage of charged particles with a combined precision r.m.s. of ~ 10 ps and ~ 10 μm, either using a single type of sensor, able to concurrently measure position and time, or a combination of position and time sensors.

Summary:

The inclusion of timing information in the structure of a recorded event has the capability of changing the way we design experiments, as this added dimension dramatically improves the reconstruction process. Depending on the type of sensors that will be used, timing information can be available at different stages in the reconstruction of an event, for example (i) at tracking reconstruction, if timing is associated to each point or (ii) during the event reconstruction, if timing information is associated to each track. In the first case, the 4th dimension brings a simplification already in the reconstruction algorithm as only time-compatible hits are used in the pattern recognition phase, however the electronics is very demanding as it needs to be able to accurately measure timing in each pixel. The second case is simpler as it requires the implementation of a dedicated timing layer, either inside or outside the main silicon tracker volume, to assign the timing information to each crossing track without changing the vast majority of the tracker hardware. The timing information can then be used to improve Level 1 trigger decisions, as it can be obtained faster than tracking reconstruction, and to separate events with overlapping vertices.

We will present the research and development progresses in terms of sensors and read-out electronics, showing the current best limits and reviewing the possible technological choices currently developed

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Development of Electron-Tracking Compton Imaging system using SOI Pixel Sensor with a 30-μm pitch

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Compton cameras have been used for various applications including astronomical observations, radioactive waste management, and biomedical imaging. They have advantages over mechanical collimation imaging systems in wide field of view (FOV), suppression of background, and high detection efficiency. Compton cameras use the kinematics of Compton scattering to determine the incident angular of gamma rays. The source position is identified in the intersection of multiple cone traces through a large number of events.

We explore a new approach for advanced Compton imaging with the function of tracking recoiled electron by a combination of a silicon on insulator (SOI) pixel detector and a GAGG scintillator array coupled to MPPC on the other end. The ejected direction of a recoiled electron caused by Compton scattering is detected on the SOI pixel detector with a pitch of 30 μm . The incident direction of the gamma ray can be confined to arc, which can enhance the signal-to-noise ratio (SNR) and angular resolution.

The SOI detector consists of 144 \times 144 pixels, and each pixel has a charge integration circuit and trigger circuit [1][2][3]. The GAGG array consists of 8 \times 8 crystal with a size of 3 mm \times 10 mm \times 10 mm, and each crystal is individually coupled to a pixel of TSV-type MPPC. The signal of GAGG is amplified and converted to digital signal by dynamic time over threshold method (dToT method) [4]. The coincidence event is detected and determined by the trigger signal from SOI pixel detector and dToT wired-OR output from GAGG/MPPC detector using data acquisition FPGA.

The recoiled electron trajectories of Am-241 and Cs-137 were detected on 25 \times 25 pixels in trigger-mode, and the charges caused by Am-241 were shared in around 4 pixels of SOI detector [5]. We will show the results of Electron-tracking Compton imaging using SOI pixel sensors.

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First results on the ATLAS HL-LHC H35DEMO pixel prototype

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The H35DEMO is a prototype ASIC aimed at proving that High Voltage-CMOS (HV-CMOS) sensor technologies can be qualified as tracking detectors for harsh working environments such as that of the High Luminosity-LHC (HL-LHC). The prototype is in the 0.35 μm HV-CMOS process from ams and was fabricated through an engineering run in which wafers with four different substrate resistivities that range from the standard value of 20 $\Omega\cdot\text{cm}$ to a high value of 1k $\Omega\cdot\text{cm}$ were used as a solution to increase the depletion region of the sensor. To allow studying yield issues, the prototype has a large area of 24.40 mm \times 18.49 mm that is divided into four independent matrices with a few thousand pixels each. Two of the matrices can be read out using a readout ASIC only, whilst the

other two are completely monolithic. All the matrices can be bump bonded or glued to the FE-I4 ASIC for readout in a one-to-one connection. A few test structures for sensor characterization were also integrated in the chip.

A new experimental set-up based on a custom made pcb and the ZC706 evaluation board from Xilinx has been developed by the Liverpool group. The set-up allows measuring one of the monolithic matrices by using the on-chip digital readout block. This matrix has nMOS only discriminators with and without time-walking compensation inside the pixel area. Features such as gain, speed and sensitivity to a radioactive source have been tested, showing that measured results are in good agreement with Cadence simulations. TCT and edge-TCT measurements on back biased thinned chips have allowed us to analyze the benefits of this type of biasing on charge collection effects. The first measured results on the H35DEMO prototype will be presented at the workshop.

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Test beam results of 3D detectors constructed with single-crystal and poly-crystalline diamond

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Results from prototypes of a novel detector using chemical vapour deposited (CVD) diamond and resistive electrodes in the bulk forming a 3D diamond device will be presented. The electrodes of the device were fabricated with laser assisted phase change of diamond into a combination of diamond-like-carbon, amorphous carbon and graphite. The connections to the electrodes of the 3D device were made using a photo-lithographic process. A detector system consisting of 3D devices, one based on single-crystal CVD diamond and one based on poly-crystalline CVD diamond were connected to a multi-channel readout and successfully tested in a 120 GeV proton beam at CERN proving for the first time the feasibility of the 3D diamond detector concept for particle tracking applications. Subsequent tests have refined our understanding of the charge sharing between 3D cells and the position resolution of these devices. The electrical properties and beam test results of the prototype devices will be presented.

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Development of n⁺-in-p planar pixel sensor flip-chip modules with quad FE-I4 readout ASIC's

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We have developed prototype pixel detector modules for the inner tracker of the ATLAS detector to be upgraded for the high-luminosity LHC. The module is made of pixel sensor and pixel readout ASIC's, being flip-chip bumpbonded. The pixel sensor is an n⁺-in-p planar sensor of a size of 2×2 of ATLAS FE-I4 pixel readout ASIC's, called the quad-sensor. Seven such sensors were laid out in 6-inch p-type FZ wafer, with three different gaps between the ASIC's, and thinned to 150 μm. The wafers of the FE-I4 ASIC's were also thinned to 150 μm and deposit with lead-free SnAg solder bumps. The bumpbonding was made specifically by taking care of removing oxidation in the surface of the

bump pads/solders of the sensors/ASIC's. Four of the quad-sensor modules, with 16 ASIC's, were bumpbonded by introducing Hydrogen-plasma reflow process (H-SnAg), and in addition, two were by applying solder-flux. The quad-sensor modules were gone through thermal cycles between +/- 40°C, irradiation to protons of a fluence of approximately 3×10^{15} neq/cm². Bump disconnection was checked against the beta-ray response before and after the thermal cycles and the irradiation. No large-area bump disconnection was observed. The modules were evaluated with testbeams and showed good performance.

Authors: Y. Unno, Hamamatsu Photonics K.K. and ATLAS-J Silicon Collaboration

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Edge Integrity Determination for Assessing Sensor Chip Quality

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CERN operates a large hadron collider (LHC) to conduct one of large scale particle physic experiment, namely ALICE. In this experiment, thousand of sensor chips are used to track particle trajectories after the collision events. The sensor chips are mainly installed at Inner Tracking System (ITS) which is located in the centre of LHC. Metrological measurement is performed to satisfy technical specifications of ITS sensor chips. Chip edge integrity is one of physical parameters that need to be measured. The integrity is determined based on edge cutting quality of sensor chip. A vision inspection algorithm is proposed to analyse the integrity parameter. It measures the distance between chip cutting edges and reference lines. Cracking appearances at the area between cutting edges and reference lines will also be considered in quality determination. Gray-scale image of chip edges are automatically analysed to classify chip quality. The images are acquired by a specialised vision system that provide spatial resolution at 0.5 micron per pixel. The measurement is performed for chip edge regions such as horizontal-vertical sides and corner parts. If the measurement results satisfy the required value then the chip will be accepted. Conversely, if the required value cannot be achieved then the chip will not be accepted. The proposed algorithm will be applied to complete a series of physical and electrical chip testing.

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The EIGER detector systems

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EIGER is a single photon counting hybrid pixel detector developed at the Paul Scherrer Institute (PSI) for synchrotron applications.

The pixel size is $75 \times 75 \text{ } \mu\text{m}^2$ and it features noise as low as 70 e^- equivalent noise charge RMS (depending on settings) and a very high frame rate (up to 24 kHz). Each pixel has a counter which can be configured in 4, 8 or 12 bit mode. A larger dynamic range of 32 bits can be obtained by splitting the acquisition into short sub-frames and summing them on the readout boards. The minimum dead time between frames is 3 μs thanks to the double buffering capabilities of the counter.

Large area EIGER detectors are being produced by tiling single modules. A single module consists of a $8 \times 4 \text{ cm}^2$ silicon sensor bump bonded to 4×2 readout chips, for a total of 0.5 Mpixels. The largest of the systems in production at PSI is a 9-Mpixel detector for the coherent small angle X-ray scattering (cSAXS) beamline at the Swiss Light Source Synchrotron. The very high frame rate capability is conserved for multi-module systems due to fully parallel data processing. The count rate capabilities are 200-500 kHz/pixel at 90% linearity of the counter versus the incident photon flux. Rate corrections can be applied on-board before the sub-frame summation to compensate for fast varying pile-up rates. The on-board corrections restore the linearity up to at least 1.2 MHz/pixel incident rate. Performance of the detector, calibration and operational challenges of the large systems will be presented.

EIGER can also be used to detect electrons: characterization of the detector performances with low energy electrons (8-20 keV) and medium energy ($>100 \text{ keV}$) has been performed. Results will be presented as well as plans to optimize the detector for electron detection towards the use of EIGER in photo-emission electron microscopes and transmission electron microscopes.

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Beam Test Results of the Dependence of Signal Size on Incident Particle Rate in Diamond Pixel and Pad Detectors

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We will present beam test results on the dependence of signal size on incident particle rate in charged particle detectors based on single-crystal and poly-crystalline CVD diamond. The detectors were tested over a range of particle fluxes from 2 kHz/cm² to 20 MHz/cm². The pulse height of the sensors was measured with pad and pixel readout electronics at shaping times from 10ns to 1 μs , as a test of possible charge carrier lifetime dependences. We will present data from the 2014 and 2015 beam tests at PSI indicating the pulse height of non-irradiated single-crystal CVD diamond sensors is independent of flux, while the pulse height of irradiated single-crystal CVD diamond sensors decreases with increasing particle flux. The sensitivity to flux is similar in both diamond pad sensors constructed using diamonds from the Pixel Luminosity Telescope (PLT) irradiated during its pilot run in CMS experiment and in neutron irradiated diamond pad sensors, from the same manufacturer, irradiated to the same fluence. The pulse height for non-irradiated and irradiated poly-crystalline CVD diamond pad sensors was observed to be independent of particle flux. Correlations between the spatial uniformity of the charged particle pulse-height in polycrystalline diamond and any dependence on the flux are also being studied. The latest test beam results for both single-crystal and poly-crystalline CVD diamond will be shown.

questions

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4D fast tracking for experiments at HL-LHC

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Several efforts have been recently devoted to develop high-resolution timing detectors for tracking at the High Luminosity LHC experiments while track triggers, implemented with dedicated hardware, have been used at hadron colliders to select heavy-flavour decays. In this R&D project we propose to combine the two methods to develop an innovative detector, based on accurate time and position particle hit measurements, for 4D tracking and fast track trigger. The precise measurement of the hits' time is the key feature to operate an effective pattern recognition that guarantees a high tracking efficiency while enhancing the ghost track rejection, and to perform selective track triggering. We ultimately aim to exploit this detector in flavour physics experiments, in conditions of a high event pile-up, where sensors and front-end electronics are required to provide a hit time resolution of the order of 20 ps and a hit position resolution better than 40 μm , and are able to continuously operate in a harsh radiation environment (up to a total flux of 10^{17} 1-MeV neutrons equivalent per cm^2).

Summary:

State of the art tracking pixel detectors with precise time-tagging show a time resolution of about 200 ps [1], and we aim to reduce this by one order of magnitude. Crucial aspects to achieve this ultimate time resolution are the optimization of pixel sensor geometries (in both 3D and planar technologies) to achieve the most uniform electric field, and the design of fast and low noise dedicated front-end ASIC. This front-end will incorporate a fast current amplifier followed by a discriminator and a time-to-digital converter, and will be developed in 65 nm CMOS technology with fault tolerant architecture which matches the radiation hardness requirements.

Feasibility studies of a 4D fast track finding system, using hits' space and time information, has been recently presented [2] as a possible solution for the low level track trigger of the HL-LHC experiments. The system is based on a massively parallel algorithm implemented in commercial FPGAs using a pipelined architecture and allows a precise real-time determination of the track parameters (including time) while maintaining a low fraction of reconstructed fake tracks.

The proposed detector will allow to perform flavour physics at LHC while operating at instantaneous luminosities more than one order of magnitude larger than the current ones, while guaranteeing large tracking efficiencies and a negligible ghost tracks rate.

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The Atlas IBL CO2 Cooling System

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The ATLAS Pixel detector has been equipped with an extra B-layer in the space obtained by a reduced beam pipe. This new pixel detector called the ATLAS Insertable B-Layer (IBL) is installed in 2014 and is operational in the current ATLAS data taking. The IBL detector is cooled with evaporative CO₂ and is the first of its kind in ATLAS. The ATLAS IBL CO₂ cooling system is designed for lower temperature operation (<-35°C) than the previous developed CO₂ cooling systems in High Energy Physics experiments. The cold temperatures are required to protect the pixel sensors for the high expected radiation dose up to 550 fb⁻¹ integrated luminosity.

This paper describes the design, development, construction and commissioning of the IBL CO₂ cooling system. It describes the challenges overcome and the important lessons learned for the development of future systems which are now under design for the Phase-II upgrade detectors.

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Physics benchmarks with the VELO pixel

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The upgrade of the LHCb experiment, planned to start data taking in LHC Run 3 in 2021, will transform the experiment to a trigger-less system reading out the full detector at 40 MHz event rate. The electronics of all systems will be changed and the tracking detectors completely replaced. For the Vertex detector this will see a move from the currently installed strip detectors to a fully pixel based system.

At the upgrade all data reduction algorithms will be executed in a high-level software farm with access to the complete event information. The pixel detector will play a central role in the event selection, with fast and efficient tracking algorithms being central to the ability of the computing farm to process full events at 30 MHz rate. Online alignment and calibration procedures will be mandatory as well as event reduction to optimise the bandwidth to storage. In addition, the resolution and tracking performance offered by the pixel detector is required to be at least as good - at higher occupancies and rates - than the current strip detector, in order to maintain the excellent performance of the LHCb detector in the areas of heavy flavour physics.

The pixel detector has been studied in detail and the enhancement in tracking and pattern recognition performance has been quantified. The impact of the material budget and the pixel resolution has been assessed, and performance parameters of the ASIC such as pile up and spillover have been related to the expected physics performance. The way in which the pixel detector enhances the speed and efficiency of the detector, as well as the physics performance, will be presented.

LHCb is also looking beyond the current upgrade, and considering in particular what the new technological possibilities for hybrid pixel detectors can contribute towards enabling LHCb to run at even higher luminosity. This includes concepts such as a move to 65 nm CMOS technology, improving the time stamping in pixels to improve pattern recognition and distinguish pile up vertices at high luminosity running, or the use of TSVs to improve the material budget, detector packaging and high speed signal routing. The possible impact of such applications on the future LHCb physics programme will be discussed.

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Overview and perspectives of HR/HV CMOS

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CMOS pixel sensors with a notable depletion layer have seen a large R&D focus in recent years. These devices promise competitive performance to hybrid pixel detectors without the need of hybridization, thus offering cost savings especially for large area coverage, e.g. in outer detector layers at the HL-LHC experiments. Many prototypes in various CMOS and SOI technologies have been fabricated with different starting substrate materials. Good performance even after large irradiation levels (ionizing as well as non-ionizing) has been demonstrated.

This overview talk presents the main ideas and approaches as well as the latest results from prototyping R&D, including the difficulties and drawbacks that such devices can have.

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Ultra-light mechanical supports for pixel modules

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Pixel detectors of the past decade were typically 2.0% X0 per layer. Intense R&D efforts over the past few years have brought this down to under 1.0% per layer for hybrid pixels despite an increase in their power density; detectors using MAPS, with their lower power densities are capable of 0.3% X0 for inner most layers. A survey of hybrid and monolithic pixel supports from recent and near future detectors will be presented as well as the R&D efforts into materials and fabrication techniques allowing them to achieve this new regime of mass reduction.

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PRIMARY VERTEX RECONSTRUCTION WITH THE ATLAS DETECTOR

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Efficient and precise reconstruction of the primary vertex in an LHC collision is essential in both reconstruction of the full kinematic properties of a hard-scatter event and in reconstruction of soft interactions as a measure of the amount of pile-up. The reconstruction of primary vertices in the busy, high pile-up environment of Run-2 of the LHC is a challenging task. The algorithms developed by the ATLAS experiments to reconstruct vertices in such environments, in particular the reconstruction of multiple vertices with small spatial separation, will be presented. Additionally data-driven methods to evaluate vertex resolution will be presented with a special focus on correct methods to evaluate the effect of the beam spot constraint; results from these methods in Run-2 data will be presented.

3

Silicon pixel-detector RandD for CLIC

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The physics aims at the future CLIC high-energy linear e+e- collider set very high precision requirements on the performance of the vertex and tracking detectors. Moreover, these detectors have to be well adapted to the experimental conditions, such as the time structure of the collisions and the presence of beam-induced backgrounds. The principal challenges are: a point resolution of a few μm , ultra-low mass ($\sim 0.2\%$ X0 per layer for the vertex region and $\sim 1\%$ X0 per layer for the outer tracker), very low power dissipation (compatible with air-flow cooling in the inner vertex region) and pulsed power operation, complemented with ~ 10 ns time stamping capabilities. A highly granular all-silicon vertex and tracking detector system is under development, following an integrated approach addressing simultaneously the physics requirements and engineering constraints. For the vertex-detector region, hybrid pixel detectors with small pitch ($25 \mu\text{m}$) and analog readout are explored. For the outer tracking region, both hybrid concepts and fully integrated CMOS sensors are under consideration. The feasibility of ultra-thin sensor layers is validated with Timepix3 readout ASICs bump bonded to active edge planar sensors with $50\text{-}150 \mu\text{m}$ thickness. Prototypes of CLICpix readout ASICs implemented in 65 nm CMOS technology with $25 \mu\text{m}$ pixel pitch have been produced. Hybridisation concepts have been developed for interconnecting these chips either through capacitive coupling to active HV-CMOS sensors or through bump-bonding to planar sensors. Recent R&D achievements include results from beam tests with all types of hybrid assemblies. Simulations based on Geant4 and TCAD are used to validate the experimental results and to assess and optimise the performance of various detector designs. The R&D project also includes the development of through-silicon via (TSV) technology, as well as various engineering studies involving thin mechanical structures and full-scale air-cooling tests. An overview of the R&D program for silicon detectors at CLIC will be presented.

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The STAR Pixel detector

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The PiXeL detector (PXL) of the STAR experiment at RHIC is the first application of the state-of-the-art thin Monolithic Active Pixel Sensors (MAPS) technology in a collider environment. Designed to extend the STAR measurement capabilities in the heavy flavor domain, it took data in Au+Au collisions, p+p and p+Au collisions at $\sqrt{s_{NN}} = 200 \text{ GeV}$ at RHIC, during the period 2014-2016.

The PXL detector is based on $50 \mu\text{m}$ -thin MAPS sensors with a pitch of $20.7 \mu\text{m}$. Each sensor includes an array of nearly 1 million pixels, read out in rolling shutter mode in $185.6 \mu\text{s}$. The 170 mW/cm^2 power dissipation allows for air cooling and contributes to reduce the global material budget to 0.4% radiation length on the innermost layer.

Experience and lessons learned from construction and operations will be presented in this talk. Detector performance and results from 2014 Au+Au data analysis, demonstrating the STAR capabilities of charm reconstruction, will be shown.

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The performance measurements of INTPIX6 SOI pixel detector

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The measurement results of monolithic pixel detector INTPIX6, designed at KEK and fabricated in Lapis 0.2- μm Fully-Depleted, Low-Leakage Silicon-On-Insulator (SOI) CMOS technology, are presented. INTPIX6 consists of 896×1408 integrating type pixels, $12 \mu\text{m} \times 12 \mu\text{m}$ each. The detector prototypes were produced on three various silicon wafers CZ-n, FZ-n, FZ-p, with different resistivity and doping. In this work the comparison of general performance of these three prototypes is presented, with the detailed measurement results of the CZ-n prototype. Using ^{241}Am radioactive source the noise of readout electronic was measured, showing the ENC about $70\text{-}80\text{-}e^-$. A particular focus of this work is the radiation hardness of the SOI pixel detector. The INTPIX6 has been irradiated up to 300-krad dose and its performance has been continuously monitored during the irradiation.

Summary:

The SOI detector presented in this work is one of the INTPIX family which are designed at KEK and fabricated in Lapis 0.2- μm SOI CMOS technology. Three prototypes of INTPIX6 detectors fabricated on low resistivity wafers obtained by Czochralski method (CZ-n) and on high resistivity floating zone wafers (FZ-n, FZ-p) were measured and tested in Cracow. The measurements were focused on the INTPIX6 performance, reflected by the Equivalent Noise Charge (ENC), as a function of radiation dose.

INTPIX6 is a general purpose integration type pixel with a simple data processing circuitry to reduce pixel size and obtain better spatial resolution. The whole matrix is 896×1408 with pixel dimension $12 \mu\text{m} \times 12 \mu\text{m}$. The detailed studies confirmed a full functionality of pixel detectors made on n-type doping wafer. The first measurements of the FZ-p type detector showed slightly worse performance and additional studies are needed to make further conclusions.

The INTPIX6 parameters were studied in detail with infrared laser and X-ray sources (^{241}Am and ^{55}Fe). All the measurements were taken at about -100V back bias voltage. The performed data analysis included common mode subtraction, single pixel gain correction and hit reconstruction. Such algorithm allowed to determine the ENC in range of $70\text{-}80\text{-}e^-$ for the measurements done at room temperature and with $10\text{-}\mu\text{s}$ integration time. This result is comparable to the state of the art pixel detectors. The ENC did not change significantly for different integration times, so the mean source of noise does not come from pixel leakage current.

The performance of the detector was studied during X-ray irradiation of the pixel matrix up to 300 krad dose. The detector showed very good performance, reflected by its small ENC and negligible number of bad pixels, up to 100-krad dose. Above this value the number of noisy pixels started to increase significantly but the detector was still alive giving reasonable response to laser and X-ray signal even after 300-krad dose.

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This talk will be a overall review of recent progress of RD53 Collaboration. Results obtained on the study of the radiation effects on 65nm CMOS have matured enough to defined first strategies to adopt in the design of analog and digital circuits. Critical IP-blocks and analog very front ends chains have been designed, tested before and after 5-800 MRad. Small prototypes of 64x64 pixels with a complex digital architectures have been produced, and point to address the main issues of dealing with extremely high pixel rates, while operating at very small in-time thresholds in the analog front end. The collaboration is now proceeding at full speed towards the design of a large scale prototype, called RD53A, in 65nm CMOS technology.

Summary:

The scope of CERN/RD53 collaboration is the development of pixel readout Integrated Circuits (IC) for the next generation of pixel readout chips to be used for the ATLAS and CMS Phase 2 pixel detector upgrades and future CLIC pixel detectors. The IC challenges include: smaller pixels to resolve tracks in boosted jets, very high hit rates due unprecedented particle fluence, much higher output bandwidth, radiation and large IC format with low power consumption in order to instrument large areas while keeping the material budget low. Nineteen institutes from nine countries, for a total of about 120 members are part of RD53, coming from CMS and ATLAS experiments.

This talk will be a overall review of recent progress of RD53 and the preparation towards the large scale prototype, called RD53A, in 65nm CMOS technology. Principal outcomes of the characterization of the radiation effects on electronics will be remind here, together with strategy adopted in the design of analog and digital circuits.

A total of 15-20 IP-blocks have been identified of interest for future pixel chips and four different designs of very front end analog chains have been developed, each one adopting a different architecture. All crucial IP-blocks and very front end analog chains needed for RD53A production have been designed and sent for production: most of those have been successfully tested before and after 5-800Mrad total dose: an extraction of main results will be presented.

Two small size demonstrators, consisting of a matrix of 64x64 pixels each of dimension 50x50 um² have been designed as intermediate step, and point to address in a complementary way to: address the low noise, low in-time threshold (1000e-) performance; integrate the different analog front end chains and of several IP-blocks developed; to develop a complex digital architecture with high efficiency for the very high pixel rate of 3 GHz/cm² foreseen in the inner layer of HL-LHC pixel detectors. One of the demonstrators (FE65-P2) has been produced and it is now under test; the other one (CHIPIX65) will be submitted for production in June.

The design of RD53A is on going, with a team of about ten designers working together. Main strategies, progresses and challenges will be presented.

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CMS Pixel Detector design for HL-LHC

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The LHC machine is planning an upgrade program which will smoothly bring the luminosity at about $5 \cdot 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ in 2028, to possibly reach an integrated luminosity of 3000 fb^{-1} by the end of 2037.

This High Luminosity scenario, HL-LHC, will present new challenges in higher data rates and increased radiation.

In order to maintain its physics reach the CMS Collaboration has undertaken a preparation program of the detector known as Phase-2 upgrade. The CMS Phase-2 Pixel upgrade will require a high bandwidth readout system and high radiation tolerance for sensors and on-detector ASICs. Several technologies for the upgrade sensors are being studied. Serial powering schemes are under consideration to accommodate significant constraints on the system. These prospective designs, as well as new layout geometries that include very forward pixel discs, will be presented together with performance estimations.

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Large Area Thinned Planar Sensors for Future High-Luminosity-LHC Upgrades

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Planar hybrid silicon sensors are a well proven technology for past and current particle tracking detectors in HEP experiments. However, the future high-luminosity upgrades of the inner trackers at the LHC experiments pose big challenges to the detectors. A first challenge is an expected radiation damage level of $2E16 \text{ n}_{\text{eq}}/\text{cm}^2$. For planar sensors, one way to counteract the charge loss and thus increase the radiation hardness is to decrease the thickness of their active area. A second challenge is the large detector area which has to be built as cost efficient as possible, i.e. it is aimed for low-cost and large-sized sensors.

The CiS research institute has accomplished a proof-of-principle run with n-in-p ATLAS-Pixel sensors where cavities are etched to the sensors back side to reduce its thickness. One advantage of this technology is that thick frames remain at the sensor edges and guarantee mechanical stability on wafer level while the sensor is left on the resulting thin membrane. During the dicing step, the frames can be removed in order to obtain completely thin sensors. For this cavity-etching technique, no handling wafers are required which represent a benefit in terms of process effort and cost savings. The membranes with areas of up to $\sim 4 \times 4 \text{ cm}^2$ and target thicknesses of 100 and 150 μm feature a sufficiently good homogeneity across the whole wafer area. The processed pixel sensors show good electrical behaviour with an excellent yield for such a prototype run. First sensors with electroless Ni- and Pt-UBM are already successfully assembled with read-out chips. The technology is currently transferred to 6" wafer size. First results of etching trials with dummy wafers with larger thinned areas will be shown as well.

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Ultra fast silicon timing detectors: status and future developments

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The Ultra Fast Silicon Detectors (UFSD) are a novel concept of silicon detectors based on the LGAD technology, which are able to obtain time resolution of the order of few tens of picoseconds. First prototypes with different geometries (pads/pixels/strips), thickness (300 and 50 μm) and gain (between

5 and 20) have been recently designed and manufactured by CNM (Barcelona) and FBK (Trento). Several measurements have been performed in laboratory and in test beam on these devices. First results on sensor characteristics (leakage current, breakdown voltage, gain/doping profile) and time resolution will be discussed and compared to simulation. The issue of the radiation hardness will be addressed and plan for future productions will be discussed.

The expected time resolution, the low material budget and the possibility of segmentation make USFD very interesting candidates for the measurement of the proton time-of-flight in the Precision Proton Spectrometer (CT-PPS). The application of the UFSD in this contest will be discussed.

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The Phase1 CMS Pixel detector upgrade

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The innermost layers of the CMS tracker are built out of pixel detectors arranged in three barrel layers (BPIX) and two forward disks in each endcap (FPIX). The original CMS detector was designed for the nominal instantaneous LHC luminosity of $1 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. Under the conditions expected in the coming years, which will see an increase of a factor two of the instantaneous luminosity, the CMS pixel detector will see a dynamic inefficiency caused by data losses due to buffer overflows. For this reason the CMS Collaboration has been building a replacement pixel detector which is scheduled for installation in an extended end of year shutdown during Winter 2016/2017.

The Phase I upgrade of the CMS pixel detector will operate at full efficiency at an instantaneous luminosity of $2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ with increased detector acceptance and additional redundancy for the tracking, while at the same time reducing the material budget. These goals are achieved using a new readout chip and modified powering and readout schemes, one additional tracking layer both in the barrel and in the disks, and new detector supports including a CO₂ based evaporative cooling system, that contribute to the reduction of the material in the tracking volume.

This contribution will review the design and technological choices of the Phase I detector, and discuss the status of the construction of the detector and the performance of its components as measured in test beam and system tests. The challenges and difficulties encountered during the construction will also be discussed, as well as the lessons learned for future upgrades.

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Custom ultrasonic instrumentation for flow measurement and real-time binary gas analysis in the CERN ATLAS Experiment

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The development of a custom ultrasonic instrumentation was motivated by the need for continuous real-time monitoring of possible leaks and mass flow measurement in the evaporative cooling systems of the ATLAS silicon trackers. The instruments use a pairs of ultrasonic transducers transmitting sound bursts and measuring transit times in opposite directions. The gas flow rate is calculated from the difference in transit times, while the sound velocity is deduced from their average. The gas composition is then evaluated by comparison with a sound velocity/composition database, based on the direct dependence between sound velocity and component molar concentration in a gas mixture at a known temperature and pressure. The instrumentation has been developed in several different geometries.

Five instruments are now integrated in the ATLAS Detector Control System (DCS). Three of these monitor C3F8 and CO2 coolant leaks into N2 envelopes of the SCT, IBL and Pixel detectors. Resolutions better than $2 \cdot 10^{-5}$ and 10^{-4} are respectively seen for C3F8 and CO2 leak concentrations in N2. A fourth instrument detects sub-percent levels of air ingress into the C3F8 condenser of the new thermosiphon coolant recirculator. Following extensive CFD studies a fifth instrument was built as an angled sound path flowmeter to measure the high returning C3F8 vapour flux ($\sim 1.2 \text{ kg.s}^{-1}$) to the thermosiphon condenser. A precision of $< 2.3\%$ F.S. for flows up to 10 m.s^{-1} was demonstrated. This instrument should also be capable of determining the concentrations of C3F8 and C2F6 to better than $\pm 3 \cdot 10^{-3}$ should such blends be needed to reduce the operating temperature of the SCT and Pixel detectors for enhanced radiation tolerance. Custom microcontroller-based readout has been developed for the instruments, allowing readout into the ATLAS DCS via Modbus TCP/IP on Ethernet. These instruments have many potential applications where continuous binary gas composition measurement is required, including hydrocarbon and anaesthetic gas mixtures.

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Toward HL-LHC: strategies for DAQ and track triggers

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The readout of pixel detectors at HL-LHC and the use of extracted data in the context of a track trigger are one of the big challenges for the next generation of trackers due to the enormous data volume produced and to the high trigger rate. In this talk, I will analyze the solutions that ATLAS and CMS are exploring. I will also show how new detector and data transmission technologies could, in a not too distant future, open new possibilities for the use of pixel detectors in data filtering.

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Low energy and high resolution performance of the MOENCH hybrid pixel detector

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MÖNCH is a hybrid silicon pixel detector based on charge integration and with analog readout, featuring a pixel size of 25×25 μm². The latest working prototype consists of an array of 400×400 identical pixels for a total active area of 1×1 cm². Its design is optimized for the single photon regime. An exhaustive characterization of this large area prototype has been conducted in the past months, and it confirms an ENC in the order of 35 electrons RMS and a dynamic range of ~4×12 keV photons in high gain mode, which increases to ~100×12 keV photons with the lowest gain setting.

The low noise levels of MÖNCH make it a suitable candidate for X-ray detection at energies around 1 keV and below. Its energy reconstruction and imaging capabilities have been tested for the first time at a low energy beamline at PSI, with photon energies between 1.75 keV and 3.5 keV, and results will be shown.

Imaging applications in particular can benefit significantly from the use of MÖNCH: due to its extremely small pixel pitch, the detector intrinsically offers excellent position resolution. Moreover, in low flux conditions, charge sharing between neighboring pixels allows the use of position interpolation algorithms which grant a resolution at the micrometer-level. Therefore, in order to precisely quantify the position resolution achievable with this method, a dedicated scan across one pixel using an X-ray beam with ~100 nm wide focus has been conducted. The outcomes of this test will also be presented. The same scan also provided a first indication of the radiation hardness of the device, and with its nanometric focal spot provided a good opportunity to identify possible radiation sensitive pixel components.

Finally, the prospects for future design optimization and commissioning of a larger area module will be discussed.

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IBEX: New Pixelated Photon Counting ASIC for X-ray Imaging

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We carried out a comprehensive characterization of an innovative hybrid photon counting (HPC) detector with a CdTe sensor for spectral imaging applications. The detector features the IBEX ASIC, developed at DECTRIS Ltd., with either a pixel size of 75 μm×75 μm and two thresholds per pixels, or a pixel size of 150 μm×150 μm with four thresholds. The front-end electronics is compatible with both the hole and electron collection mode required by Silicon and High-Z sensors, respectively, and the input dynamic range extends up to a threshold of 140 keV. A double-buffered counter allows for a continuous read-out with a sub-μs dead-time. The instant retrigger technology enables non-paralyzable counting achieving count rates well above 10⁷ cts/pixel/s. The chip dimensions are 2 cm×2 cm and large-area detectors can be designed by tiling chips together with minimal dead area. We investigated detectors of 75 μm×75 μm pixel size both in our in-house laboratory and at synchrotron facilities over a wide range of energies.

Quantum efficiency (QE), energy and spatial resolution and the count rate capabilities were measured.

The QE reflects the properties of the sensor material. For CdTe it is close to 100% at energies below the Cd and Te K-edges, where it suddenly decreases. It is however 60% at 95 keV for a 1mm-thick

sensor.

The energy resolution at 20 keV lies at 2.3 keV FWHM and worsens slightly for incoming energies above the K-edges.

Modulation transfer functions (MTF) were measured with direct x-ray W-tube beam in the range 40-60 kVp using the slanted-edge technique. In virtue of the direct photo-conversion the spatial resolution exceeds the resolution of a CMOS flatpanel detector with similar pixel size by a large factor. Finally, the instant retrigger technology –which allows for a non-paralyzable counting mode –extends a prompt count rate above 10^7 cts/s/pixel, corresponding to an incoming flux of above $1.7 \cdot 10^9$ cts/s/mm² for 75 μ m pixels.

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Automatic Pad Cleanness Detection using Fuzzy C-Means Clustering

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Inner Tracking System (ITS) for ALICE (A Large Ion Collider Experiment) uses more than 24 thousands pixel chip detectors. Each chip composed of 103 pad detectors with thickness of 50 micro meters. To ensure the quality of the detectors, automatic visual chip inspection is needed to detect defects that happen during mass production and pickup. Several steps are performed for automatic visual inspection. First, Fourier based template matching is used to detect the position of the pad inside the image. After that, Fuzzy c-means (FCM) is used to cluster the presented on the pad found. The RGB information on each pixel is used as input for the FCM. The number of cluster defined for the FCM is 3 because each cluster will represent the die edge, the pad, and the defect. From the color of the cluster centers found, the defect is determined as the darkest color among the other clusters. From the experiment, it is shown that the proposed approach can achieve average accuracy of 90%.

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Development of Visual Inspection System for Detecting Surface Defects on Sensor Chip

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This study presents a visual inspection method based on image processing to detect surface defects found on pixel chip pad. Pixel chip is a particle detector used in Inner Tracking System (ITS) which is part of ALICE experiment (A Large Ion Collider Experiment). The quality of chip including the surface pad quality has to well assessed in order to guarantee the successfulness of the overall experiments. A large number of pixel chips are used in ITS which demands both quick and accurate tests of the surface pad. Therefore, an effective inspection technique is needed to address such a problem. This paper proposes a design approach to assess the quality of surface pad by using image processing techniques. The design approach consists of three steps. Firstly, K- Means is employed to divide the surface pad into clean and defect areas. Secondly, defect area is extracted by using Gabor

filter. Lastly, Canny Edge filter is executed to detect the defects of the defect area. Experimental results show that the proposed approach can achieve significantly high accuracy and recall probability which are by 84.9% and 77.9% respectively.

Summary:

ALICE (A Large Ion Collider Experiment) is an experiment at CERN (Conseil Européen pour la Recherche Nucléaire), Switzerland that is designed to address the physics of strongly interacting matter and properties of the Quark-Gluon Plasma (QGP) using proton-proton, proton-nucleus and nucleus-nucleus collisions. In this experiment, a Large Hadron Collider (LHC) is used to accelerate two beams in opposite direction. The collision produces billion of particles with scattered trajectories, in which those particles need to be tracked and then identified.

The LHC apparatus consist of a central barrel, a forward muon spectrometer and a set of small detect

The pALPIDEfs design is used for particles detector. This design has dimension 15x30 mm/-2 for a single chip and 103 contact region with 200 μ m of diameter. As we can see in Figure, 103 contact area is aligned on the chip. According to its thickness, manual inspection is very hard to be done, because of light in weight, and small in size. These contact area are gold plated, and coated with other material (silicon). As mentioned before, during the production process damages may happen with unexpected condition. Figure shows the contamination process during placement activities using vacuum pick up tool.

In accordance with the pad area diameter, microscope used for visual inspection system needs to reach an appropriate view with certain magnification (500x). This system will be applied in mass production process to avoid several damages. Visual inspection for chip quality assessment is widely applied in industrial application by automated inspection system.

The study is focused in visual inspection for chip pad area. It aims to detect contaminated or defe

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A new Data Acquisition System for the CMS Phase 1 Pixel Detector

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A new pixel detector will be installed in the CMS experiment during and extended technical stop of the LHC in the beginning of 2017. The new pixel detector, built from four layers in the barrel region and three layers on each end of the forward region, is equipped with upgraded front-end readout electronics, specifically designed to handle the high particle hit rates created in the LHC environment. The DAQ back-end was entirely redesigned to handle the increased number of readout channels, the higher data rates per channel and the new digital data format. Based entirely on the microTCA standard, new front-end controller (FEC) and front-end driver (FED) cards have been developed, prototyped and produced with custom optical link mezzanines mounted on the FC7 AMC and custom firmware. At the same time as the new detector is being assembled, the DAQ system is set up and its integration into the CMS central DAQ system tested by running the pilot blade detector already installed in CMS. This talk describes the DAQ system, integration tests and results, and an outline for the activities up to commissioning the final system at CMS in 2017.

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PFM2: a 32x32 Processor for X-ray Diffraction Imaging at FELs

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This work presents the results from the characterization of a readout chip for application to experiments at the next generation X-ray free electron laser (FEL). The ASIC, named PixFEL Matrix (PFM2), has been designed in a 65 nm CMOS technology and consists of 32x32 pixels. Each cell covers an area of 110x110 μm^2 and includes a low-noise charge sensitive amplifier (CSA) with dynamic signal compression, a time variant shaper used to process the signal at the preamplifier output, a 10-bit successive approximation register (SAR) analog-to-digital converter (ADC) and digital circuitry for channel control and data readout. Two different solutions for the readout channel, based on different versions of the time variant filter, have been integrated in the chip. Both solutions can be operated in such a way to cope with the high frame rate (exceeding 1 MHz) foreseen for future X-ray FEL machines. The ASIC will be bump bonded to a slim/active edge pixel sensor to form the first demonstrator for the PixFEL X-ray imager. This work has been carried out in the frame of the PixFEL project funded by Istituto Nazionale di Fisica Nucleare (INFN), Italy. The members of the PixFEL Collaboration are affiliated with Università di Bergamo, Università di Pavia, Università di Pisa, Università di Trento and INFN, Italy.

Summary:

The experimental environment at the next generation X-ray free electron laser (FEL) facilities requires that the electronic instrumentation be able to cope with very challenging specifications in terms of space and amplitude resolution, frame rate, input dynamic range, frame storage capability and radiation hardness. The PixFEL collaboration aims at developing a multilayer, hybrid pixel detector for X-ray diffraction imaging applications compliant with these severe requirements [1]. The sensing layer will be based on a fully depleted slim edge silicon pixel detector to minimize the dead area at the sensor edge. The readout processor will result from the vertical integration of two layers, one for the integration of the analog front-end and the ADC, the second one to dedicated memories used to accumulate data in applications with high X-ray pulse rates. In the first stage of the project, the main building blocks of the readout channel have been designed and successfully tested [2,3]. Moreover, the initial steps have recently been taken in the characterization of slim/active edge sensors from the first production batch [4].

Following the outcomes from the characterization of the first prototype front-end [2,3], a readout chip, consisting of 32x32 square cells and called PFM2, has been designed and submitted to the foundry at the end of March 2016. As for the prototype, a 65 nm CMOS technology has been chosen for the design of the PFM2 chip in order to accommodate all the pixel functionality in a pitch of 110 μm . Each cell includes a low-noise charge sensitive amplifier with dynamic signal compression, a time variant shaper, which implements a trapezoidal weighting function, a low power, small area 10-bit SAR converter, relying on a time interleaved method and elementary digital circuitry for channel control and data readout.

In the new chip, starting from the compression idea already validated with the first channel prototype, a more complex feedback network has been designed for the charge sensitive amplifier. The feedback transistor, responsible for the dynamically changing sensitivity of the CSA, is split into four devices with the same channel length and different channel widths. Three switches, in series with three of the four feedback elements and controlled with two programming bits through a binary-to-thermometric decoder, determine the total area of the feedback MOS capacitor. By a suitable choice of the configuration bits, the amplifier is made capable of processing signals from photons at 1, 2, 4 or 10 keV while preserving its capability of complying with an input dynamic range of 1 to 10^4 photons.

Two different solutions of the time variant shaper have been integrated in the PFM2 chip. Half of the cells in the 32x32 array is equipped with the filter already implemented and tested in the channel prototype, based on a transconductor, which converts the voltage at the output of the CSA into a current, and on the so called flip-capacitor filter (FCF) [5]. The other half of the array incorporates a new version of the time variant shaping stage named differential gated integrator (DGI). The new proposed architecture is based on a differential integrator designed around the same forward gain block already implemented for the FCF. The two input terminals of the differential integrator are switched between the reference voltage (V_{ref}) and the output of the CSA (V_a) to obtain, by means of a correlated double sampling (CDS) technique, a trapezoidal weighting function. More in details, during the baseline integration interval, the non-inverting input of the DGI is connected to the output of the CSA, whereas the other terminal

is shorted to V_{ref} . In the subsequent signal settling interval, both the terminals are left floating while the charge generated in the detector by the diffracted laser pulse induces a signal at the CSA input. A second integration is performed in the subsequent period, during which the inverting input of the DGI is connected to the CSA output and the non-inverting terminal is connected to the reference voltage. At the end of this time interval, the amplitude of the signal at the output of the DGI block (V_o) is proportional to the difference between the CSA output level after the photon signal arrival (V_{a+}), and the baseline level (V_{a-}): $V_o = V_{ref} + (T/RC)(V_{a+} - V_{a-})$, where T is the integration time and R and C are the resistance and the capacitance in the differential integrator. At the end of the cycle, after the voltage level has been sampled by the ADC, the feedback capacitances of the charge sensitive amplifier and of the filter are reset. The new filter has been simulated by referring to the target processing frequency of 5 MHz of the European XFEL. The total power consumption for the channel with the DGI (including the ADC) is about 230 μ W for an integration time of 50 ns (a quarter of the minimum processing period of 200 ns), to be compared to the 350 μ W power dissipation for the channel with transconductor and FCF.

At the time of the conference, besides discussing in detail the readout channel and array architecture, results from the experimental characterization of the chip will be presented.

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Edge-on illuminated silicon pixel detector for medical imaging

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Aim of our project is to contribute in the improvement of X-ray Computed Tomography, making the detection process more efficient, in order to reduce the dose delivered to the patient. The benefits of switching from indirect to direct detection of photons and from Charge Integrating to Photon Counting mode have already been proven by several groups. Counting the number of photons instead of measuring the total deposited energy enhances the quality of the image, especially for soft tissues. Our goal is to prove the feasibility and assess the experimental advantages of such a setup in Computed Tomography.

We use a 500 μ m thick silicon sensor in edge-on illumination coupled to a Medipix readout chip. This geometry consists in illuminating the detector from the side and it is required in order to compensate

for the low attenuation efficiency of silicon for photons of energy above 30 keV. In addition to increasing the volume per unit area, with this configuration, partial energy discrimination is obtained. Spectral energy measurements may form a powerful tool in this field.

A custom reconstruction algorithm has been developed in collaboration with CWI. Using the attenuation model and the detector energy response function, it is possible to exploit the depth segmentation, to obtain a reconstructed image for different energy intervals. This result will be more enhanced when switching to a readout chip (the Medipix3 chip) that allows different energy threshold to be set.

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Status of HVCMOS Sensor Developments for ATLAS

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The HVCMOS sensors are a type of CMOS active sensors where signal generation occurs in depleted silicon. HVCMOS sensors are fast and radiation tolerant, mostly due to use of large pixel electrodes and high depletion voltage that leads to uniform and strong electric field and fast charge collection. The development of these sensors started in 2006 and they are now seen as an option to the standard sensor technologies such as hybrid- or strip-detectors for several particle physics experiments, among others ATLAS and CLIC. For Mu3e experiment HVCMOS is the main technology.

In the last year there were several important achievements in HVCMOS development - for instance the design and production of the first reticle-size HVCMOS sensor in AMS H35 technology –H35DEMO that was performed in collaboration between Universities of Bern, Geneva, Liverpool, KIT and CERN. H35DEMO can be readout either as a monolithic detector, with the readout electronics implemented on the sensor chip, or attached to an external readout chip. In the latter case, capacitive signal transmission between the sensor- and the readout-chip can be used. The sensor has been implemented on four different substrates from the standard low-resistivity substrate to the >k Ohm cm substrate. The main purpose of H35DEMO project is to demonstrate that a large HVCMOS sensor fulfils the ATLAS specifications and to show that HVCMOS is a reliable and mature technology. H35DEMO is currently being tested in our group and the first results are encouraging. For instance, we measure significantly better signal to noise ratio than with the previous smaller prototypes, the time resolution is also better.

In 2016 the first HVCMOS reticle-size prototype for the ATLAS strip layers has been also designed and submitted. The goal of this project, performed in collaboration of ATLAS strip groups and us, is to design a segmented strip detector - a pixel detector with long pixels - that can replace the strip sensors.

In parallel to the characterization of H35DEMO, we are already working on several more advanced large-area monolithic sensors that contain all the features necessary for the use in the ATLAS experiment. The submission of these designs is planned for Summer 2016. The designs are optimized according to several application scenarios of HVCMOS sensors that are currently discussed between ATLAS groups: 1) The use of monolithic HVCMOS sensors in the outer pixel layers. 2) The use of capacitively- or DC-coupled pixel detectors based on a HVCMOS sensor and a new readout chip in the inner pixel layer. Here, the goal is a pixel size of 25 x 25 micrometers or less. 3) The use of HVCMOS segmented-strip monolithic sensors in the outer tracker regions. 4) The design of triplet layers.

For these application cases, novel electronic blocks have been developed: very small content addressable memory cells that can be used to keep the particle-hit information for relatively long time > 25 microseconds and to detect the coincidence of the hit information with a trigger signal, small HVCMOS pixels, high-rate and low-latency readout blocks and different circuits for enhancement of time resolution.

This contribution will present the status of the project; the architecture and the design details of the new sensors will be described as well. In the second part of the contribution the results of latest measurements performed at KIT will be presented. The measurement results of other collaboration partners will be presented in the talk of Dr. Vilella Figueras.

Summary:

The HVCMOS sensors are a type of CMOS active sensors where signal generation occurs in depleted silicon. HVCMOS sensors are fast and radiation tolerant, mostly due to use of large pixel electrodes and high depletion voltage that leads to uniform and strong electric field and fast charge collection. The development of these sensors started in 2006 and they are now seen as an option to the standard sensor technologies such as hybrid- or strip-detectors for several particle physics experiments, among others ATLAS and CLIC. For Mu3e experiment HVCMOS is the main technology.

In last year there were several important achievements in HVCMOS development: For instance the design and production of the first reticle-size HVCMOS sensor in AMS H35 technology –H35DEMO that was performed in collaboration between Universities of Bern, Geneva, Liverpool, KIT and CERN. H35DEMO can be readout either as a monolithic detector, with the readout electronics implemented on the sensor chip, or attached to an external readout chip. In the latter case, capacitive signal transmission between the sensor- and the readout-chip can be used. The sensor has been implemented on four different substrates from the standard low-resistivity substrate to the >k Ohm cm substrate. The main purpose of H35DEMO project is to demonstrate that a large HVCMOS sensor fulfils the ATLAS specifications and to show that HVCMOS is a reliable and mature technology. H35DEMO is currently being tested at KIT and the first results are encouraging. In parallel to the characterization of H35DEMO, we are already working on several more advanced large-area monolithic sensors that contain all features necessary for the use in the ATLAS experiment. The submission of these designs is planned for Summer 2016.

This contribution will present the status of the project; the architecture and the design details of the new sensors will be described as well. In the second part of the contribution the results of latest measurements performed at KIT will be presented.

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Evaluation of a pulse counting type SOI pixel using synchrotron radiation X-rays

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Application of the Silicon-On-Insulator (SOI) technology [1] to a pixelated detector for imaging experiments using Synchrotron X-rays is expected as a good method for developing a fine pixelated detector because there is no mechanical bump bonding in the SOI device. The first beam test for a

proto type chip of a pulse counting type SOI pixel, CPIXTEG3b, was performed in BL-14A at Photon Factory, KEK. CPIXTEG3b was designed under the Double-SOI technology [2] for defensing from the cross talk and increasing the radiation hardness. It has a 64×64 -pixel array where the area size of each pixel is $50 \mu\text{m} \times 50 \mu\text{m}$. Sensitivity for X-rays respect to the incident position in a pixel was measured with the pencil beam having a diameter of $10 \mu\text{m}$ at 8 keV and 16 keV of X-ray energy. Because of its small size of a pixel, this data also contained the charge sharing effect. Hence this data could be used for a study of the point spread function. Response of the discriminator in the analogue circuit of the pixel was calibrated by the electric pulse and this result was checked about all pixels by use of the flat field beam.

In this conference, we will introduce some results of this performance tests.

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HV-CMOS pixel detectors in BCD8 technology

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This paper describes the first pixel detectors realized with the BCD8 technology by STMicroelectronics.

The BCD8 is a 160 nm process integrating bipolar, CMOS and DMOS devices and it is mostly used for automotive application. A version with 70 V voltage capability has been tested to evaluate its suitability for the realization of CMOS sensors with a depleted region of several tens of micrometer. Sensors featuring $50 \times 250 \mu\text{m}^2$ pixels on a $125 \Omega\text{cm}$ resistivity substrate have been characterized showing a uniform breakdown at 70 V before irradiation, as expected by design in this technology, and a capacitance of about 80 fF at 50 V reverse bias voltage.

The response to ionizing radiation is tested using radioactive sources and an X-ray tube, reading out the detector with an external spectroscopy chain. At the nominal 50 V bias, the device can detect soft X-rays, whose ionization yield is comparable to a minimum ionizing particle in the depletion region, demonstrating the detector is suitable also for charged particle detection and tracking application. Irradiation tests were performed up to proton fluences exceeding $5 \times 10^{15} \text{p/cm}^2$ and they show that depletion and breakdown voltages increase with irradiation.

The presentation will review the main results of the sensor performance characterization and radiation hardness measurement, as well as the design of an integrated front-end electronics, including a charge preamplifier, a comparator and a threshold tuning DAC, that can be coupled to the ATLAS FE-I4 chip for readout.

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ATLAS TRACK RECONSTRUCTION IN DENSE ENVIRONMENTS AND ITS INEFFICIENCY MEASUREMENTS USING PIXEL DE/DX

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ATLAS track reconstruction code is continuously evolving to match the demands from the increasing instantaneous luminosity of LHC, as well as the increased centre-of-mass energy. With the increase in energy, events with dense environments, e.g. the cores of jets or boosted tau leptons, become much more abundant. These environments are characterised by charged particle separations on the order of ATLAS inner detector sensor dimensions and are created by the decay of boosted objects. Significant upgrades were made to the track reconstruction code to cope with the expected conditions during LHC run 2. In particular, new algorithms targeting dense environments were developed. These changes lead to a substantial reduction of reconstruction time, while at the same time improving physics performance. The employed methods are presented and the prospects for future applications are discussed. In addition physics performance studies are shown, e.g. a measurement of the fraction of lost tracks in jets with high transverse momentum. The method uses the ionization loss per unit length (dE/dx) in the silicon sensors to determine the fraction of lost tracks.

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The ATLAS Insertable B-Layer: from construction to operation

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ATLAS IBL is a fourth layer of pixel detectors, and has been installed in May 2014 at a radius of 3.3 cm between the existing Pixel Detector and a new smaller radius beam-pipe. The new detector, built to cope with high radiation and occupancy, is the first large scale application of 3D detectors and CMOS 130nm technology. The IBL detector construction was achieved within about two years starting from mid-2012 to the May 2014 installation in ATLAS, a very tight schedule to meet the ATLAS installation and detector closure before starting the Run2 in Spring 2015. The key features and challenges met during the IBL project will be presented, as well as its commissioning and operational experience in LHC.

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Development of a Detector Control System for the ATLAS Pixel detector in the HL-LHC

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The upgrade of the LHC to the High-Luminosity LHC (HL-LHC) requires a new inner tracking detector (ITk). The innermost part of this new tracker is a pixel detector. The University of Wuppertal is developing a new detector control system (DCS) to monitor and control this new pixel detector. The current concept envisions three parallel paths of the DCS. The first path, called security path, is hardwired and provides an interlock system to guarantee the safety of the detector and human beings. The second path is a control path. This path is used to supervise the entire detector. The control path has its own communication lines independent from the regular data readout for reliable operation. The third path is for diagnostics and provides information on demand. It is merged with

the regular data readout and provides the highest granularity and most detailed information. To reduce the material budget, a serial power scheme is the baseline for the pixel modules. A new ASIC used in the control path is in development at Wuppertal for this serial power chain. A prototype exists already and a proof of principle was demonstrated. Development and research is ongoing to guarantee the correct operation of the new ASIC in the harsh environment of the HL-LHC. The concept for the new DCS will be presented in this talk. A focus will be made on the development of the DCS chip, used for monitoring and control of pixel modules in a serial power chain.

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Radiation-Hard/High-Speed Parallel Optical Links

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We have designed an ASIC with four radiation-hard drivers to operate a VCSEL array at 10 Gb/s for possible applications in the pixel detector of ATLAS at HL-LHC. The ASIC has been fabricated in a 65 nm CMOS process. We have also designed an optical module that couples the ASIC to a VCSEL array. The optical module had been exposed to an intense beam of protons to study the radiation hardness of the high-speed optical links. The irradiated devices will be extensively characterized after the radiation cool down. We will present the results from the study.

Summary:

The LHC at CERN is now the highest energy and luminosity collider in the world. The collider and detectors have recently completed an upgrade to operate at higher energy and luminosity. In addition, there are plans to further upgrade the collider and detectors to operate at even higher energy and luminosity. This requires the optical links to transmit data at much higher speed to handle the much increased luminosity. We will present results from an R&D program for a possible application in the optical link upgrade for the pixel detector of the ATLAS experiment.

We have designed an ASIC that contains an array of four high-speed/radiation-hard drivers to operate a VCSEL (Vertical Cavity Surface Emitting Lasers) array. The bandwidth of each driver is 10 Gb/s. The ASIC has been fabricated using a 65 nm CMOS process. We have designed an optical module, opto-board, to characterize the ASIC. The opto-board is a high-speed version of the optical modules that have been successfully deployed in two generations of optical links for the pixel detectors of the ATLAS experiment. We have characterized the performance of the ASIC at 10 Gb/s. Although the ASIC is operational at 10 Gb/s, some improvements would be needed. However, the performance of the ASIC is quite satisfactory at 5 Gb/s, the target bandwidth for the pixel detector of the ATLAS experiment at the high-luminosity LHC.

We have irradiated some ASICs on opto-boards with and without VCSEL arrays using 24 GeV/c protons. The total ionized dosages are 10 and 74 Mrad, respectively. This irradiation scheme will allow us to study the degradation of the ASIC and VCSEL separately for high-speed operation. We will present the performance of the ASICs before and after irradiation.

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Operational Experience with the CMS Pixel detector

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The CMS pixel detector was repaired, calibrated and commissioned successfully for the second run of Large Hadron Collider. The replaced modules were calibrated separately and showed the expected behavior of an un-irradiated detector. In 2015 the system performed excellent with an even improved hit efficiency and spatial resolution compared to Run I. During this time, the operational team faced various challenges including the loss of a sector in one half shell which was partially recovered. This year the detector is expected to withstand luminosities that are beyond its design limits and will need a combined effort of both online and offline team to yield the high quality data that is required to reach our physics goals. In parallel, the Phase I pilot system was commissioned and used to prepare for the imminent upgrade of the detector. We present the experience gained during the second run of the LHC and show the latest performance results of the CMS pixel detector.

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Readout electronics and test bench for the CMS Phase I pixel detector

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The present CMS pixel detector will be replaced with an upgraded pixel system during the LHC extended technical stop in winter 2016/2017. The CMS Phase 1 pixel upgrade combines a new pixel readout chip, which minimizes detection inefficiencies, with several other design improvements to maintain the excellent tracking performance of CMS at the higher luminosity conditions foreseen for the coming years. The upgraded detector features new readout electronics which require detailed evaluation. For this purpose a test stand has been setup, including a slice of the CMS pixel DAQ system, all components of the upgraded readout chain together with a number of detector modules. The test stand allows for detailed evaluation and verification of all detector components, and is also crucial to develop tests and procedures to be used during the detector assembly and the commissioning and calibration of the detector. In this talk the system test and its functionalities will be described with a focus on the tests performed for the barrel pixel detector. Furthermore, the assembly and integration of the readout electronics for the final detector system will be presented.

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3D Integration Technology using Through Silicon Vias for Hybrid Pixel Detector Modules

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Hybrid pixel detector modules are the main building blocks of silicon particle tracking detectors in high energy physics experiments as well as in x-ray cameras for research and development using synchrotron radiation. Wire bonding is used so far to connect the readout ICs to the detector services. The 3D integration technology with through-silicon-vias (TSVs) offers several advantages in terms of reduction of peripheral area of hybrid modules as well as reduction of signal path length for fast

signal readout. A via last approach for electronic readout ICs using copper-filled through-silicon-vias will be described in this presentation. Starting with the description of the individual process steps for TSV formation the specific details of the technology for different types of readout ASICs will be described. Due to the fact that the TSV connects the inner layers of the IC with the IO-redistribution layer of the chip backside the details of chip design has to be involved in the process development already at an early state. The application of TSV process will be shown on several types of electronic readout ASICs, i.e. ATLAS FE-I4B and MEDIPIX3. Depending on the status of process development at the time of presentation the talk will give the current state of test results of 3D integrated pixel detector modules.

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A 12-bit, 1 MS/s, Digitally-Calibrated SAR-ADC Used for CZT-Based Multi-Channel γ -Ray Imager

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In this paper, we focus on the design of a 12-bit 1 MS/s radiation-hardened, digitally-calibrated SAR-ADC used for CZT-based multi-channel γ -ray imager. A 64-channel CZT-based imaging system developed in our laboratory comprises a CZT-pixelated detector, a 64-channel front-end readout chip, 64 analog-to-digital converter (ADC) chips, a digital signal processor, and an image-reconstruction platform (e.g., workstation or PC). The output analog voltages of 64 channels front-end readout chip are simultaneously sampled and digitalized using the 64 low-power and high-resolution SAR-ADC chips.

The previous works in digitally-calibrated SAR-ADC usually adopt 1.86-radix capacitors in both LSB and MSB with perturbation technique. However, for LSB-weights calibration, since the input of analog signal is very small, the perturbation could be beyond the level of ground, and the calibration can not be realized. Considering that the variation of the LSB capacitors contributes insignificant errors to the conversion accuracy, the new DAC structure with 2-radix capacitors in LSB and 1.86-radix capacitors in MSB is adopted in the proposed SAR-ADC for digital bit-by-bit calibration. The weights of LSB are fixed at 2-radix, and the weights of MSB are digitally-calibrated by the bit-by-bit calibration technique using the weights of LSB.

Two radiation-hardened design technologies are utilized in the layout design to improve the radiation tolerance of the SAR-ADC. Firstly, the P+ and N+ guard rings are added in NMOS and PMOS transistors, respectively, the guard rings provide a path for the large current leakage which is caused by high energy particles, to prevent latch-up from occurring. Secondly, the distance between PMOS and NMOS transistors is increased as compared with the ordinary situation, which can increase the base region of the parasitic bipolar, thus can reduce the current amplification factor and can prevent latch-up from occurring.

A 12-bit 1 MS/s SAR-ADC prototype chip is designed and implemented in 0.35 μ m mixed-signal 3.3V/5V CMOS process. The die size of the SAR-ADC core is 856 μ m \times 802 μ m. Fast Fourier transform (FFT) techniques are used to test the dynamic performances of the ADC, including distortions and noises. When the frequency of the input sinusoidal signal is 9.9 kHz and the sampling rate is 1 MS/s, the simulation results show that, the signal-to-noise and distortion ratio (SINAD) is 70.10 dB and effective number of bits (ENOB) is 11.35-bit, the power dissipation of SAR-ADC is 3mW, and the figure of merit (FOM) is 1.15pJ/conversion-step.

The SAR-ADC developed in this paper is with the features of high precision, low power, small die size, and radiation-hardened, it can be used in the pixelated detector imaging system.

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High rate capability and radiation tolerance of the new CMS pixel detector readout chip PROC600

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The first layer of the CMS Phase I pixel detector will be placed at a distance of 3cm from the interaction point. At the instantaneous luminosity of $2 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ foreseen for the LHC operation in 2017-25, the pixel hit rate at this layer is expected to be as high as 600MHz/cm². A new readout chip, called PROC600, to be used for Layer 1 modules has been design at PSI. The pixel hit efficiency of the chip is above 99% at the rate of 600MH/cm². The properties and high rate capability of PROC600 will be discussed. The CMS Phase I pixel detector is expected to be in operation untill 2024/25. The total flux seen by the first layer will reach $2\text{-}3 \times 10^{15} \text{ neq/cm}^2$ which corresponds to 80-120MRad. To justify a robust and efficient operation of PROC600 it has been irradiated to a several doses up to 480MRad. The chip performance after irradiation including pixel hit efficiency will be presented.

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The Belle II Pixel Detector

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The DEPFET collaboration develops highly granular, ultra-transparent active pixel detectors for high-performance vertex reconstruction at the Belle II experiment, KEK, Japan. The key features of the DEPFET sensors have been proven: in-pixel amplification, high signal-to-noise ratio, non-destructive pulse height readout, integration of the readout ASICs on the All-Silicon module. The vertex pixel detector (PXD) will consists of two DEPFET layers at radii of 14 mm and 22 mm providing close to 8M pixels which will be read out within 20 μ s. A complete detector concept including mechanical support, cooling and services was developed and tested together with four layers of the silicon strip detector (SVD) during a beam test in spring 2016 at DESY. After a brief introduction to the Belle II experiment, the Pixel Detector PXD and the DEPFET sensor concept, this contribution will present measurements of PXD pilot modules including the functionality of an electronic shutter which allows to shield the sensor during beam injection. Finally an overview of the PXD production, QA tests and integration plan will be provided.

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Experience with the AFP 3D Silicon Pixel Tracker

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The ATLAS Forward Proton (AFP) experiment has recently installed two 3D Silicon pixel trackers in Roman Pots at one side of the ATLAS interaction point (IP) in order to measure forward protons. Each tracker consists of three to four 3D FE-I4 pixel modules. The detector will be completed with

two more 3D trackers at the other side of the IP plus time-of-flight detectors at both sides in the winter shutdown 2015/2016. AFP is the second HEP experiment that applies the 3D sensor technology, after the ATLAS IBL.

The technology was chosen as it was demonstrated in numerous qualification beam tests that it fulfills the AFP requirements of slim edges of less than 200 μm , radiation hardness in the case of non-uniform irradiation, and a tracker resolution of about 3 μm in the short pixel direction.

The 3D pixel sensors have been produced by CNM Barcelona in a double-sided process with non-passing-through columns, profiting from IBL experience. They have been bump-bonded to the FE-I4 readout chip, assembled, wire-bonded and undergone a Quality Assurance procedure at IFAE Barcelona. The module delivery, tracker assembly and installation in the LHC tunnel took place in February 2016, followed by commissioning and first data taking in Roman Pots inserted into the LHC beam during the LHC intensity ramp-up in April/May 2016.

This presentation will give an overview on the qualification, production and commissioning of the AFP 3D pixel trackers.

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AGIPD: A fast X-ray imager for the European XFEL

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The AGIPD (Adaptive Gain Integrating Pixel Detector) collaboration - consisting of Deutsches Elektronensynchrotron (DESY), University of Hamburg, University of Bonn and the Paul-Scherrer-Institute (PSI) - is currently developing a 2D hybrid pixel detector system capable to fulfill the requirements of the European XFEL (XFEL.EU).

At the XFEL.EU photons will arrive in bunch trains every 100 ns (or at a rate of 10 Hz). Each train consists of 2700 bunches that arrive within 600 μs (i.e. a bunch spacing of 220 ns, meaning 4.5 MHz frame rate) followed by 99.4 ns without pulses. Each single pulse consists of 10^{12} X-ray photons arriving in less than 100 fs with an energy tunable between 250 eV up to 25 keV.

In order to cope with the large dynamic range, the first stage of each pixel in the AGIPD ASIC is a charge sensitive preamplifier with three different gain settings that are dynamically switched during charge integration allowing to have both single photon resolution at 12.4 keV (with SNR>10) and to cover a dynamic range up to $10^4 \times 12.4$ keV photons. This gain switching is automatic and per pixel. The high frame rate (4.5 MHz) requires an on-pixel storage of every frame before the readout takes place during the gap between bunch trains.

The full scale chip (AGIPD1.0), received at the end of 2013, is a 64 x 64 pixel matrix. Each pixel (area 200 x 200 μm^2) is equipped with 352 storage cells. A long period of testing (almost 3 years) showed that even if the main performance parameters already match the requirements of the XFEL.EU a resubmission of the chip was necessary to fix all the design flaws spotted that make the actual chip not easy to calibrate and operate.

The new AGIPD1.1 design has been submitted in December 2015 and the chip was received in March 2016. Since then the ASIC is under test and a pre-characterization shows that many of the problems and limitations of the old chip are solved and the overall performance has strongly improved.

In this contribution the complete characterization activity on AGIPD1.0 will be shown with both experimental and simulation results. A detailed discussion about the choices made for the redesign of

the AGIPD1.0 chip will follow. At the end results of the characterization of the new chip AGIPD1.1 will be shown in comparison with AGIPD1.0.

Summary:

The AGIPD (Adaptive Gain Integrating Pixel Detector) collaboration - consisting of Deutsches Elektronensynchrotron (DESY), University of Hamburg, University of Bonn and the Paul-Scherrer-Institute (PSI) - is currently developing a 2D hybrid pixel detector system capable to fulfill the requirements of the European XFEL (XFEL.EU).

The XFEL.EU is a free electron laser that is being built at DESY (Hamburg, Germany). The first light is foreseen for early 2017. This machine shows many new and innovative features [1]. These features will open the way to new scientific opportunities in many fields of science and at the same time set many challenges in the detector design [2], in particular its extremely high frame rate.

At the XFEL.EU photons will arrive in bunch trains every 100 ns (or at a rate of 10MHz). Each train consists of 2700 photon pulses that arrive within 600 ns –which corresponds to a frame rate of 4.5MHz - followed by 99.4 ns without pulses. This extremely high frame rate sets a critical constraint on the design of the readout electronics. Since the readout of every single frame at 4.5 MHz is impossible, the signals must be stored on-pixel by means of an array of storage cells. The number of storage cells is a trade off between the number of frames that one wants to record per bunch train and the pixel area. The AGIPD detector [3][4] offers the possibility to store up to 352 images per bunch train by means of 352 analog storage cells per pixel.

Another important feature of the XFEL.EU is the extremely high peak brilliance of 5×10^{33} ph./s/mm²/mrad²/0.1% bandwidth. Such a brilliance means that each single pulse consists of 10^{12} X-ray photons squeezed in less than 100 fs with an energy tunable between 250 eV and 25 keV. From the point of view of the detector design this translates into three challenges. First, since a potential high number of photons will impinge on the detector pixels at the same time (<100fs) the single photon counting principle is not feasible. Second, a high dynamic range is required to be able to measure both a large photon signal and at the same time have single photon resolution in the areas of the detector where the intensity is low. The approach used by AGIPD to cope with these challenges is already included in its acronym. AGIPD is a charge integrating detector with multiple gain stages that are dynamically switched per pixel depending on the number of incoming photons, allowing to have both single photon resolution at 12.4 keV and to cover a dynamic range up to $10^4 \times 12.4$ keV photons.

The third challenge imposed by the brilliance regards the radiation tolerance. A total ionizing dose (TID) of 1 GGy is foreseen for 3 years of operation of the machine. At the target energy of 12.4 keV a fraction equal to 90% of the radiation is absorbed by the sensor therefore 100 MGy are expected on the readout electronics. This unprecedented level of irradiation forced to choose a radiation tolerant technology (IBM 130nm) and use a radiation tolerant design for the major part of the chip.

The design of such a complex chip is not trivial and the characterization and debugging phase to arrive to a final working system with the required performance can require several years. The first full scale chip (AGIPD1.0), received at the end of 2013, is a 64 x 64 pixel matrix and has been fully characterized and debugged for almost three years in order to assess its performance [5]. This long period of testing showed that even if the main performance parameters already match the requirements of the XFEL.EU a resubmission of the actual chip was necessary to fix all the design flaws spotted that makes the actual chip not easy to calibrate and to operate. One of the flaws regard the cross-talks between the analog voltages and the fast digital control signal lines that allow to access the different memory cells and that can be well described with an aggressor-victim model. The result of such a coupling is an evolution of different reference voltages in time that can limit the possibility to calibrate the detector. Moreover the resistive coupling between the last four parallel stages (offchip drivers) of the amplification chain cause the so called 'ghosting' effect. The ghosting effect consists in the appearance of three spurious images (ghosts) on the chip in the three homologous positions with respect to the real one. To finish, the power distribution is another critical point of the design of this ASIC. As it has been seen a voltage drop of few tens of mV across the chip can cause non negligible problems during the gain switching.

As already mentioned the actual chip performance, even if non-optimal, has proven to be suitable to successfully build the first 1Mega-pixel detector system matching the specification given by the XFEL.EU. The 1M system is now in construction and will be delivered to the XFEL.EU at the beginning of August 2016 and will be equipped with AGIPD1.0 chips and will be then upgraded with AGIPD1.1 chips in the future.

The new AGIPD1.1 design has been submitted in December 2015 and the chip was received in March 2016. Since then the ASIC is under test and a pre-characterization shows that many of the problems and limitations of the old chip are solved and the overall performance has strongly improved.

The results of the careful testing activity - that will be shown in this contribution - together with the simulations of such a complex chip are useful to arrive to a final version of the ASIC and are a very valuable experience for the future development of such kind of detectors.

[1] European XFEL: <http://www.xfel.eu/en/index.php>

[2] H. Graafsma, Requirements for and development of 2 dimensional X-ray detectors for the European X-ray Free Electron Laser in Hamburg, JINST 4 P12001, DOI: 10.1088/1748-0221/4/12/P12011 (2009).

[3] X. Shi et al, "Challenges in chip design for the AGIPD detector", Nucl. Instr. Meth. A 624, p.387 - 391 (2010).

[4] D. Greiffenberg et al., Towards AGIPD1.0: optimization of the dynamic range and investigation of a pixel input protection, 2014 JINST 9 P06001.

[5] D. Mezza et al., Characterization of AGIPD1.0: the full scale chip, Submitted to Nuclear Instruments and Methods A

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Testbeam results of n+-in-p planar pixel sensor of quad ASIC pixels and high momentum resolution pixel detectors

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An n+-in-p planar pixel semiconductor tracking detector is being developed with HPK for the ATLAS detector upgrade of high luminosity LHC (HL-LHC). The novel design of single-FE-I4 size (20.9 x 18.5 mm squared) planar pixel sensor with 250x50 micro-meter squared has been developed and tested using FE-I4 read out ASIC. The module with four-FE-I4 on single pixel sensor (41.2 x 35.7 mm squared) are produced and tested to emulate actual installation of ATLAS detector. For the pixels located inter pixel region need "ganging" structure which is Aluminum rail connecting inter ASIC pixels to the normal pixels to readout signals via normal pixel. The effect to the efficiency by the ganging structures are tested with and without irradiation corresponding fluence of HL-LHC operation. Irradiation are preformed at CYRIC Tohoku University, with 70MeV protons. As high momentum resolution pixel detector, 500x25 micro-meter squared size pixel detectors are developed to have twice better resolution for bending direction of charged particle in solenoid magnet. In this talk performance study using testbeam results for quad ASIC pixel detector and high momentum resolution detector are presented.

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Readout electronics for LGAD sensors

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Low Gain Avalanche Detectors (LGAD) represent a remarkable advance in high energy particle detection, since they provide a moderate increase (gain ~ 10) of the collected charge, thus leading to a notable improvement of the signal-to-noise ratio, which largely extends the possible application of Silicon detectors beyond their present working field. The optimum detection performance requires a careful implementation of the multiplication junction, in order to obtain the desired gain on the read out signal, but also a proper design of the edge termination and the peripheral region, which prevents the LGAD detectors from premature breakdown and large leakage current.

The Low Gain Avalanche Detector (LGAD) is based on the standard Avalanche Photo Diodes (APD) concept, commonly used in optical and X-ray detection applications, including an internal multiplication of the charge generated by radiation. The multiplication is inherent to the basic n⁺⁺-p⁺-p structure, where the doping profile of the p⁺ layer is optimized to achieve high field and high impact ionization at the junction.

All avalanche diode detectors have a region with a high electrical field leading to multiplication of signal charges (electron and/or holes) flowing through this region. The gain mechanism is achieved within the semiconductor material by raising the electric field as high as necessary to enable the drifting electrons to create secondary ionization during the collection process. Normally, the junction consists of a thin and highly doped n-type layer on top of a moderately doped p-layer in which the multiplication (of electrons) takes place. A high resistivity p-type silicon substrate is typically used to produce detectors with a bulk that can be fully depleted.

Compared to standard APD detectors, LGAD (Low Gain Avalanche Detectors) structure exhibit moderate gain values. This is mandatory to obtain fine segmentation pitches in the fabrication of microstrip and pixel detectors, free from the limitations commonly found in avalanche detectors. In addition, a moderate multiplication allows the fabrication of thinner sensors, with an output signal amplitude that is as large as that from thicker sensors without internal gain. The design of LGAD structure exploits the charge multiplication effect to obtain a silicon detector that can simultaneously measure precisely the position and time of arrival of incident particles.

The LGAD structures are optimized for applications such as tracking or timing detectors for high energy physics experiments or medical applications where time resolution lower than 30 ps is required.

In this paper, an ASIC fabricated in 180 nm CMOS technology from AMS with the very front-end electronics used to readout LGAD sensors is presented as well as its experimental results. The front-end has the typical architecture for Si-strip readout, i.e., preamplification stage with a Charge Sensitive Amplifier (CSA) followed by a CR-RC shaper. Both amplifiers are based on a folded cascade structure with a PMOS input transistor and the shaper only uses passive elements for the feedback stage and the shaping time is fixed at 1 μ s. The CSA has programmable gain and a configurable input stage in order to adapt to the LGAD sensors. The fabricated prototype is 0.865 mm x 0.965 mm and includes the biasing circuit for the CSA and the shaper, 4 analog channels (CSA+shaper) and programmable charge injection circuits included for testing purposes. The power consumption is 150 μ W per channel.

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Radiation damage caused by neutron capture in boron doped silicon pixel sensors

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CMOS Monolithic Active Pixel Sensors (MAPS) for charged particle tracking provide a unique combination of excellent spatial resolution ($\sim 5 \mu$ m), light material budget (0.05% X₀) and an advanced

tolerance to radiation. This makes them the technology of choice for the vertex detectors of various experiments in heavy ion and particle physics including NA61 and CBM.

In this application, the P-doped MAPS are exposed to various kinds of radiation, among them thermal neutrons. Those neutrons create negligible bulk damage according to the NIEL-model. However, this model ignores that thermal neutrons may initiate a nuclear fission of the boron dopants ($B_{10} + n \rightarrow Li + \alpha + 3MeV$) found in P-doped silicon. It was questioned, whether the fast fission products originating from this reaction might damage the sensors.

We estimated the magnitude of the additional damage based on theoretical arguments. Moreover, we irradiated MIMOSA-19 sensors, which were obtained from the IPHC Strasbourg, with cold neutrons at the PGAA beam line of the FRM-II nuclear reactor. We introduce the results of our theoretical studies and compare the non-trivial radiation damage effects to be expected with our experimental findings. We motivate that the NIEL model may underestimate the damage caused by thermal neutrons in MAPS by one to two orders of magnitude under unfavorable conditions.

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From LHC to HL-LHC ... challenges and routes to solutions

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The pixel detectors currently in operation established the hybrid pixel technology that is now mainstream. From this new vantage point, several concepts that were previously too controversial are now being explored for the HL-LHC generation of detectors. At the same time, some problems that were considered solved have shown surprises, while in other cases the correct path appears to be the opposite of the previously assumed solution. This talk will review the challenges of HL-LHC and the development carried out to address them, highlighting the above aspects. The challenges around the HL-LHC ring include high rate and radiation for both sensors and electronics, large area and low cost, high track density and pileup, higher resolution and lower mass, higher readout rate. In most cases specific developments to address these challenges will be further covered in other talks in this conference (3D, planar, and high speed sensors, MAPS, mechanics and cooling, RD53 and radiation tolerance, high speed readout, etc.) so the intent here is to present an overview and introduction.

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Pixel Detector Prototype based on IGZO TFT preamplifier and Analog counter

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IGZO (indium gallium zinc oxide) semiconductor TFT (thin film transistor) is commonly used for large area flat-panel display as switching and this technology also has an advantage for making a large area detector. A prototype of 8 x 8 pixel detector based on IGZO charge sensitive preamplifier (CSA) and analog counter was designed and fabricated for future photon counting radiation system,

such as CT. The size of pixel in fabricated array is 1.5 mm x 1.5 mm and whole size is 12mm x 12 mm. The size of CSA and analog counter is within 300 μ m x 300 μ m. The fabricated CSA shows the ENC of approximately 1050 electrons rms at the shaping time of 3 μ s with 1.3 mW and analog counter is operated with up to 1 Mcps in the first prototype. The energy spectrum was acquired using test pulse of MPPC/SiPM sensors since the decoupling capacitor (10fF) is implemented in pixel. The performance coupled with CdTe detector will be also presented in the conference.

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ALPIDE: the Monolithic Active Pixel Sensor for the ALICE ITS upgrade

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The upgrade of the ALICE vertex detector, the Inner Tracking System (ITS), is scheduled to be installed during the next long shutdown period (2019-2020) of the CERN Large Hadron Collider (LHC). The current ITS will be replaced by seven concentric layers of Monolithic Active Pixel Sensors (MAPS) with total active surface of ~ 10 m², thus making ALICE the first LHC experiment implementing MAPS detector technology on a large scale.

The ALPIDE chip, based on TowerJazz 180 nm CMOS Imaging Process, is being developed for this purpose. A particular process feature, the deep p-well, is exploited so the full CMOS logic can be implemented over the active sensor area without impinging on the deposited charge collection. ALPIDE is implemented on silicon wafers with a high resistivity epitaxial layer. A single chip measures 15 mm by 30 mm and contains half a million pixels distributed in 512 rows and 1024 columns. In-pixel circuitry features amplification, shaping, discrimination and multi-event buffering. The readout is hit driven i.e. only addresses of hit pixels are sent to the periphery.

The upgrade of the ITS presents two different sets of requirements for sensors of the inner and of the outer layers due to the significantly different track density, radiation level and active detector surface. The ALPIDE chip fulfils the stringent requirements in both cases. The detection efficiency is higher than 99%, fake hit probability is orders of magnitude lower than the required 10^{-5} and spatial resolution within required 5 μ m. This performance is maintained even after an irradiation up to several Mrad and few 10^{13} 1 Mev n_{eq}/cm², which is above what is expected during the detector lifetime. Readout rate of 100 kHz is provided and the power density of ALPIDE is less than 40 mW/cm².

This contribution will provide a summary of the ALPIDE features and main test results.

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Simulation of polarization effect and charge collection in pixelated CdTe sensors

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Recent progress in the fabrication of fine-pitch CdTe sensors and the development of bonding technology makes this material a good candidate for hybrid pixel detector systems, in particular for imaging experiments at synchrotrons (or free-electron lasers) with X-ray energy up to a few hundred keV. The main drawbacks of CdTe sensors in terms of their electrical performance are the high leakage current for pixel electrodes fabricated by ohmic contact, and the time dependence of charge collection caused by biasing and flux for electrodes fabricated by Schottky contact. The latter is also known as the polarization effect. To properly simulate and understand both effects, and to optimize the sensor layout in the future, the knowledge and implementation of traps into simulation is essential. In this work, the Cd vacancies (V_{cd}), V_{cd}-donor complexes, deep traps as well as residual impurities have been considered. The concentration of deep traps is calibrated by comparing the material resistivity of simulation and measurement on a Cl-doped CdTe pad sensor produced by Acrorad. Based on this result, the polarization effect has been simulated and explained. In addition, the charge collected by edge pixels and their non-uniformity compared to central pixels, which is caused by the change in resistivity at the edge of the sensor, has been studied and compared to measurements. Finally, the validation and limit of the trap model and its influence on sensor-layout optimization are discussed.

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The prototype of 6-bit SAR ADC for SOI pixel detector readout

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Silicon-On-Insulator (SOI) technology uses an insulator layer in a standard silicon substrate CMOS structure. The reduction of parasitic capacitances to substrate increases the speed of a circuits and decreases their power consumption. Moreover, there is a possibility to design monolithic detectors with sensor matrix and electronic integrated on a single wafer. These features make the SOI technology a good candidate for particles detector readout systems. In this work the design and preliminary measurements of 6-bit SAR ADC is presented. The ADC was designed in 200 nm Lapis SOI and is dedicated for column readout of SOI pixel detectors developed in this technology. The first measurements show that correct operation and the ADC achieves ENOB of about 5 bits at 7-MHz of sampling frequency. The measured power consumption is about 300 μW.

Summary:

The SOI technology is a promising candidate for future high energy physic detector systems because of the possibility for monolithic pixel detector design. Moreover, the Burried-Oxide (BOX) layer in the SOI structure helps to reduce the power consumption of the electronic circuits and increase their speed. The additional advantages is latch-up effects elimination and significant reduction of Single Event Upsets (SEU). The proposed Analog-to-Digital Converter (ADC) is a sub-part of a complex pixel detector matrix with dedicated readout electronics, being developed by the authors of this work in 200nm Lapis Fully-Depleted, Low-Leakage SOI technology.

The Successive Approximation Register (SAR) architecture provides a good conversion speed in

In order to test the behavior of different transistors available in 200nm Lapis SOI, three di

First measurements show that all prototypes are fully functional and there is no meaningful d
The presented ADC has been implemented as column ADC and fabricated in a prototype monolithic

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Operational Experience with the ATLAS Pixel detector

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Run-2 of the LHC is providing new challenges to track and vertex reconstruction with higher energies, denser jets and higher rates. Therefore the ATLAS experiment has constructed the first 4-layer Pixel detector in HEP, installing a new Pixel layer, also called Insertable B-Layer (IBL). In addition the Pixel detector was refurbished with a new service quarter panel to recover about 3% of defective modules lost during run-1 and a new optical readout system to readout the data at higher speed while reducing the occupancy when running with increased luminosity.

The commissioning and performance of the 4-layer Pixel Detector will be presented.

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Ultra-low material pixel layers for the Mu3e experiment

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The upcoming Mu3e experiment will search for the charged lepton flavour violating decay of a muon at rest into three electrons. The maximal energy of the tracks will be 53 MeV, hence low material budget is a key performance requirement. We will show our approach to meet the requirement of about 1 % of radiation length per detector layer. This includes the choice of thinned active monolithic pixel sensors in HV-CMOS technology, ultra-thin flexible high density interconnects, and Helium gas cooling.

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Performance of the EUDET-type beam telescopes

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Beam telescopes are vital tools for R&D projects focussing on position sensitive particle detection sensors. These range from collider-specific detectors with high radiation tolerance [1-2], high resolution and low material requirements [3] to medical applications [4], among others. Test beam studies are used at various stages of sensor and read-out chip development and are considered as the “gold standard” of sensor and detector testing. Besides the LHC experiments, many others like Mu3e, Belle-II, BEAST, etc. use a EUDET-type beam telescope to characterise their sensors, covering examples from specific upgrade scenarios to generic sensor R&D.

Summary:

Test beam measurements at the test beam facilities of DESY have been conducted to characterise the performance of the EUDET-type beam telescopes originally developed within the EUDET project. The beam telescopes are equipped with six sensor planes using MIMOSA26 monolithic active pixel devices. A programmable Trigger Logic Unit provides trigger logic and time stamp information on particle passage. Both data acquisition framework and offline reconstruction software packages are available. User devices are easily integrable into the data acquisition framework via predefined interfaces.

In this talk, the biased residual distribution is studied as a function of the beam energy, plane spacing and sensor threshold.

Iterative track fits using the formalism of General Broken Lines are performed to estimate the intrinsic resolution of the individual pixel planes. The mean intrinsic resolution over the six sensors used is found to be (3.24 ± 0.09)

upmu

meter. With a 5 GeV electron/positron beam, the track resolution halfway between the two inner pixel planes using an equidistant plane spacing of 20 mm is calculated to be (1.83 ± 0.03)

upmu

meter. Towards lower beam energies the track resolution deteriorates due to increasing multiple scattering.

Sensor threshold studies show an optimal working point of the MIMOSA26 sensors at a sensor threshold of between five and six times their RMS noise.

Measurements at different plane spacings are used to calibrate the amount of multiple scattering in the material traversed and allow for corrections to the predicted angular scattering for electron beams.

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Pulse height analysis techniques for radiation detectors

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Most radiation detectors require pulse (or signal) processing electronics so that energy or time information involved with radiation interactions can be properly extracted. The objective of this work is to develop and compare various pulse processing techniques for x-ray and Gamma ray spectrometers which can be used for future scientific missions.

A preamplifier is the first component in a signal processing chain of a radiation detector which has a main function to extract the signal from the detector without significantly degrading the intrinsic signal-to-noise ratio. Preamplifier does not act as an amplifier but it collects charge created within a detector. Charge sensitive pre-amplifier (CSPA) output is a pulse, carrying the information of interacted photon energy. CSPA output signal is given to pulse height analyzer for energy spectroscopy. The pulse height analyzer performs several essential functions. Its primary role is to magnify the amplitude of the preamplifier output pulse from the mV range into the 0.1 ~ 5 V range which is proportional to incident photon energy.

To make a comparative study we are developing various pulse height analysis techniques like, pulse height analysis using constant pulse discharge, Pulse width modulation technique, Digital pulse pro-

cessing technique and pulse height measurement using peak detector & successive approximation ADC. This comparative study will help to identify the proper processing technique for various radiation detection instruments. By this study, proper pulse processing method can be selected based on instrument specifications like number of detectors, total incoming photon count rate, spectral resolution, size, mass and power.

Above said pulse processing methods were implemented on hardware and tested with x-ray detector (silicon drift detector-SDD). Performance of processing techniques is compared based on achieved spectral resolution, count rate handling, power consumption and total component requirement. Each technique has its own advantage and disadvantages will be presented in the symposium.

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The VeloPix ASIC for the LHCb VELO Upgrade

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The LHCb upgrade, scheduled for LHC Run-3, will transform the experiment to a trigger-less system reading out the full detector at 40 MHz event rate. The Vertex Locator (VELO) will be a hybrid pixel system, featuring silicon pixel sensors with $55 \times 55 \mu\text{m}$ pitch, read out by the VeloPix ASIC. The sensors and ASICs will approach the interaction point to within 5.1 mm and be exposed to a radiation dose of up to 370 MRad or $8 \times 10^{15} \text{ 1 MeV n}_{\text{eq}} \text{ cm}^{-2}$. *The hottest ASIC must sustain pixel hit rates of more than 900 Mhits/s*

This paper will present the VeloPix ASIC which has been developed for the readout of the upgraded VELO. This ASIC derives from the Medipix/Timepix family and has many features in common with the Timepix3, however the VeloPix is further optimised for speed and radiation hardness. Each ASIC reads out an array of 256×256 pixels with $55 \times 55 \mu\text{m}$ pitch. *The ASIC are flipchipped in groups of three per ASIC. The ASIC is designed in a 130 nm CMOS technology.*

The ASIC readout is data driven and zero suppressed, and the implementation of the super pixel concept (4x2 pixel grouping) further optimises the bandwidth and available space. The timewalk is minimised (at 1000 e⁻ threshold) to reduce the number of out-of-time hits in the 25 ns LHC data taking conditions. Because of the severe radiation environment the ASIC is equipped with SEU protection and is designed to cope with sensor leakage currents. In order to meet the huge data output rate requirement while keeping the power consumption within the budget a dedicated 5.12 Gbit/s output serialiser, the GWT (Gigabit Wireline Transmitter), has been developed. The ASIC has been submitted in May and we expect to show the very first performance results.

Summary:

The LHCb upgrade, scheduled for LHC Run-3, will enable the experiment to be read out at 40 MHz in triggerless mode, with full event selection being performed offline. The Vertex Locator (VELO) will be upgraded to a pixel device with a new dedicated ASIC, the VeloPix, a 130 nm technology chip with data driven and zero suppressed readout. The sensors are positioned with an innermost radius at just 5.1 mm from the LHC beams and the hottest ASICs will experience rates of more than 900 Mhits/s. The recently submitted ASIC will be presented along with the first test results.

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LHCb VELO Upgrade

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The VERTex LOcator (VELO) is the silicon detector surrounding the interaction region of the LHCb experiment. From 2019, LHCb aims to run at a luminosity of $2 \times 10^{33} \text{ cm}^{-2} \text{ s}^{-1}$, 5 times greater than the current luminosity, and to enhance trigger efficiency. Upgrades are required to many of the LHCb sub-detectors and the experiment will transform to a system reading out the full detector at 40-MHz event rate, operating event selection in a dedicated computer form.

The VELO consists of two halves situated in a secondary vacuum inside the LHC beam pipe, separated by a thin custom-made RF foil. The two halves can be retracted when beams are injected and closed during stable beams, positioning the first sensitive pixel 5.1-mm from the beams.

Each half of the VELO will consist of 26 L shaped modules. The module is a double sided construction, with two hybrid pixel assemblies and their PCB circuits mounted on either side of the central backbone; a 400- μm thick silicon plate incorporating cooling microchannels for the circulation of evaporative CO_2 . Operation is at a sufficiently low temperature to avoid thermal runaway of the irradiated sensors.

The VELO's proximity to the beam means that it is exposed to a harsh radiation environment, resulting in non uniform radiation damage across the sensors. The hybrid pixel system will be equipped with data driven electronics and designed to withstand a radiation dose of up to $8 \times 10^{15} \text{ 1 MeV n}_{eq} \text{ cm}^{-2}$. The silicon pixel sensors have a pitch of $55 \times 55 \mu\text{m}^2$, read out by the VeloPix ASIC which is being developed based on the TimePix/MediPix family. The performances of prototype sensors from two manufactures have been tested at testbeam before and after exposure to both uniform and non uniform irradiation. A dedicated telescope system based on the TimePix3 assemblies was created for testbeam studies at the SPS, CERN. This allows several different tests of the prototype sensors, for example, detailed analysis of the resolution, efficiency, charge sharing and radiation effects.

An overview of the LHCb VELO upgrades and the current status will be described together with a presentation of some of the analysis from testbeam using the TimePix3 telescope.

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Pixel hybridization technologies for the HL-LHC

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During the 2024-2025 shutdown, the Large Hadron Collider (LHC) will be upgraded to reach an instantaneous luminosity up to $7 \times 10 \text{ cm}^{-2} \text{ s}^{-1}$. This upgrade of the accelerator is called High-Luminosity LHC (HL-LHC). The ATLAS and CMS detectors will be upgraded to meet the new challenges of HL-LHC: an average of 200 pile-up events in every bunch crossing and an integrated luminosity of 3000 fb^{-1} over ten years. In particular, the current trackers will be completely replaced to meet the requirements coming with the high instantaneous and integrated luminosities.

The pixel detectors, the innermost part of the trackers, need significantly rethinking in all their basic elements to the performance and/or to reduce the overall cost of the trackers. A new 65 nm front-end electronics is being developed by the RD53 collaboration. The new front-end chip will be compatible with $50 \times 50 \mu\text{m}^2$ or $25 \times 100 \mu\text{m}^2$ pixel size sensors. An intensive program of R&D has been promoted to study new sensor technologies. The smaller pixel sizes imply up to five times the number of bumps used in the current ATLAS Insertable B-Layer modules and consequently an order of 120 thousands pixels per chip.

In this talk, a review of the hybridization technologies will be presented. In particular, the on-going qualification program at Selex will be discussed. Selex has been one of the two vendors for the current ATLAS pixel detector and as required by the HL-LHC projects, it is now upgrading its capability to meet larger wafer size at higher bump density. The qualification of some flip-chip sites will be also presented as a possible help in the organization and production workflow. Finally, alternative hybridization techniques, as the capacitive coupling for HVCMOS detectors, will also be discussed.

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Physics performance of the ATLAS Pixel Detector

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The ATLAS Pixel Detector is the innermost detector of the ATLAS experiment at the Large Hadron Collider at CERN, providing high-resolution measurements of charged particle tracks in the high radiation environment close to the collision region. It is the unique 4-pixel detector layers in HEP. The operation and performance of the Pixel Detector at LHC running are described. More than 97% of the detector modules were operational during this period, with an average intrinsic hit efficiency larger than 99%. The evolution of the noise occupancy is discussed, and measurements of the Lorentz angle, delta-ray production and energy loss presented.

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Development of CdTe Pixel Detectors Combined with an Aluminum Schottky Diode Sensor and Photon-Counting ASICs

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We have been developing CdTe pixel detectors combined with a Schottky diode sensor and photon-counting ASICs. On the CdTe sensor device the front side was deposited with aluminum to form pixelated electrodes and the back side was covered with a single platinum-electrode. This electrode configuration has the advantage of providing a high Schottky barrier formed on the Al/CdTe interface, and, hence, a benefit to operate the CdTe as an electron-collecting pixelated diode. The 2D-detector module was designed with a pixel pitch of 0.2 mm x 0.2 mm and an area of 19 mm x 20 mm or 38.2 mm x 40.2 mm. The SP8-04F10K ASIC has a preamplifier, a shaper, 3-level window-type discriminators and a 24-bits counter in each pixel. The single-chip detector with 100 x 95 pixels successfully operated with a photon-counting mode selecting X-ray energy with the window comparator. We have performed a feasibility study for white X-ray microbeam experiment. Laue diffraction patterns were measured during the scan of the irradiated position in a silicon steel sample. The grain boundaries were identified by using the differentials between adjacent images at each position. In this talk, we will present the specification and performance of CdTe pixel detectors with the SP8-04-F10K ASICs.

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Operational Experience with the ALICE Pixel Detector

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The Silicon Pixel Detector (SPD) constitutes the two innermost layers of the Inner Tracking System of the ALICE experiment. It is the closest detector to the interaction point and a special effort was done to narrow its material budget down to 1% X₀ per layer. As a vertex detector, it has the unique feature of generating a trigger signal that contributes to the L0 trigger of the ALICE experiment. The SPD started to record data since the very first pp collisions at LHC in 2009 and it was operational in Pb-Pb collisions as well as in p-Pb collisions in 2013. It is still fully operational in the ongoing LHC run period, Run 2, after a long shutdown period of two years. This contribution will present the main features of the SPD, the detector performance and the operational experience, including calibration and optimization activities from Run 1 to Run 2.

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NOVEL TIME-DEPENDENT ALIGNMENT OF THE ATLAS INNER DETECTOR IN THE LHC RUN II

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ATLAS is a multipurpose experiment at the LHC proton-proton collider. Its physics goals require high resolution, unbiased measurement of all charged particle kinematic parameters. These critically depend on the layout and performance of the tracking system and the quality of its offline alignment. For the LHC Run II, the system has been upgraded with the installation of a new pixel layer, the Insertable B-layer (IBL). ATLAS Inner Detector Alignment framework has been adapted and upgraded to correct very short time scale movements of the sub-detectors. An outline of the track based alignment approach and its implementation within the ATLAS software will be introduced. Special attention will be paid to describe the techniques allowing to pinpoint and eliminate track parameters biases due to alignment. In particular, a mechanical distortion of the IBL staves up to 20um has been observed during data-taking. The techniques used to correct for this effect and to match the required Inner Detector performance will be presented.

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Thin hybrid pixel assembly with backside compensation layer on ROIC

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ATLAS will replace the entire tracking system for operation at the HL-LHC. This will include a significantly larger pixel detector of approximately 10 m². It is critical to reduce the mass of the pixel modules and this requires thinning both the sensor and readout to about 150 micrometers each. The bump yield in thin module assembly using solder based bump bonding can be problematic due to wafer bowing during processing at high temperatures. A new bump-bonding process using backside compensation on the readout chip to address the issue of low yield will be presented. Results from characterization of assemblies produced from readout wafers thinned to 100 micrometers and the effect of applying backside compensation will be presented. Hybrid modules with bond yields close to 100% have been measured using 100 um thick FEI4 readout chip.

Summary:

The ATLAS FE-I4 readout IC, ROIC, is almost 20 mm x 20 mm in size with order 10 micrometers of metal and dielectrics above the CMOS implants. When the die is thinned to a few hundred micrometers it bows due to the stress in the dielectric/metal layers no longer being resisted by a thick silicon substrate. This bowing is increased further at elevated temperatures due to the different coefficient of thermal expansions of the dielectric/metal layers and silicon substrate. Solder based bump-bonding typically takes place at 260C and will increase the bow of the die significantly to several hundred micrometers. The size of the solder bumps are only 25 micrometers in diameter. Therefore, bowing of the ROIC will cause issues with the yield of the solder connections as they will not make electrical connection with the sensor and ROIC. The work will show that the bow of the die can be affected with the use of a post-processed dielectric layer and metal layer deposited on the backside of the wafer. The bow of the FE-I4 dies as a function of die temperature for different backside dielectric deposition is shown. The details of the fabrication process and the characterization techniques are described, as well as the final result. The processing technologies have been chosen to be compatible with both the existing CMOS ROIC but also with the through-silicon-via, TSV, technology of the foundry. The near 100% bond yield of assemblies made from 100 micrometer thick ROICs and 150 micrometers sensors are shown. The assemblies have been shown to be robust to thermally cycling from 60C to -40C 100 times and to thermal shock (defined as a sudden change from room temperature to -40C).

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Application of a Transient-Current-Technique based on a Two-Photon-Absorption process to the characterization of a HV-CMOS deep n-well

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Transient Current Techniques (TCT) based on laser-induced photo-currents produced by Single Photon Absorption (SPA) processes have been extensively used during the last two decades as a powerful tool to study many of the properties relevant to operation of semiconductor detectors such as the electric field distribution, carriers mobility, CCE, VDep, trapping lifetimes and the space-charge sign and geometry of complex segmented semiconductor junctions; moreover, the TCT techniques have been proven an excellent method for the understanding of the radiation-induced alterations of the semiconductor material and junction structure [1]

Very recently, an innovative Transient Current Technique was introduced where the free charge carriers are created in a Two-Photon-Absorption (TPA) process induced by a focused femto-second laser pulse with a wavelength of 1300nm[2][3]. The fact that in a TPA process the absorption of the light depends on the square of the intensity of the light beam used for the current generation allows a localized TPA-induced electron-hole pair creation in a micrometric scale voxel centered on the laser waist. As a consequence, this new technique opens the possibility to carry out a 3D mapping of the sensor's space-charge properties with micrometric resolution.

Due to its intrinsic spatial resolution, the TPA-TCT technique is a very appropriate choice for the characterization of the alterations of the sensor's active volume induced by the ionizing radiation; in especial manner, for the case of partially depleted sensors as it is the case of the carrier collecting n-well implemented in HV-CMOS sensors. Using the TPA-TCT technique on a HV-CMOS device the deep n-well has been accurately measured being able to determine its effective doping concentration for the first time in this kind of depleted CMOS devices[4] achieving a unprecedented

insight on the doping level and dimensions of the deep n-well suitable for a better understanding and optimization of the device design.

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IDSAC - IUCAA Digital Sampler Array Controller

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IUCAA Digital Sampling Array Controller (IDSAC) is a generic CCD Controller which is flexible and powerful enough to control a wide variety of CCDs and CMOS detectors used for ground based astronomy. It has a fully scalable architecture, which can control multiple CCDs and can be easily expanded. The controller has a modular backplane architecture consists of Single Board Controller Cards (SBCs) and can control a mosaic or independent of 5 CCDs. Each Single Board Controller (SBC) has all the resources to a run Single large format CCD having up to four outputs. All SBCs are identical and are easily interchangeable without any reconfiguration. A four channel video processor can process up to four output CCDs with or without dummy output at 1Mpixels/Sec/Channel with 16 bit resolution. Each SBC will have USB 2.0 interface which will be connected to a separate computer via USB to Fiber converters. The SBC uses a reconfigurable hardware (FPGA) as a Master Controller. The best feature of IDSAC is it uses the technique of Digital Correlated Double Sampling(DCDS). It is known that CCD video output is dominated by thermal KTC noise contributed from the summing well capacitor of the CCD output circuitry. To eliminate thermal KTC noise Correlated Double Sampling (CDS) is a very standard technique. CDS performed in Digital domain (DCDS) has several advantages over its analog counterpart, such as - less electronics, faster readout and easier post processing. It is also flexible with sampling rate and pixel throughput while maintaining the core circuit topology intact. The noise characterization of the IDSAC CDS signal chain has been performed by analytical modelling, software simulation and practical measurements. Various types of noise such as white, pink, power supply, bias etc. has been considered while creating a analytical noise model tool to predict noise of a controller system like IDSAC. Standard test bench softwares like Pspice and Multisim are used to simulate the noise performance while several tests are performed to measure the actual noise of IDSAC.The theoretical calculation

matches

very well with component level simulation as well as practical measurements within 10% accuracy.