INFN Mezzanine

Report of Contributions

https://agenda.infn.it/e/10173

Contribution ID: **0** Type: **not specified**

Goal of the meeting, the next months

Tuesday, 22 September 2015 15:30 (30 minutes)

Presenter: PALLA, Fabrizio (PI)

Contribution ID: **1** Type: **not specified**

Geometry, pattern banks and data formats

Tuesday, 22 September 2015 16:00 (45 minutes)

Presenter: Dr VIRET, Sebastien (CNRS/IN2P3)

Contribution ID: **2** Type: **not specified**

Status of the PCA (in C++) and its floating point implementation

Tuesday, 22 September 2015 16:45 (30 minutes)

Presenter: STORCHI, Loriano (P)

Contribution ID: **3** Type: **not specified**

Thermal analysis of the mezzanine

Tuesday, 22 September 2015 17:15 (30 minutes)

Contribution ID: **4** Type: **not specified**

Lookup table and constants

Wednesday, 23 September 2015 09:00 (30 minutes)

Contribution ID: **5** Type: **not specified**

Filtering/reducing combinations FW

Wednesday, 23 September 2015 09:30 (30 minutes)

Contribution ID: **6** Type: **not specified**

Status of DO and TF firmware

Wednesday, 23 September 2015 10:50 (30 minutes)

Presenter: GENTSOS, Christos (Auth)

Contribution ID: **7** Type: **not specified**

Status of AM06 chip and changes wrt AM05

Wednesday, 23 September 2015 11:20 (30 minutes)

Presenter: ANNOVI, Alberto (PI)

Contribution ID: **8** Type: **not specified**

Aurora link firmware status

Wednesday, 23 September 2015 11:50 (30 minutes)

Presenter: MAGAZZU', Guido (PI)

Contribution ID: **9** Type: **not specified**

Filtering/reducing combinations 2

Wednesday, 23 September 2015 10:00 (20 minutes)

Presenter: CASARSA, Massimo (TS)

Contribution ID: **10** Type: **not specified**

Status of the AM05 mezzanine tests - what have we learned?

Wednesday, 23 September 2015 14:00 (1 hour)

Presenters: MAGALOTTI, DANIEL (PG); FEDI, Giacomo (PI); MAGAZZU', Guido (PI)

Contribution ID: **11** Type: **not specified**

Proposed changes for the AM06 mezzanine

Wednesday, 23 September 2015 15:00 (1 hour)

Contribution ID: **12** Type: **not specified**

Discussion on mezzanine qualification procedures

Thursday, 24 September 2015 09:00 (1 hour)

Presenter: CHECCUCCI, Bruno (PG)

Contribution ID: **13** Type: **not specified**

Discussion on firmware integration policy

Thursday, 24 September 2015 10:00 (30 minutes)

Contribution ID: **14** Type: **not specified**

Signup for the AM06 mezzanine work and item distribution

Thursday, 24 September 2015 11:00 (1 hour)

Test 4 AM blocks cross talk and operations with 4 AM blocks (including sync)

Check the power budget of the mezzanine (measurements and availability from the Pulsar 2b, including external power)

Check the clock jitter. Clock should be changed anyway to match Xilinx specs.

Check external memory needs. Measure the time of access. Decide which type.

Evaluate resources needs for the FPGA including all FW.

Evaluate the time to modify the PCB for 8 AM chips

Evaluate the time to modify the PCB to accommodate the needed changes

NB: the last 2 items depend on how many engineers will be working. So Time and FTE estimates.

Contribution ID: **15** Type: **not specified**

Plan for the next months

Thursday, 24 September 2015 12:00 (30 minutes)