Status of DO and TF firmware

for the INFN mezzanine meeting

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Outline

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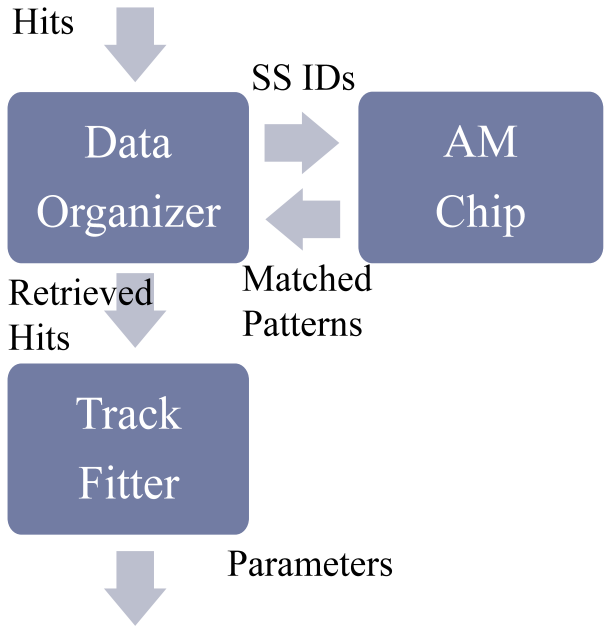
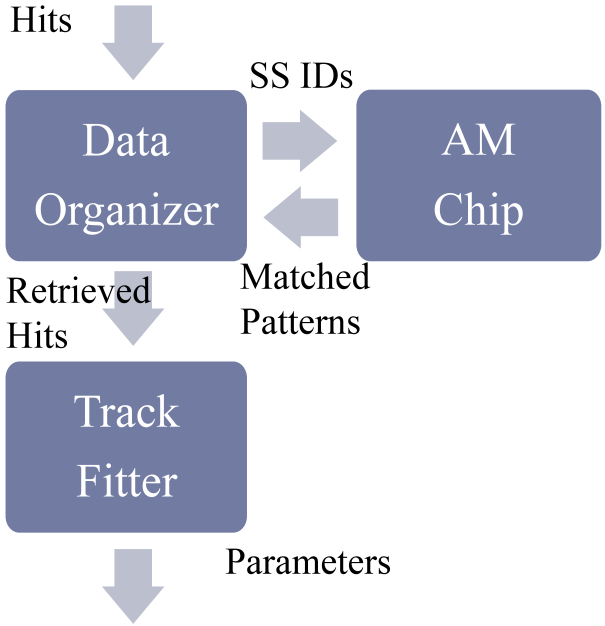
Data Organizer functionality

- DO stores full resolution hits according to their 16-bit stub ID
- It forwards the stub ID to the AMChips for pattern recognition
- It retrieves the full resolution hits according to the results from the AMChips
- All possible combinations that form tracks are found and forwarded to the TF



Track Fitter functionality

- Track Fitter performs linear fits at a high speed
- For each candidate track, calculates parameters and χ^2 (fit quality)
- Very fast operation ($500MHz+$)
- A whole fit is done in parallel, each clock cycle



DO modifications

- DO has two modes of operation
  - Write mode, where the hits are written in the internal memory structures
  - Read more, where the hits are read
- It can operate at one mode at a time
  - That means that a DO instance can't accept data all the time
- The need arises to have two DO instances at the same time
  - When one is taking data in, the other is pushing data out

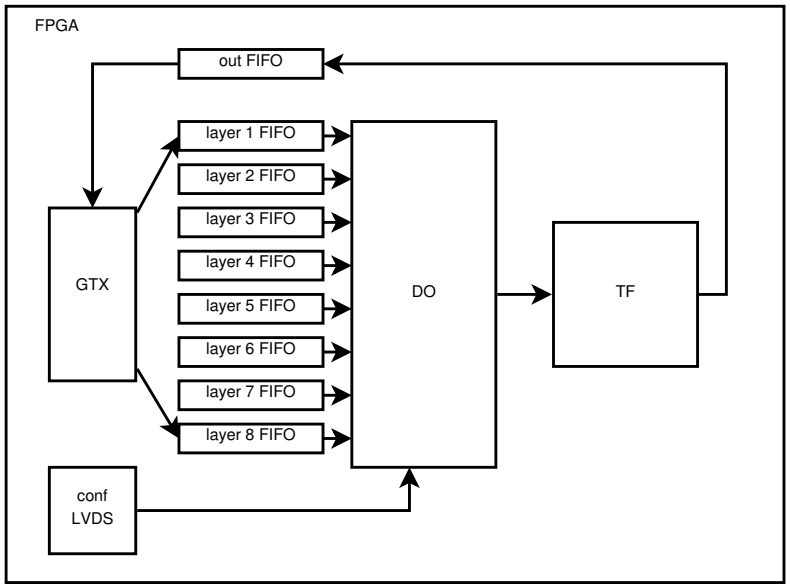
TF modifications

- TF was originally designed for ATLAS detector layout, does the fit from 11 dimensions
  - The architecture is such that for 16 dimensions, the register utilization doubles
  - This utilization is not acceptable, modifications in the architecture needed to combat that
- There are two combiner units for each TF, operating at exactly half the frequency
  - As it is, each combiner takes care of one road at a time
  - In the case of a jet, there may be some very populated roads
  - There's benefit to breaking up the processing of each road to two combiners
  - That way it's half the time in twice the combiners
  - That can increase the efficiency in events with jets

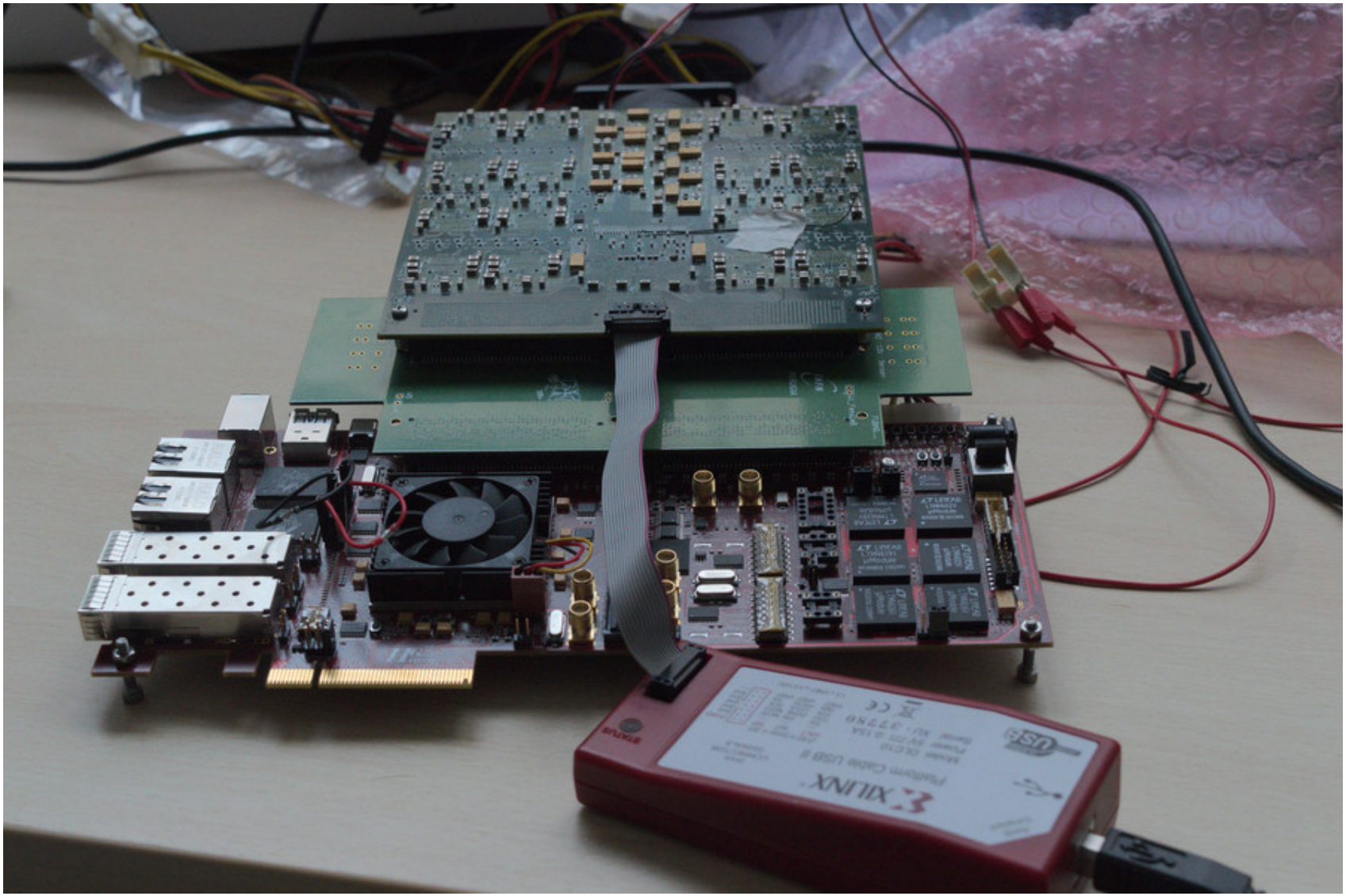
Outline

short-term goals

- Avoid using external RAM as a LUT
- Integrate DO+TF in the simplest configuration possible
- start with just 1 TF unit, 1 DO unit
  - have quick implementation cycles during integration
  - get to a simple version that just works, fast
  - be quick in identifying potential problems
  - we can add the rest of the units later

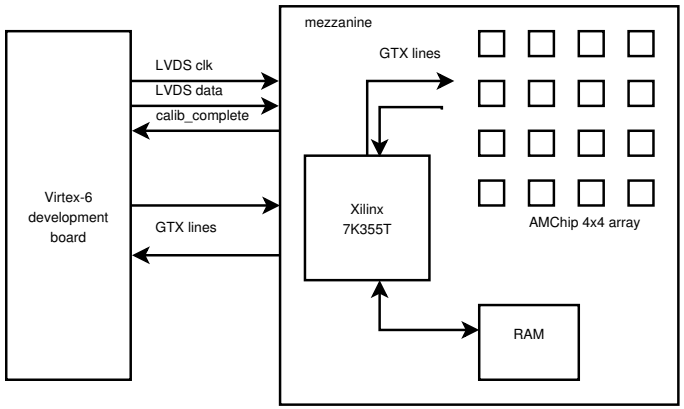


Development setup photo



Necessary connectivity

- The mezzanine sits on the Virtex-6 evaluation board on two FMC connectors
- Hit/stub data transfer is done via multi-gigabit GTX links
- Secondary communication is good to have
  - IPBus is available on the Virtex board, not on mezzanine
  - Configuration data is necessary for the DO road decoding LUT and TF fit coefficients
  - LVDS serial link is an option, not many pins and fast

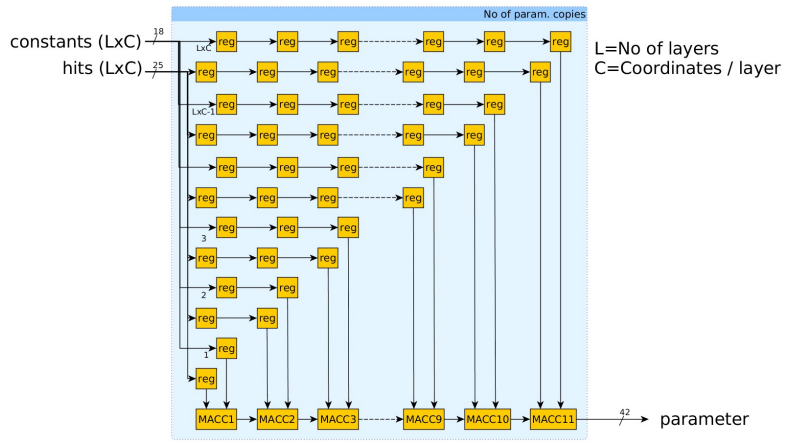


LVDS serial link

- 5 differential pairs + 1 single ended used
  - 1 differential pair for clock transmission
  - 4 differential pairs for data
  - 1 single ended to signify receiver successful calibration
- Data width on the parallel ends is 32 bits
- Link speed is 400MHz DDR, gives 3.2GBits/sec
  - 100MT/s on the parallel ends
- Custom logic developed
  - Data eye calibration
  - Word alignment
- Link has been tested using PRBS
  - zero errors up to $2.5 \cdot 10^{13}$bits, will be tested more

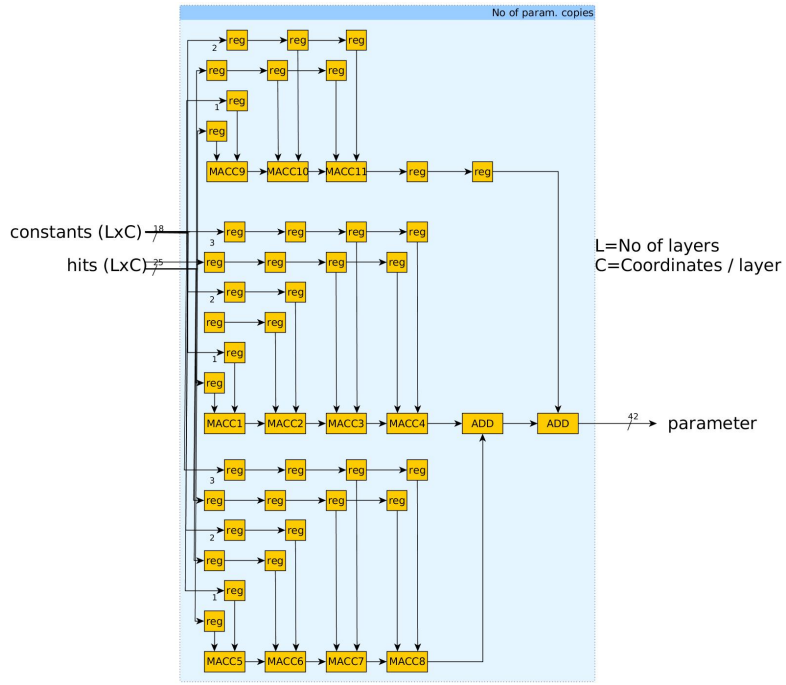
TF architecture - old

- Need to cut down on register usage
- Single computing pipeline not efficient in that way



TF architecture - new

- Broken down computing pipeline to 3 parallel ones
- +14.6% on DSP units
- - 20% on LUTs
- - 48% on registers
- 5% less latency



Summary

- Completed steps on the road to integration
  - LVDS link for configuration created
  - DO input FIFO hierarchy implemented
  - TF improvements implemented
  - Logic layout laid down
- Short-term missing steps
  - tap into existing FSM to create control signals
  - test
- Further steps
  - Add external RAM interface (already there but for DDR3)
  - Add logic to double the DO instances
  - Implement with all four TF units there
  - Realize the improvements on the combiners