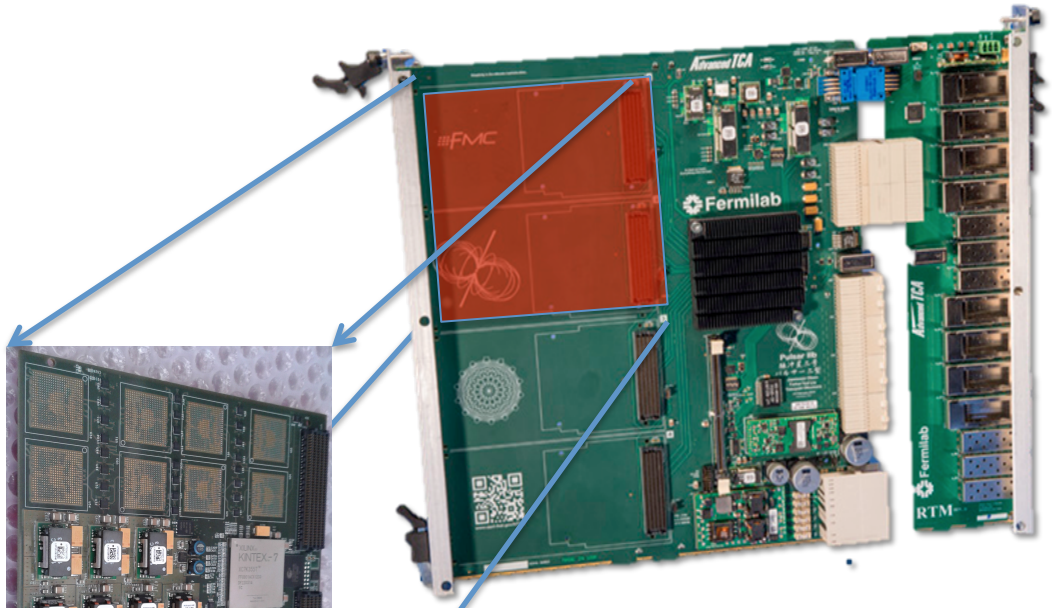
AM06 update from ATLAS FTK

Alberto Annovi
INFN – Pisa (ATLAS)

Common HW Model for Phase-II Track Triggers

ATCA

FTK Data Formatter



http://www-ppd.fnal.gov/ATCA/

future AM chip

x16

16 AM chips
1 FPGA
RAM
Power modules

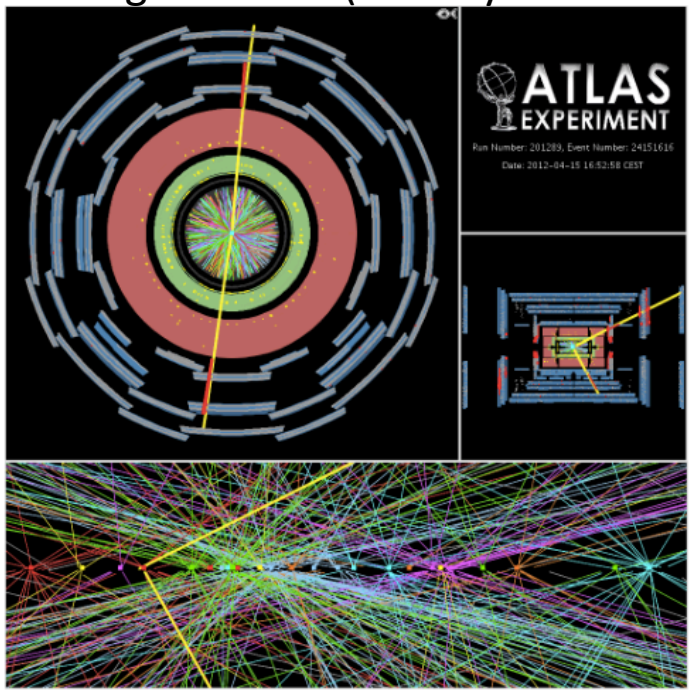
Pattern recognition mezzanine
D. Magalotti et al (RDfase2)

https://indico.cern.ch/event/299180/session/11/contribution/38/material/poster/0.pdf

Tracking & processing power

From B. Heinemann
Connecting The Dots (Berkely Feb 2015)

- Current LHC (~2015):
  - 30 tracks per collision
  - 30 collisions per event
  - 1000 events/s
  - Need to find **1M tracks/s**
- Future LHC (~2025):
  - 30 tracks per collision
  - 200 collisions/event
  - 10000 events/s
  - Need to find **>60M tracks/s**



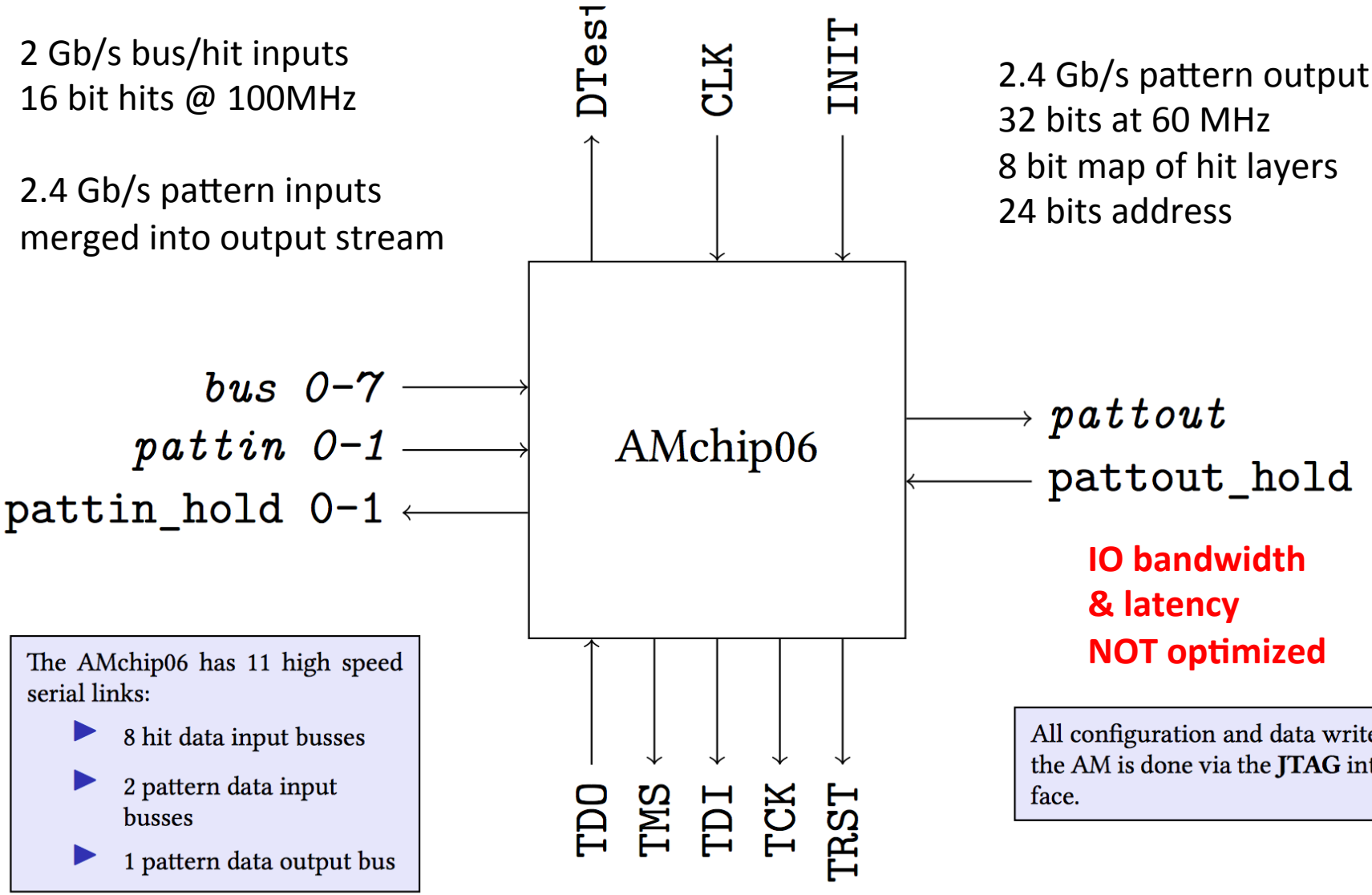
Current FTK: ~40 M track/s

- Tracking and offline processing in general **are an important challenge for Phase-II upgrades.**
- HW optimized solutions being planned considered (more) extensively:
  - track triggers can also be a offline co-processor.

AM06 logical pinout

2 Gb/s bus/hit inputs
16 bit hits @ 100MHz

2.4 Gb/s pattern inputs
merged into output stream



2.4 Gb/s pattern output
32 bits at 60 MHz
8 bit map of hit layers
24 bits address

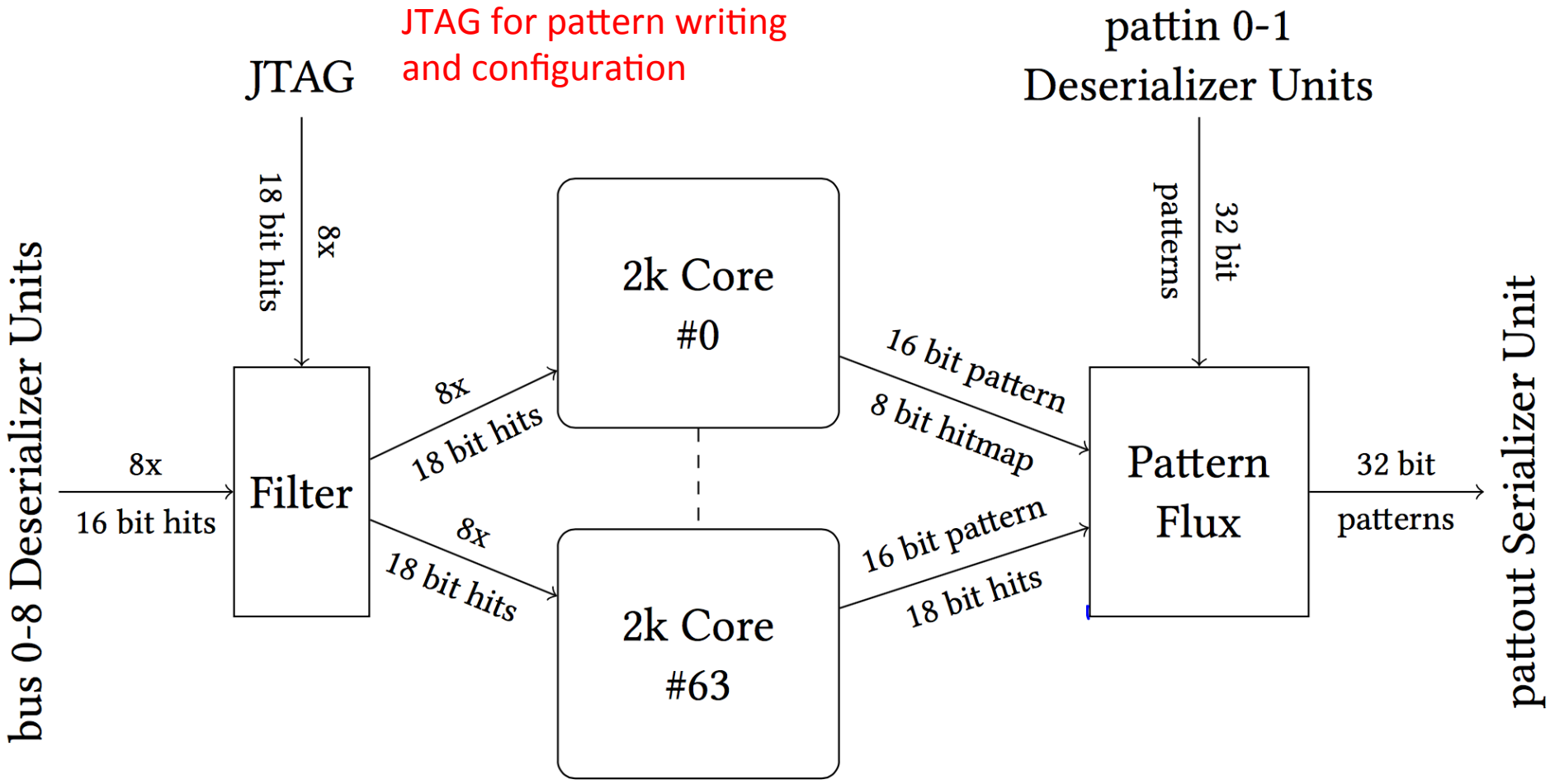
IO bandwidth
& latency
NOT optimized

The AMchip06 has 11 high speed serial links:

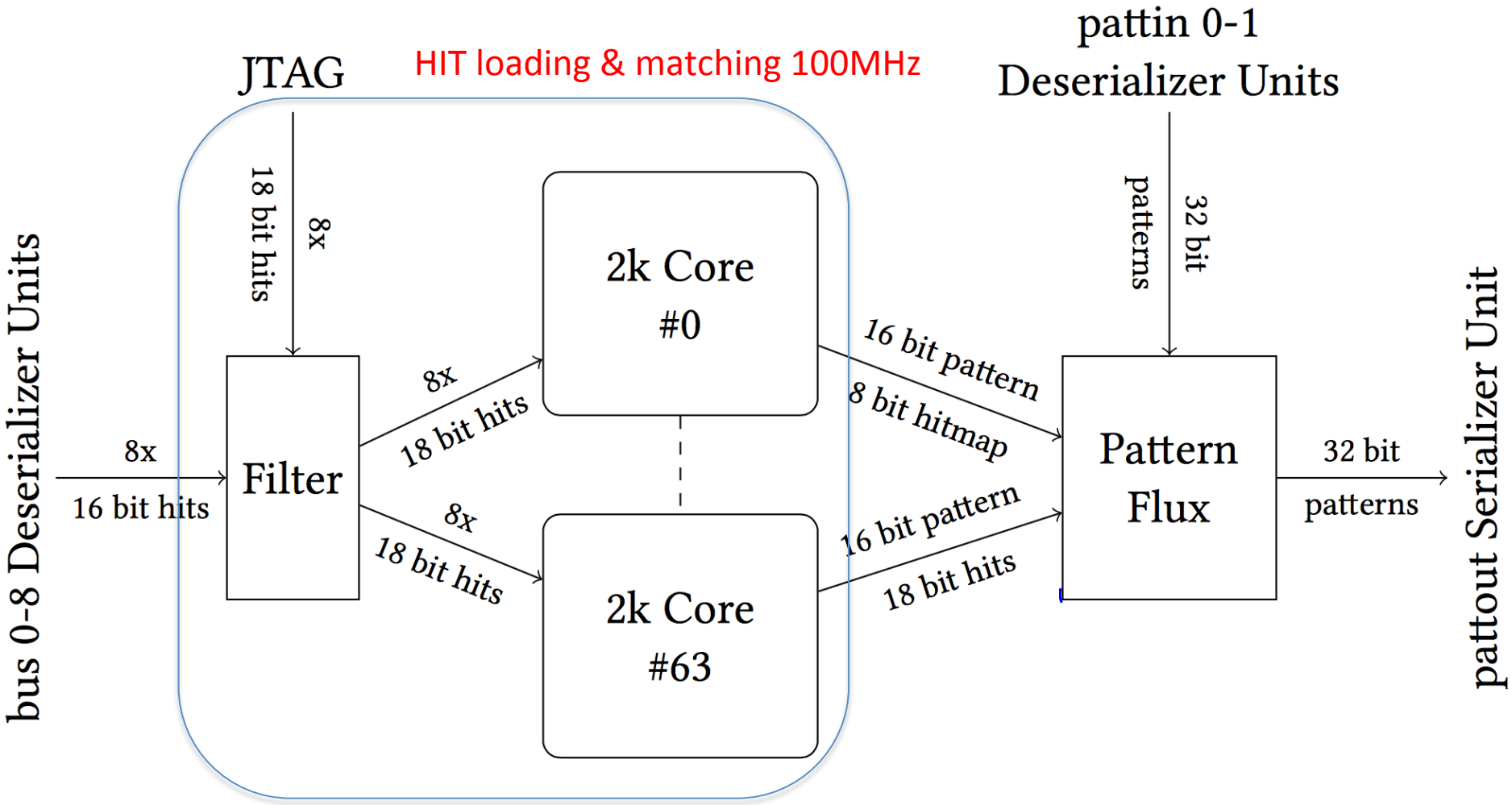
- 8 hit data input busses
- 2 pattern data input busses
- 1 pattern data output bus

All configuration and data write in the AM is done via the **JTAG** interface.

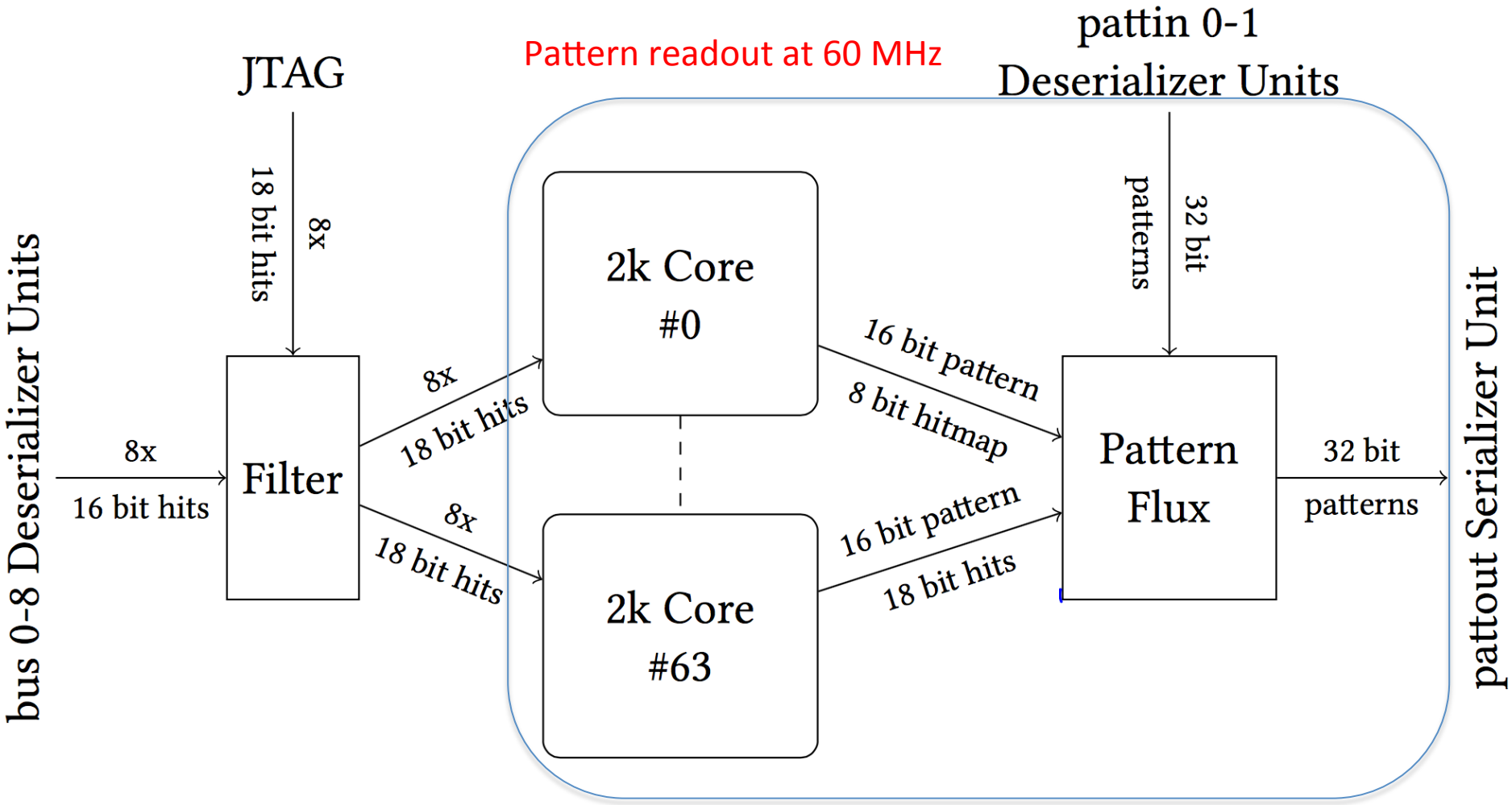
AM06 internal organization



AM06 internal organization

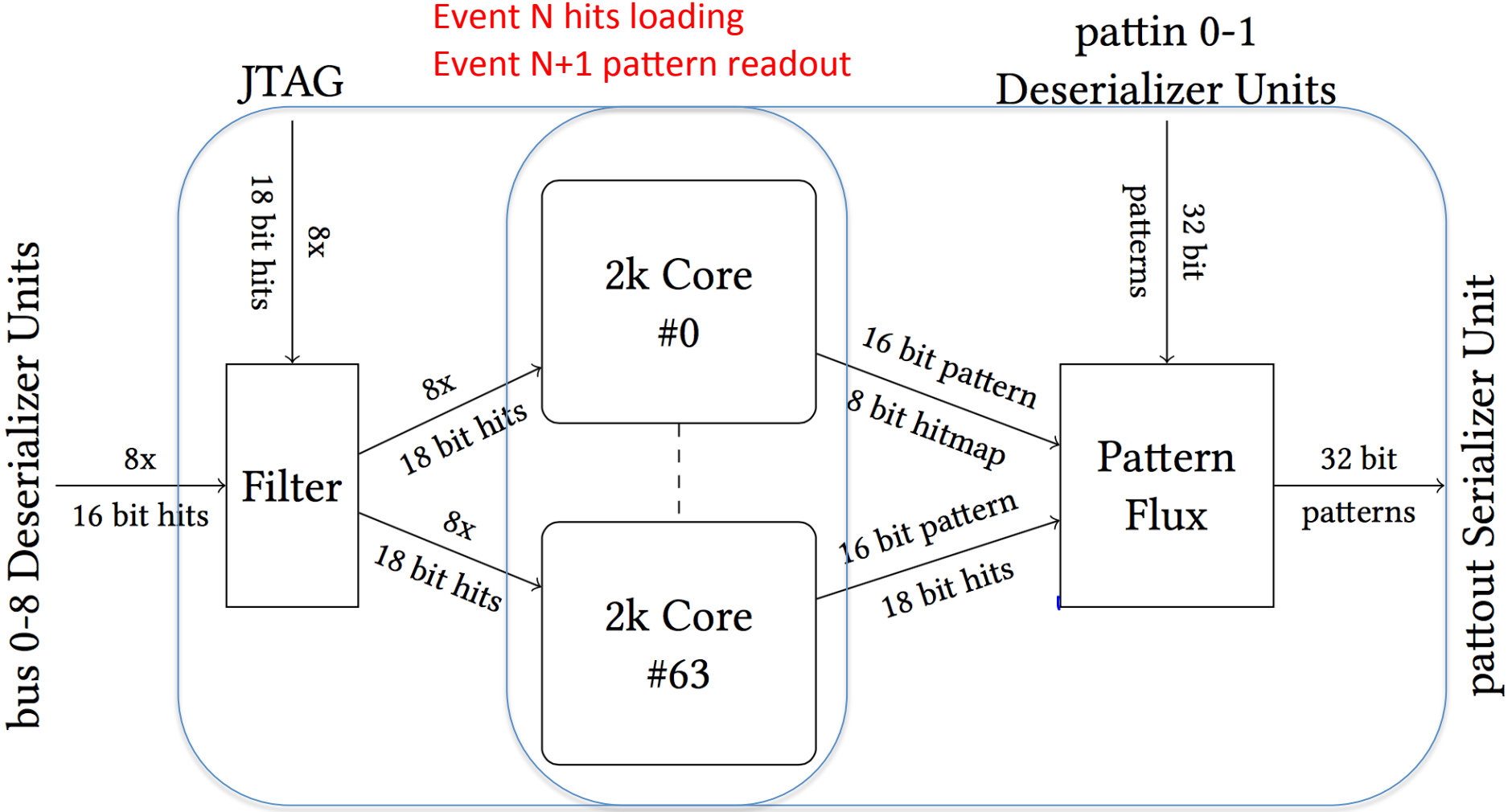


AM06 internal organization



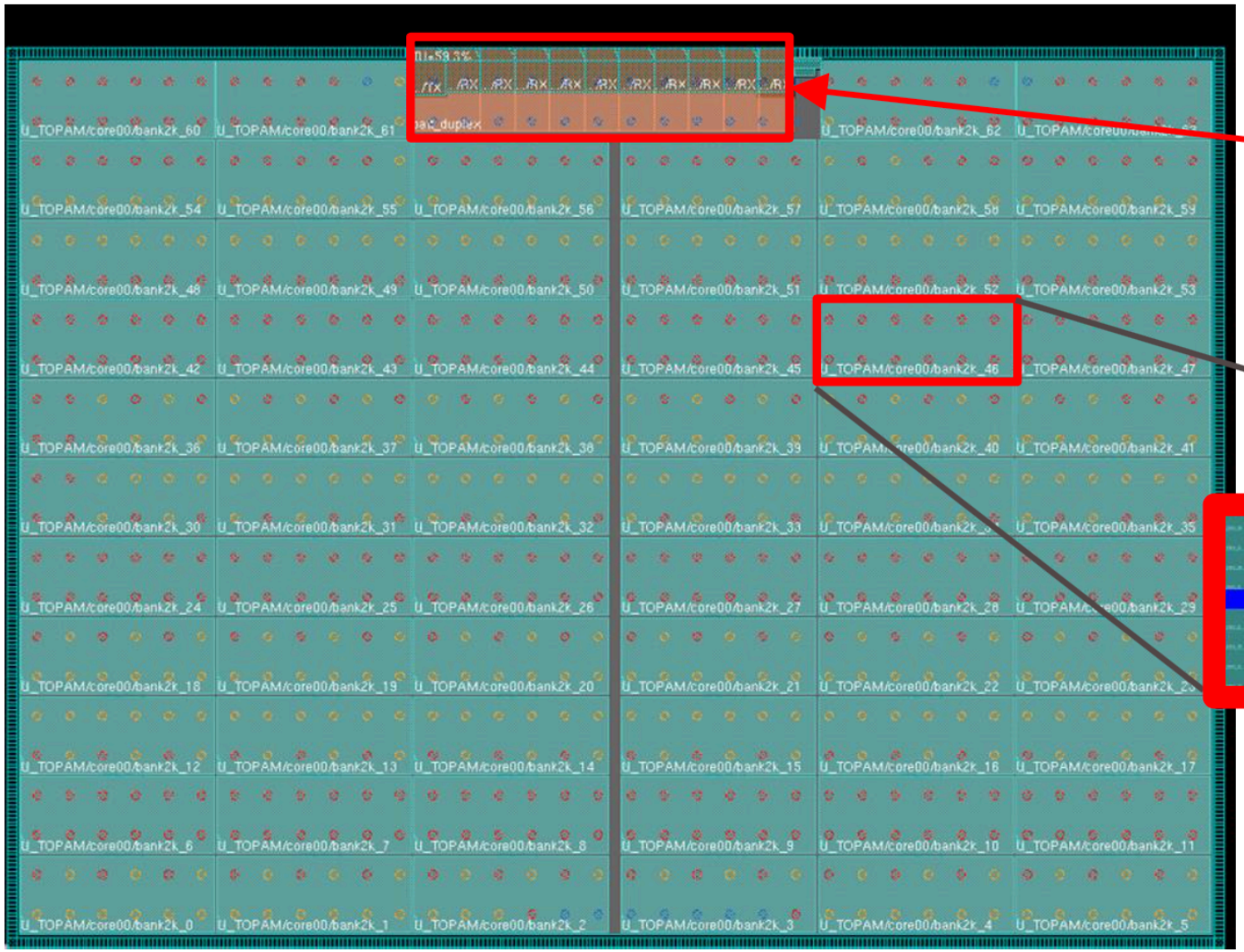
AM06 internal organization

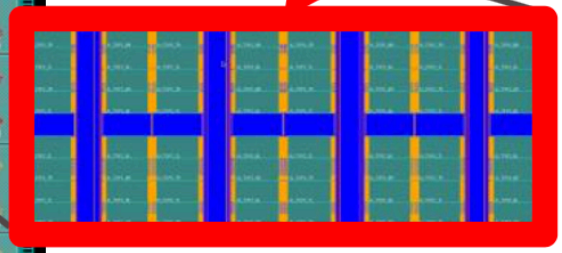
2 events processed in pipeline
Event N hits loading
Event N+1 pattern readout



Layout AM06

TSMC 65nm, size ~ 11x15mm^2, ~400transistors





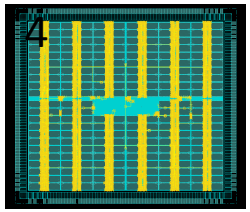
Serializer - Deserializer

2k-pattern block

4 blocchi da 64 patterns in colonna

Variable resolution with “don’t care” (DC) bits

AMchip0



- For each layer: a “bin” is identified by a number with DC bits (X)
- Least significant bits of “bin” number can use 3 states (0, 1, X)
- The “bin” number is stored in the Associative Memory
- The DC bits can be used to OR neighborhood high-resolution bins, which differ by few bits, without increasing the number of patterns

Pixels:

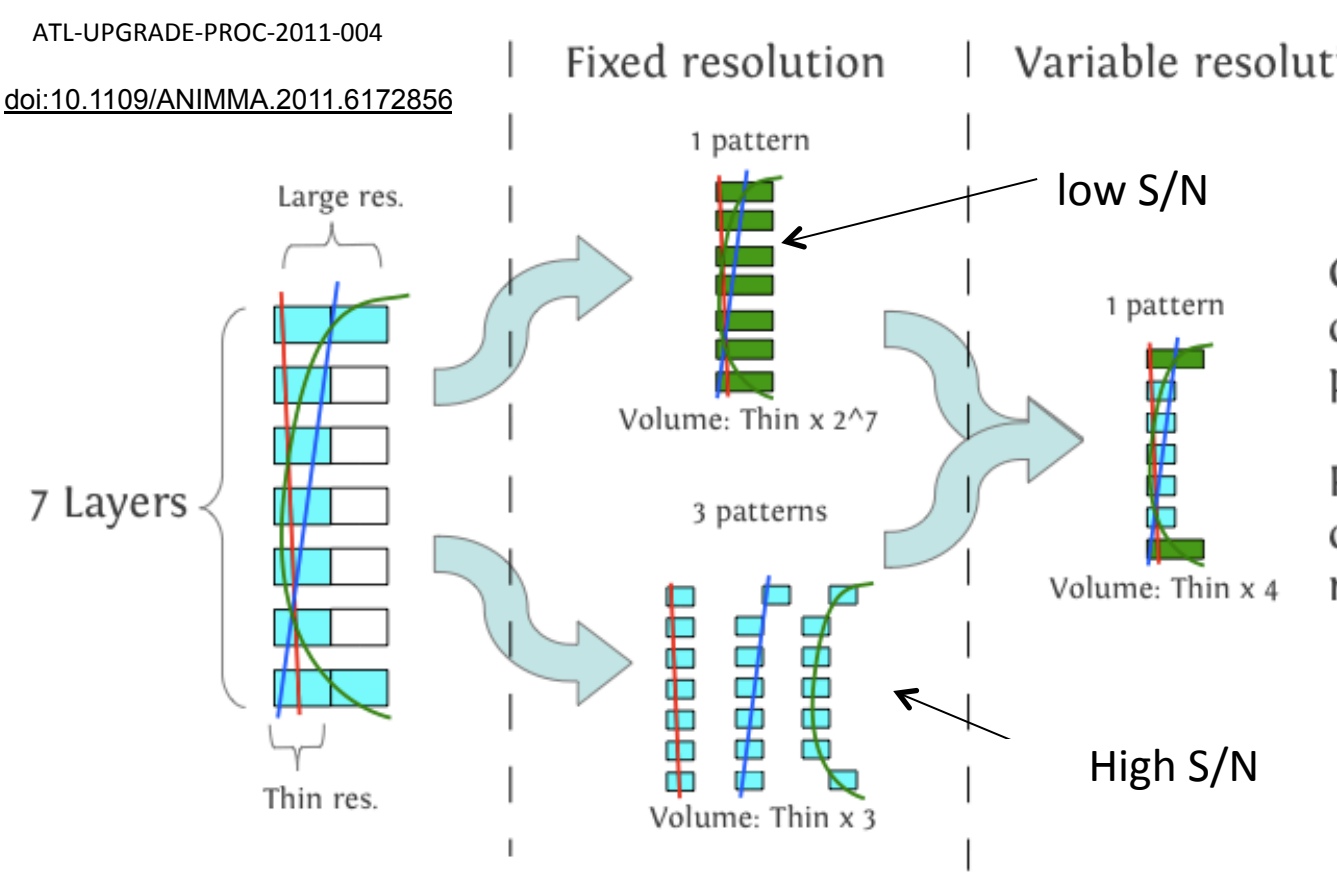
0	1	2	3	4	5	6	7
8	9	10	11	12	13	14	15
16	17	18	19	20	21	22	23
24	25	26	27	28	29	30	31

Using binary format
“01010” selects bin 10
“0001x” selects bins 2 or 3
“1x000” selects bins 16 or 24
“0x11x” selects bins 6,7,14, or 15
“111xx” selects bins 28 to 31

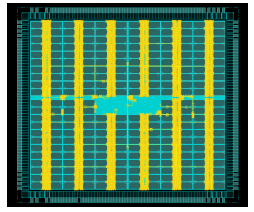
AMCHIP04: VARIABLE RESOLUTION

ATL-UPGRADE-PROC-2011-004

doi:10.1109/ANIMMA.2011.6172856



AMchip04



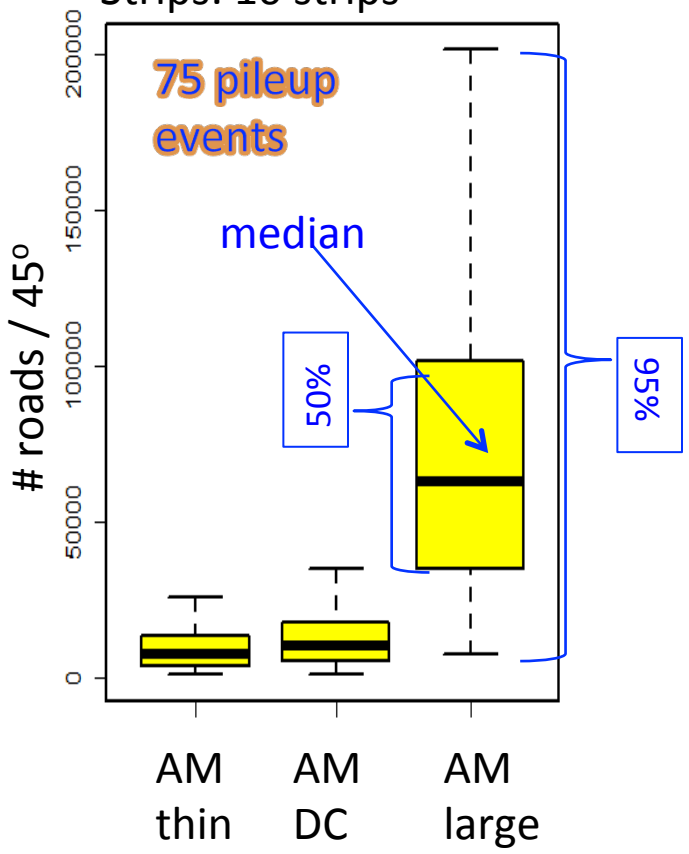
Implemented with the "don't care" feature: inspired by the Ternary CAMs

- Increases the width of a pattern only when needed
- Fully programmable
- The choice of wider or narrower width patterns is made layer by layer with simulation

Performance (max 1 DC/layer)

G. Volpi

AM thin channel grouping:
Pixels: 12 along ϕ, 36 along η
Strips: 10 strips



Pileup events	config	Max # DC bits / layer	# roads / 45°	# patterns
75	AM large patterns	0	53500	138M
75	**AM w/ DC**	**1**	**8250**	**138M**
75	AM thin patterns	**0**	5950	384M

- Pattern bank reduction factor: ~ 3
- AM with DC capability reduces the fakes by a large factor: ~ 7
- Good performance with almost same HW

FTK TDR configuration:
2 ternary cells for pixels, 1 for strips
pattern bank reduction approximately x5

Ternary cells encoding

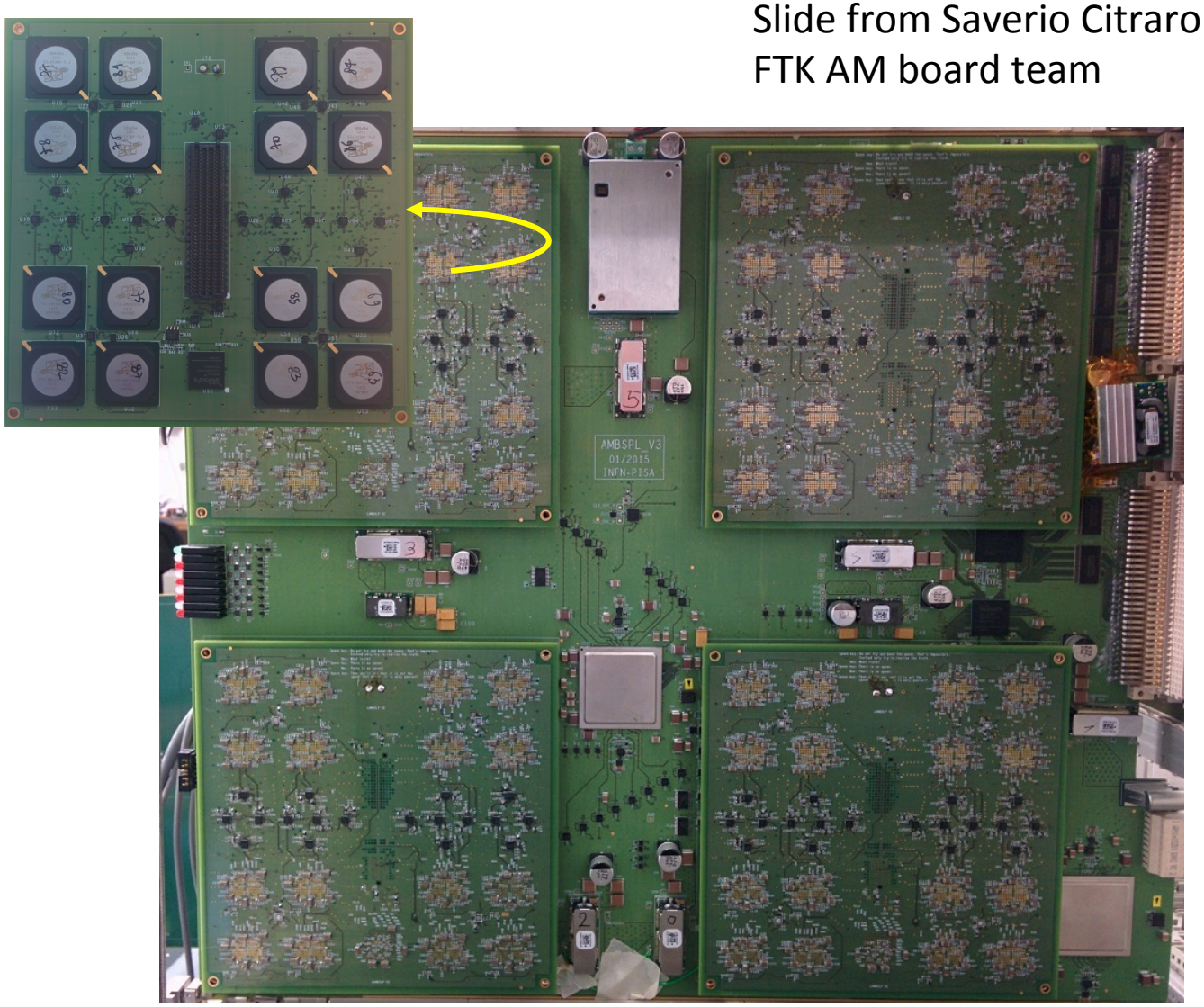
- Input is 16 bits per word per bus
  - Actually use 32 bits words with 2 hits/word
- Internal CAM have 18 bits memory per layer/word
- One ternary cells uses 2 bits internal memory
  - Can store 0, 1 and X (X= don't care)
- Possible configurations:
  - 16 bits input – 2 ternary cells
  - 15 bits input – 3 ternary cells
  - …
  - 9 bits input – 9 ternary cells
  - Extra input bits are ignored
- Number of ternary cells is programmable for each layer independently

AMBSLP

With 64 AM05 chips

Slide from Saverio Citraro
FTK AM board team

- Serial Links @ 2Gb/s
- VME 9 U
- Clock @100MHz
- Supply Voltages:
  - 2,5V
  - 1,8 V
  - 1,2V
  - 1V
- Power consumption:
  ~ 250 Watt



AM05/06 chip power

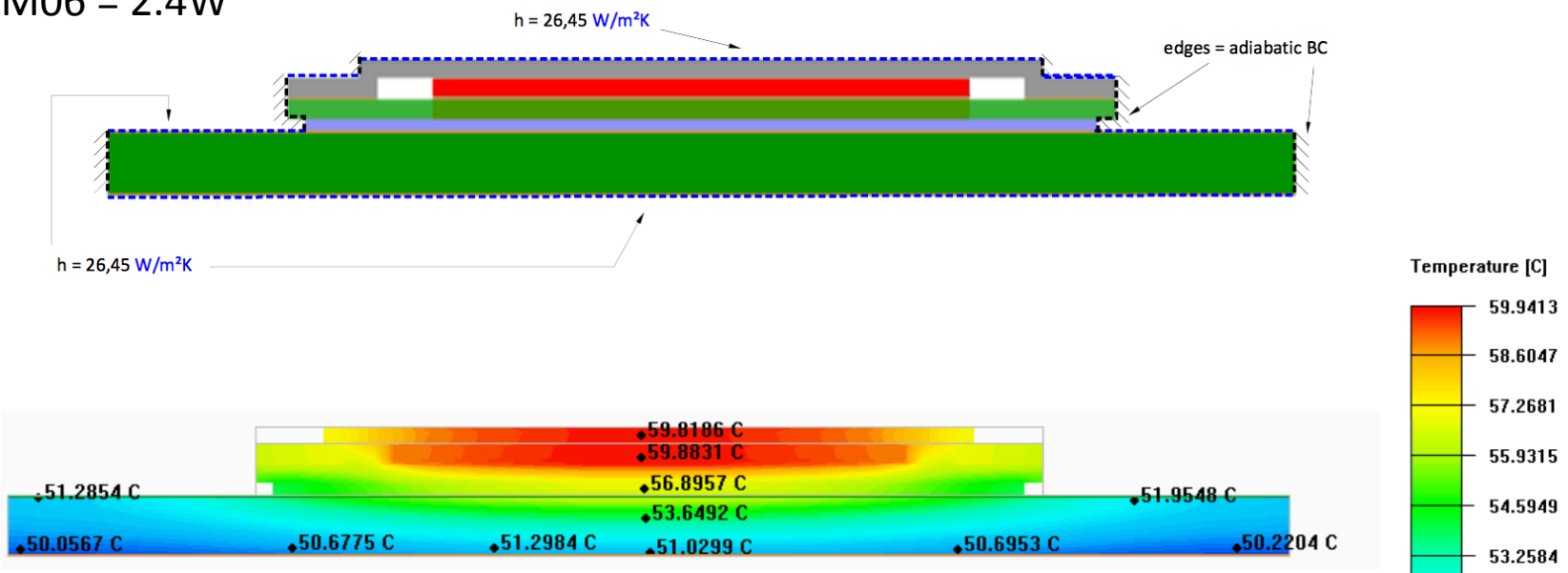
- Measurements from a few AM05 chips
  - Please check them on board and add margin as appropriate
- 3 voltages: 2.5, 1.2, 1.0
- 2.5 V (IO) roughly 120mA average
  - Please assume > 150-200mA
- 1.2 V (ser des core) 60mA average
  - Please assume > 100mA
- IO + serdes power ~ 0.4W
- 1V (core) power estimate 3W +- 20% (AM06 extrapolated)
  - At full usage 100% hits loaded at 100 MHz (times 8 inputs)
  - Requires +-50mV ripple on board (+-50mV ripple internally)
- "Possible" dissipated power 3W*70% + 0.4W ~ 2.5W
- Requires low jitter clock

AM06 thermal sim (IMEC for FTK)

P. Giannetti

Only top and bottom sides with h-coefficient

Power/AM06 = 2.4W

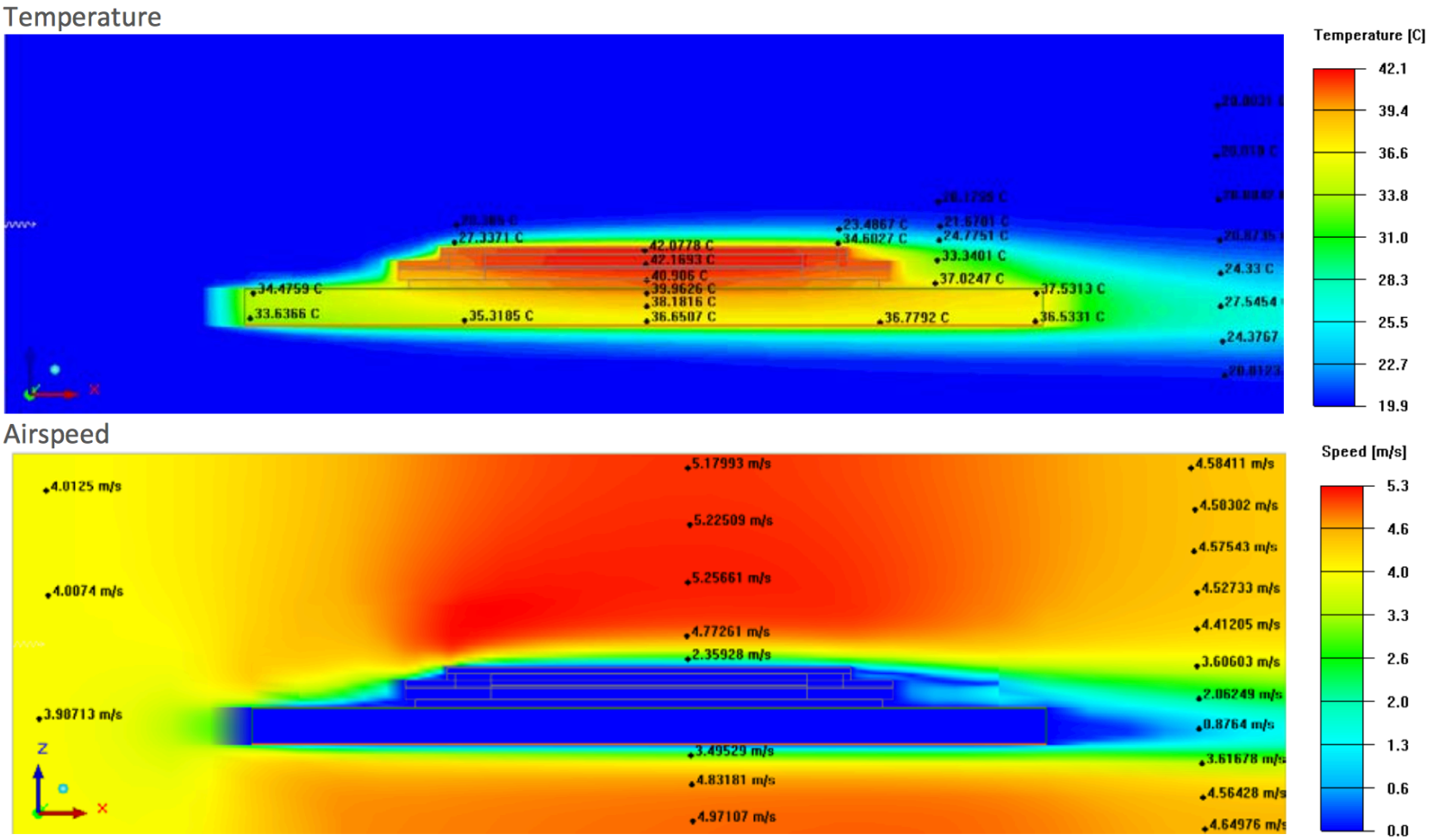


Heat flow to package top (heat slug): 0.53W (22%)
Heat flow through side package (side of substrate and solder balls): 0.10W (4%)
Heat flow through PCB: 1.77W (74%)

AM06 thermal sim (IMEC for FTK)

Power/AM06 = 2.4W

4m/s →



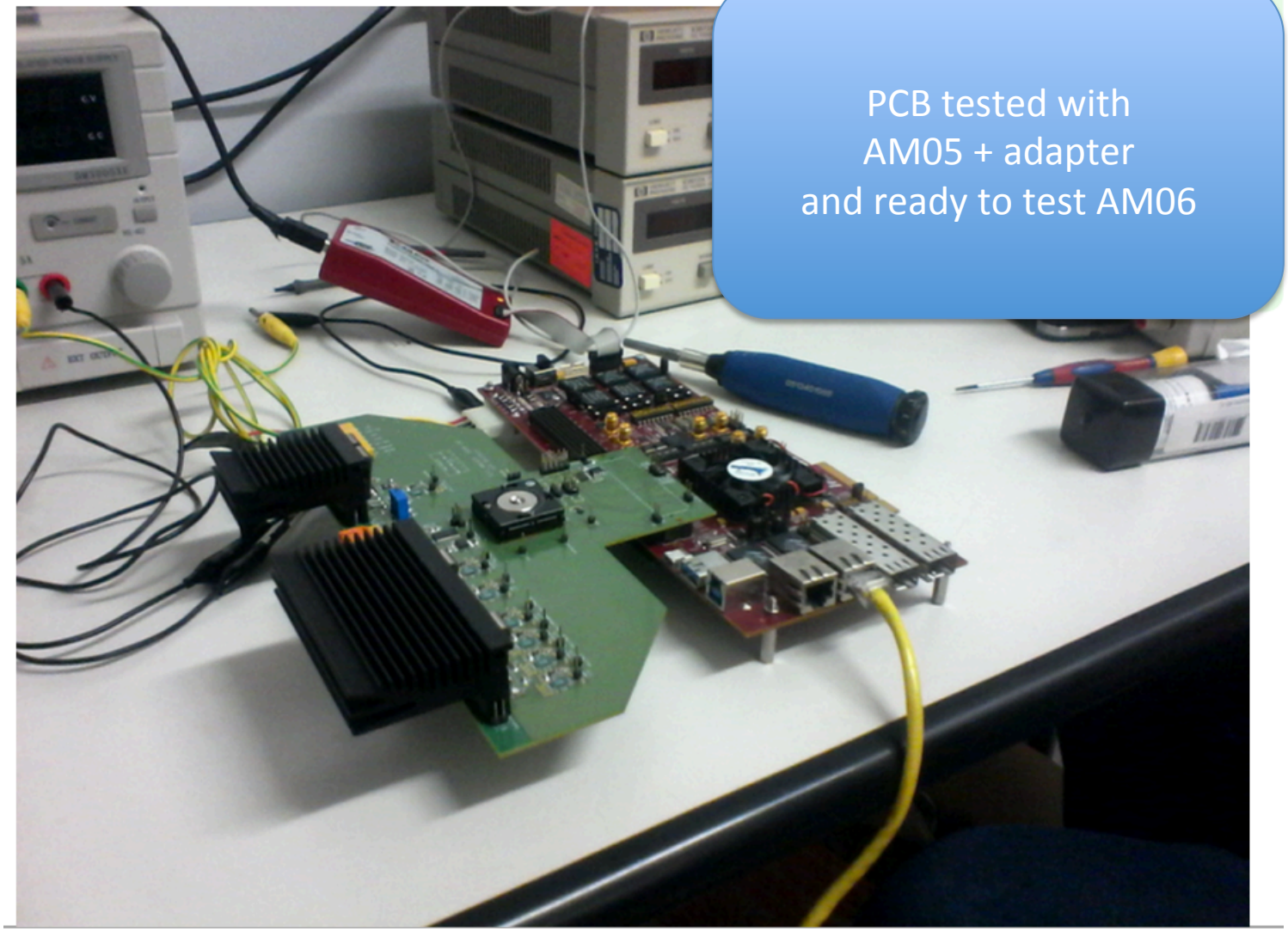
FTK AMchip

M. Beretta, F. Crescioli, A. Stabile, an others

- FTK AM06 submitted July
  - Packaged AM06 for FTK arriving mid-October
  - 9 wafers split: 3 typical, 3 slow, 3 fast
    - Unless crisis for initial FTK installation, plan to use some for phase-II studies
- Next steps
  - Characterize typical chips
    - Select and install 64 on a FTK AM board
  - Characterize slow and fast corners
  - Test all devices

AM06 test mezzanine

Mezzanine by
INFN Frascati
M. Beretta et al



PCB tested with
AM05 + adapter
and ready to test AM06

Next steps

- We are looking forward to get AM06
- Ready for characterization and initial testing