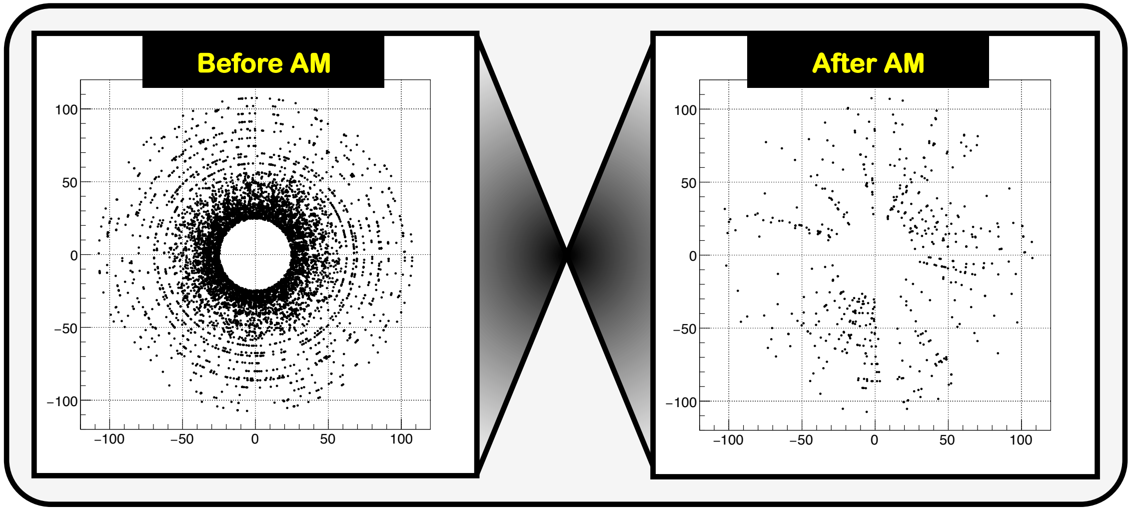
Geometry, pattern banks, and data formats



Geometry
Data formats
Pattern banks

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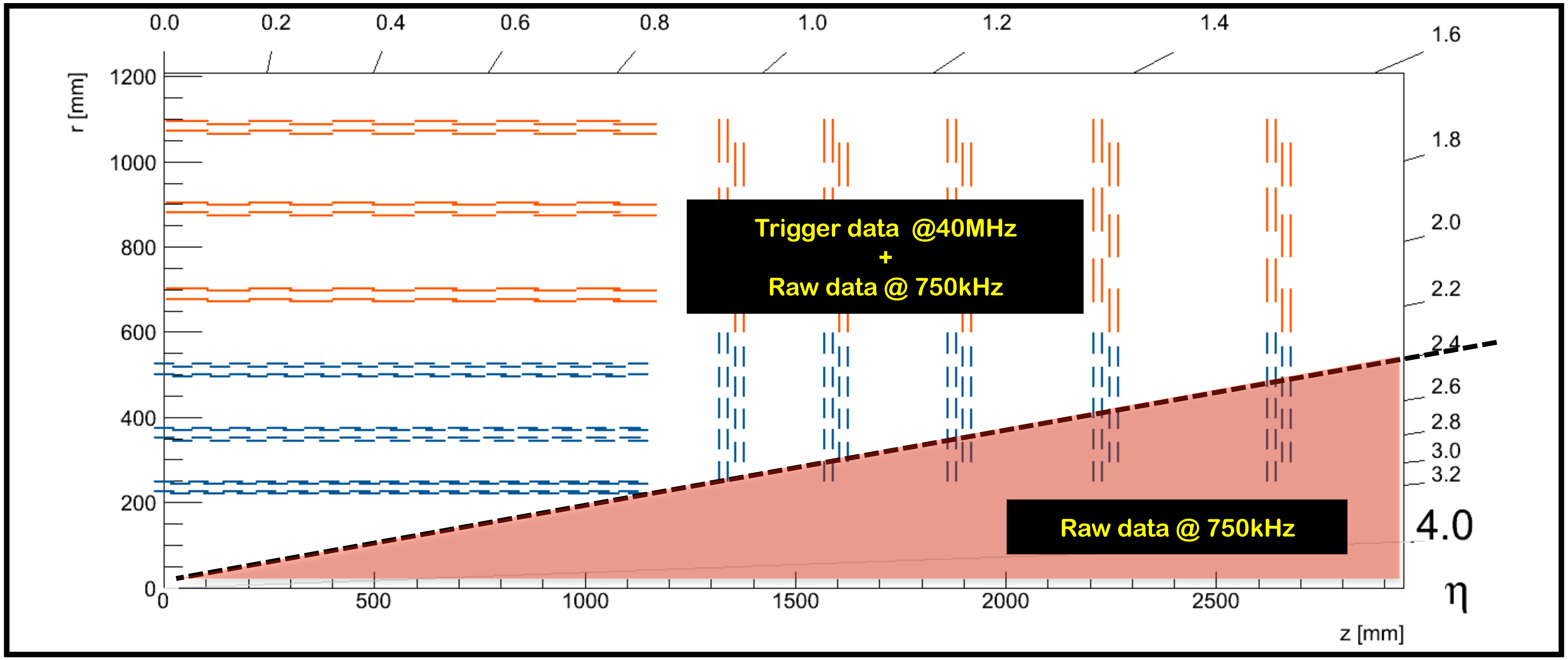
for the Lyon AM team

→ **Phase II tracker geometry (*Technical Proposal* (*)):**



→ L1 tracking capability up to **|η|=2.4.**

→ All the modules have a good ϕ resolution (***strip pitch 90μm***)

→ r/z pitch of the **PS modules** is 1.5mm in the disks/barrel

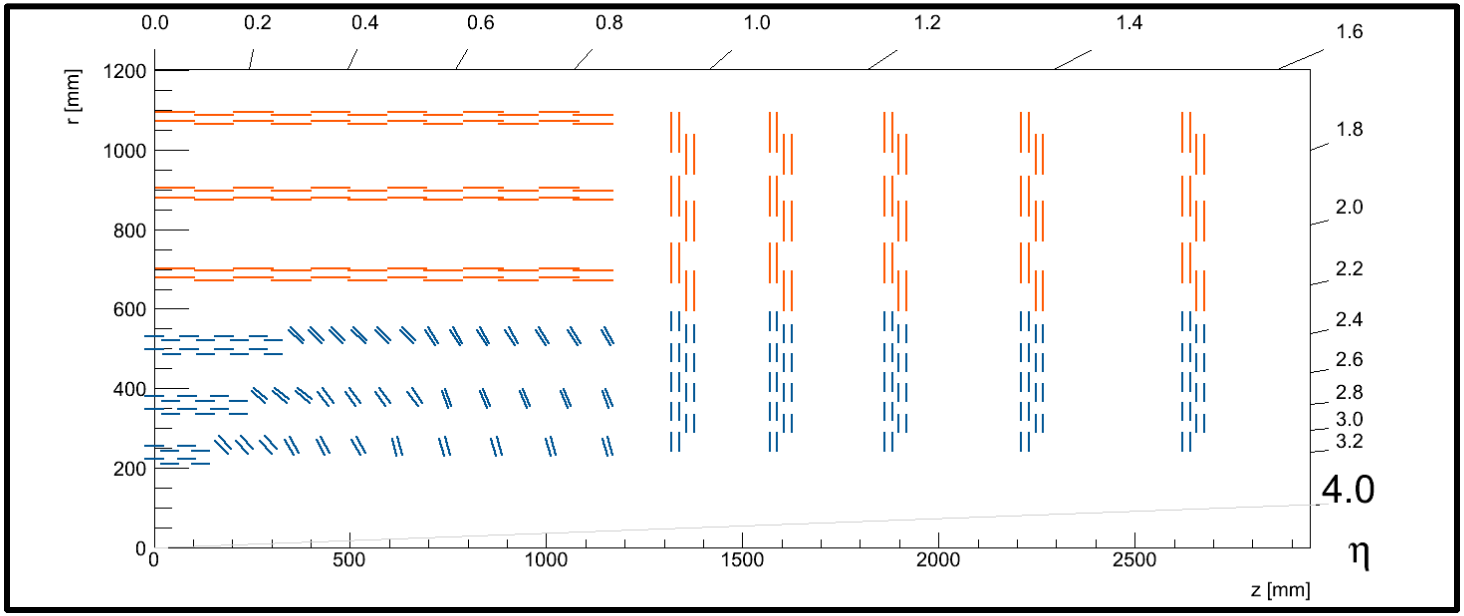
→ r/z pitch of the **2S modules** is 5cm in the disks/barrel

→ (*)***Reference:*** S.Mersi: http://mersi.web.cern.ch/mersi/layouts/.current/TechnicalProposal2014/index.html

→ **<u>Future geometry (*not for the demonstrator*):</u>**

→ **Tilted geometry**(*) is currently studied, as it allows to:

- Reduce the amount of material at high rapidity
- Reduce the cost (*less modules*)
- **Heavily simplifies the PS modules FE electronics**

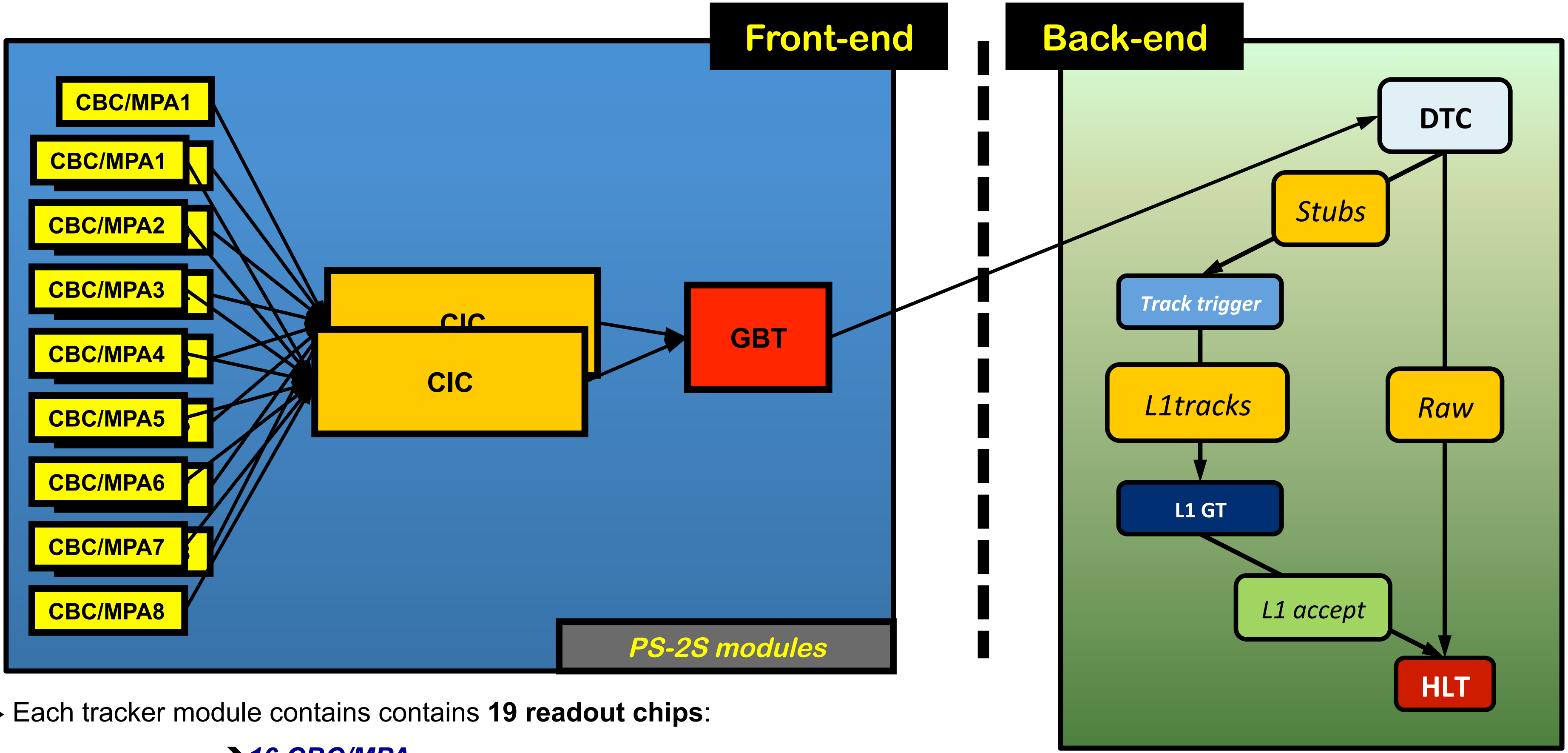


→ Available in CMSSW before end of 2015.

→ **Should be relatively harmless for the AM approach** (*apart from the fact that we will have to redo everything…*)

→ (*)***Reference:*** S.Mersi: http://mersi.web.cern.ch/mersi/layouts/.current/ShortTilted3xPS_3x2S_5disks_longer_uncut/index.html

→ **Phase II tracker data extraction protocol (*):**



→ Each tracker module contains contains **19 readout chips**:

➔ *16 CBC/MPA*
➔ *2 CIC* ➔ **this is where the core stub data format is defined**
➔ *1 GBT*

→ (*)***Reference:*** F.Vasey: https://indico.cern.ch/event/326723/session/4/contribution/11/material/slides/0.pdf

→ Latest CIC 2S data format (*PRBF.raw*):

→ The stub payload is what will be received on the PRM (*along with tower module info*)

320 bits																	
header												payload list of stubs					trailer
	error / status bit									bx ID	nb stub	bx ID	chip ID	stub address	stub bend		
0	CBC1	CBC2	CBC3	CBC4	CBC5	CBC6	CBC7	CBC8	concentrator							....	
1b	9bits									12bits	4bits	3bits	3bits	8bits	4bits		Bits at '0'

→ It was shown that **4 bits are sufficient for the bend**(*). Means that 2S stub size is now 18 bits. Up to 16 stubs per block. Limited to 15 as sufficient.

→ Up to **30 stubs / 8BX / module**

→ Sufficient for 2S trigger info transmission up to PU200 (**)

→ (*)***Reference:*** SV: https://indico.cern.ch/event/350910/session/4/contribution/12/material/slides/0.pdf

→ (**)***Reference:*** SV: https://indico.cern.ch/event/375536/session/4/contribution/21/material/slides/0.pdf

→ Latest CIC PS data format (*PRBF.raw*):

320 bits										
header				payload / list of stubs						trailer
	error / status bit	bx ID	nb stub	bx ID	chip ID	stub address	stub bend	z pos		
1	MPA1, MPA2, MPA3, MPA4, MPA5, MPA6, MPA7, MPA8, concentrator								....	
1b	9bits	12bits	4bits	3bits	3bits	8bits	3bits	4bits		Bits at '0'

→ It was shown that in PS **3 bits are sufficient for the bend** (*see previous slide for ref.*). Means that PS stub size is **21 bits**. Up to 35 stubs per CIC block in the most ambitious GBT transmission projection (*to be confirmed*)

→ Up to **70 stubs / 8BX / module (*was 20 until now*)**

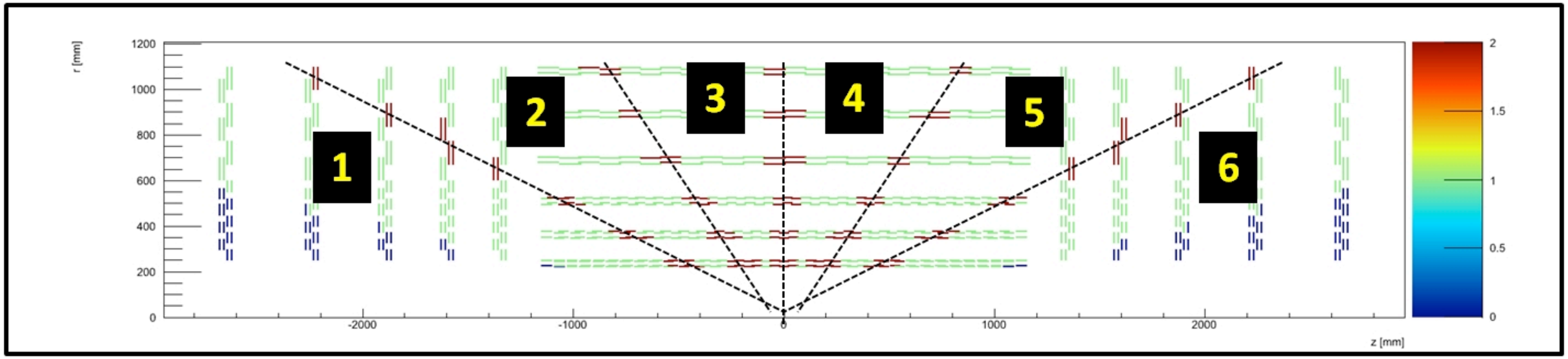
Mode	TRG size	N_{stubs}/CIC
LP-SEC	***320***	**14**
LP-LEC	***384***	**17**
10G-SEC	***640***	**29**
10G-LEC	***768***	**35**

Sufficient to pass all the stubs at PU200 if 3GeV/c threshold

→ (*)***Reference:*** SV: https://indico.cern.ch/event/350910/session/4/contribution/12/material/slides/0.pdf

→ Trigger towers:

→ At the backend level, DTC boards send the stubs into dedicated trigger towers (***optimal tracker to DTC cabling crucial, but far from simple***)



Eta range	1	2	3	4	5	6
Sector numbers	*0→7*	*8→15*	*16→23*	*24→31*	*32→39*	*40→47*

→ Three tower types: **barrel**, **hybrid**, and **endcap**

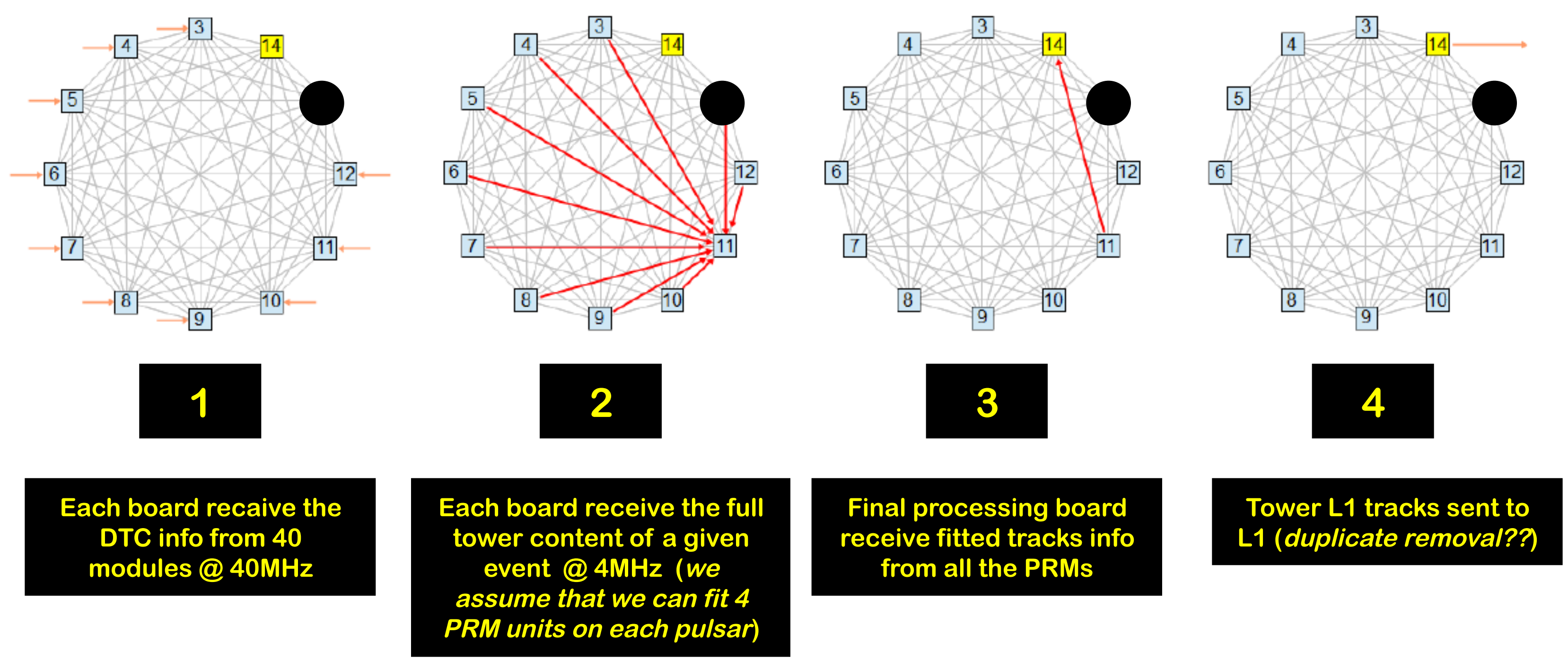
→ A stub never belongs to more than 4 towers

→ **Total PRBF.raw rate in one tower:**

→ **We consider that all the stubs will arrive into the PRB boards (*3GeV/c threshold*)**

→ Based on tower stub rates, we can estimate the **data transfer rates in an ATCA shelve containing 10 PRB boards.**

→ For simplicity, we assume that there is no communication between shelves (*ie no gateway board, job done in the DTCs*), and that there is ~400 modules/tower

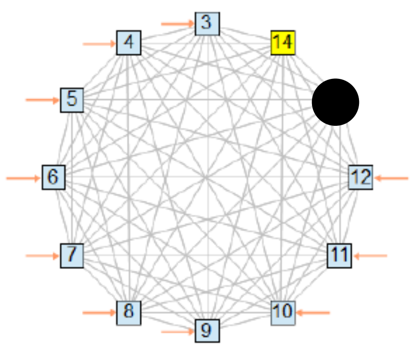


Simplified track trigger data flow (DIP/PRB combo (*) with data splitting in the DTCs)

→ (*)***Reference:*** J.Olsen: http://indico.cern.ch/event/271059/contribution/2/material/slides/1.pdf

→ Max and average stub rate per tower (DTC➔PRB):

→ For step 1, the routing will have to be done wisely in order to **ensure that each PRB receives roughly the same amount of data.**



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Each board recaive the DTC info from 40 modules @ 40MHz

→ Average rates measured with 1000 PU+4tops events, with a 3GeV/c stub threshold. 95% limits are also given (*ie 95% of the events are below this values*).

Rates in stubs/tower/BX		PU140			PU200		
		Tower type			Tower type		
		Barrel	Hybrid	Endcap	Barrel	Hybrid	Endcap
3GeV	*Average rate*	240	261	307	339	373	459
	95% lim	*339*	*357*	*423*	*462*	*497*	*620*

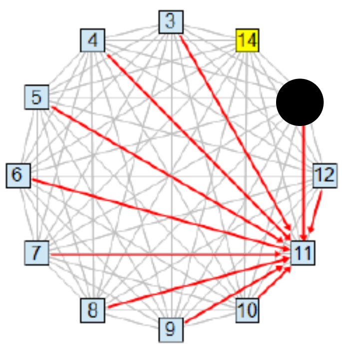
→ Means that in 95% of the case, PRB rate is lower than 62 stubs per BX at PU200. Assuming 40 bits per stubs, this corresponds to a **max *'average'* input rate of ~100Gbps per PRB board from the DTCs**

→ Of course, tails will always occurs, but 100Gbps is already an overestimate of the average load.

→ Max stub rate per PRM (PRB➔PRB):

→ Safe upper limit from DTC to PRB is ~100Gbps (*PU200/3GeV threshold/busy events only*)

→ From there one can get the upper limit **from PRB to PRB.**



2

Each board receive the full tower content of a given event @ 4MHz (*we assume that we can fit 4 PRM units on each pulsar*)

→ Each PRB receives every 1 out of 10 events the data from 9 other PRBs

→ Max rate from PRBs to PRBs is therefore 100/10*9 = **90 Gbps**

→ Means a **max input rate per FMC connector of ~25Gbps (*should not forget the 10th PRB data*)**

→ **Once again these values provide a safety factor of ~35% wrt what we will get at max on average.** It is well within the spec of the pulsar FMC connector (*64Gbps*)

→ This is for PU200, with a 3GeV threshold.

→ **PRB➔PRM friendly format conversion should occur here**

→ **What are we aiming for, for the three tower types?**

→ Main requirements (***necessary whatever the trackfit strategy is***):

→ Banks with **~1M patterns per tower**

→ **No efficiency loss for p_T>5GeV/c**, **more than 95% efficiency below that (*particularly in jets*)**

→ Less than **50% fake roads** (*ie roads containing less than 4 stubs from a good primary particle*)

→ Less than **100 matched roads per tower in average,** for PU up to 200

→ If possible, less than **100 matched roads per tower in 95% of the events** (*ie account for tails*)

→ Latest bank properties:

→ The latest emulator is not yet on CMSSW, but available on github (***https://github.com/gbaulieu/amsimulation***).

→ It now includes:

- **Fountain patterns** (*superstrip size radius dependent*) in barrel and endcaps
- **DC bit allocation per layer** (*layers can have different DC bit numbers*)
- New methods to print bank information
- Possibility to **truncate a bank to a given size** (*keeping only the most probable patterns*)
- Lots of methods for the testbench are also currently developed (*CMSSW interface*)

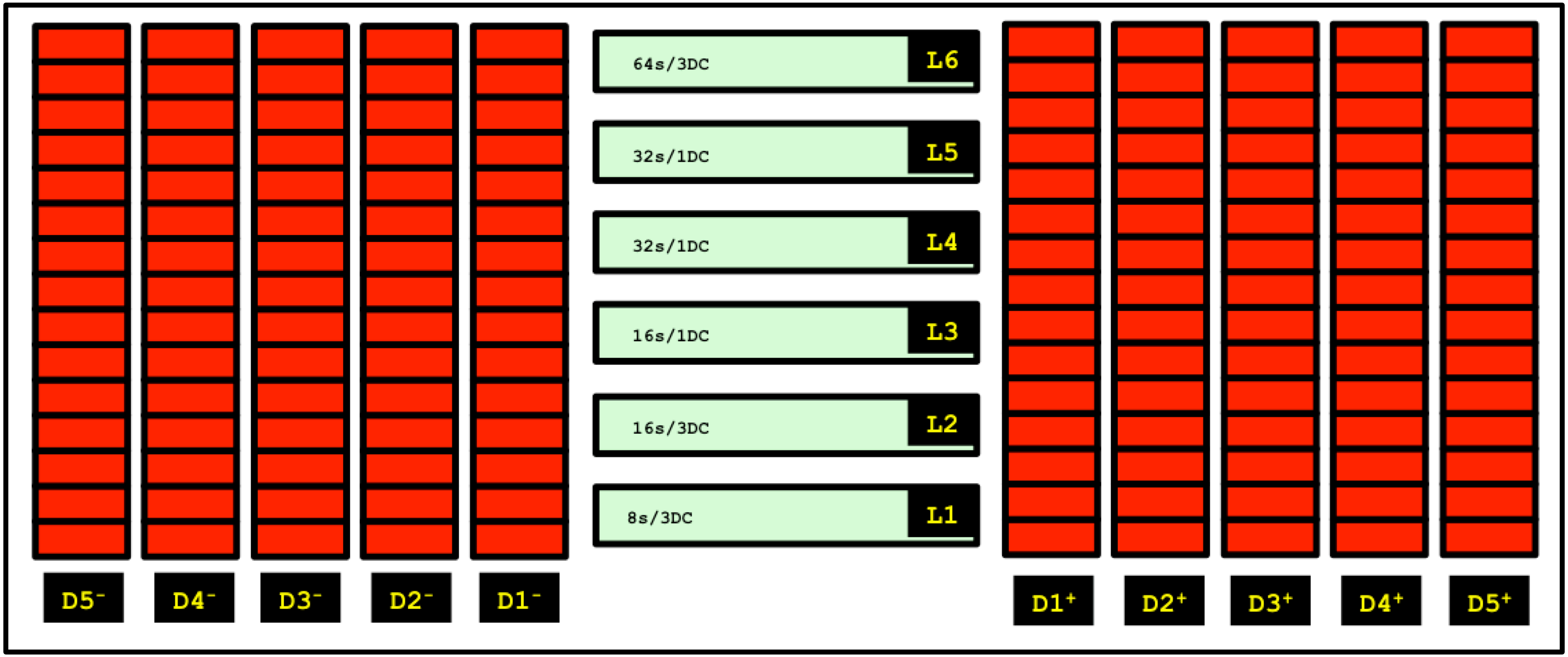
→ A set of banks using all those features was created:

srm://lyogrid06.in2p3.fr/dpm/in2p3.fr/home/cms/data/store/user/gbaulieu/SLHC/bank_150828_merged/truncated/

→ Banks are built using only tracks with a p_T>3.1GeV/c

→ This set of banks is the result of a long optimisation process, but considering the enormous AM parameter phase space, this is not the end of the story…

→ Legacy bank properties (*barrel*):

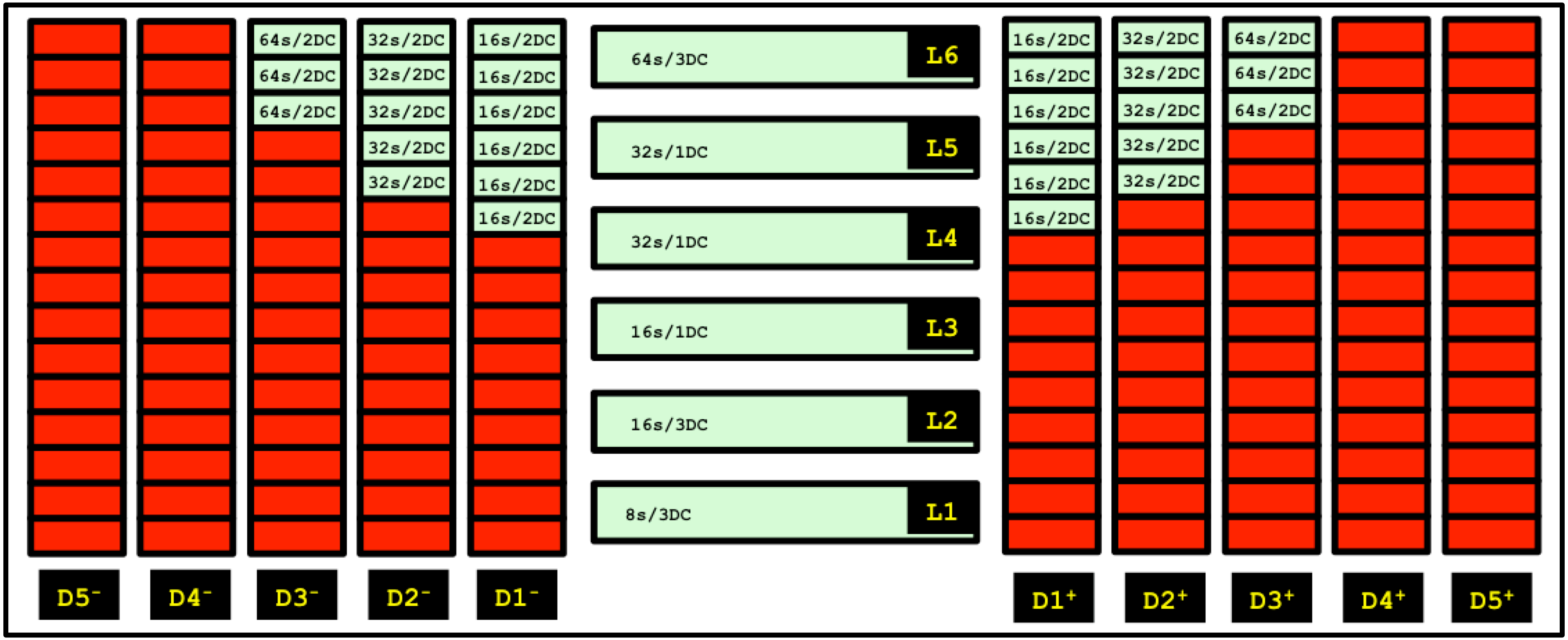


→ First number is the Sstrip ϕ width, in strips, second value is the max number of DC bits in the layer.

→ Z granularity is the module

→ **Bank truncated to 1M patterns**

→ **Legacy bank properties (*hybrid*):**

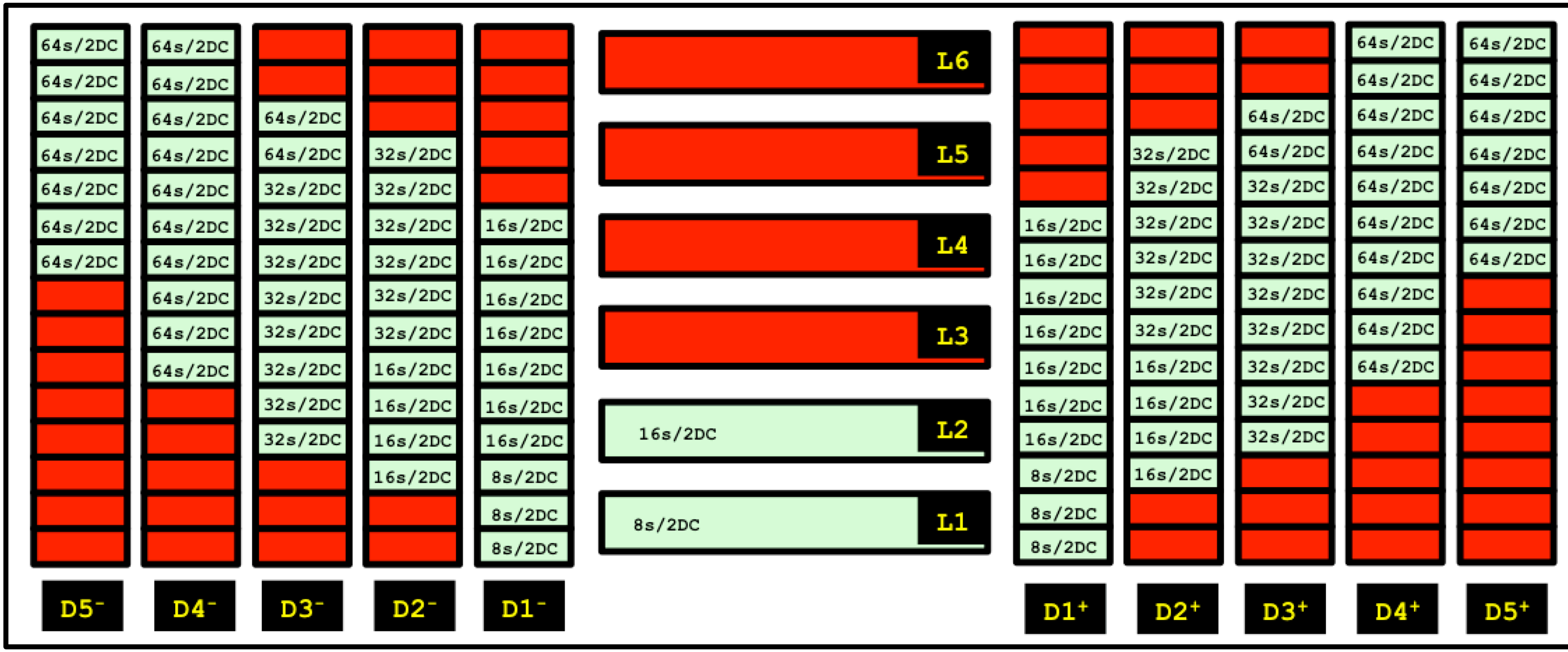


→ First number is the Sstrip ϕ width, in strips, second value is the max number of DC bits in the layer.

→ Z/R granularity is the module

→ **Bank truncated to 1.5M patterns**

→ Legacy bank properties (*endcap*):



→ First number is the Sstrip ϕ width, in strips, second value is the max number of DC bits in the layer.

→ Z/R granularity is the module

→ **Bank truncated to 1M patterns**

→ <u>Legacy bank performances (*efficiencies*):</u>

→ Total number of patterns is 56M (*~440 AM06 chips, so ~18k chips for the full system*)

	Muons		Electrons		PU140 + 4tops		PU200 + 4tops	
	$p_T \geq 3$	$p_T \geq 10$	$p_T \geq 3$	$p_T \geq 10$	$p_T \geq 3$	$p_T \geq 10$	$p_T \geq 3$	$p_T \geq 10$
ϵ^{SR}	$100.0_{-0.05}$	$100.0_{-0.05}$	97.0 ± 0.1	98.4 ± 0.1	98.0 ± 0.1	98.4 ± 0.2	98.1 ± 0.1	98.5 ± 0.2
ϵ^{TW}	99.9 ± 0.05	99.9 ± 0.05	99.8 ± 0.05	99.8 ± 0.05	$100.0_{-0.05}$	$100.0_{-0.05}$	$100.0_{-0.01}$	$100.0_{-0.05}$
ϵ^{AM}	99.0 ± 0.05	99.1 ± 0.05	94.9 ± 0.1	95.8 ± 0.1	97.8 ± 0.1	99.5 ± 0.1	97.8 ± 0.1	99.3 ± 0.2
ϵ^{CB}	99.9 ± 0.05	99.9 ± 0.05	98.4 ± 0.1	98.5 ± 0.1	99.3 ± 0.05	99.4 ± 0.1	99.1 ± 0.1	99.3 ± 0.2
$\epsilon^{SR \rightarrow CB}$	98.8 ± 0.05	98.9 ± 0.05	91.4 ± 0.2	92.8 ± 0.2	95.2 ± 0.1	97.3 ± 0.2	95.0 ± 0.1	97.2 ± 0.3

Table 6: Efficiencies up to the combination builder, for $p_T \geq 3$GeV/c

→ AM step efficiencies within requirements

→ Legacy bank performances (*road rates and fakes*)

→ Values given for PU+4tops events

		PU conditions	
		140	**200**
Barrel	***Matched road rate (in roads/BX/tower)***	**30,2**	**40,4**
	95% limit (in roads)	**123**	**149**
	Fake road proportion (in %)	**19,0**	**32,2**
Hybrid	***Matched road rate (in roads/BX/tower)***	**28,1**	**42,4**
	95% limit (in roads)	**108**	**141**
	Fake road proportion (in %)	**37,2**	**53,6**
Endcap	***Matched road rate (in roads/BX/tower)***	**19,5**	**28,1**
	95% limit (in roads)	**69**	**92**
	Fake road proportion (in %)	**24,3**	**28,1**

→ Well within requirements at PU140 (95% limit a bit too large for the barrel, but OK). Situation is a bit worse at PU200, but relatively acceptable.

→ Fake rate larger in hybrids because matching threshold lower (*4 inst. of 5*)

→ Current tracker geometry will evolve in the coming weeks. This should not impact the efficiency of our approach (*apart endcap tower rate reduction*).

→ Data transmission/formats from modules to the PRM is still not frozen, some important points must be solved asap:

- **Modules to DTC cabling**
- **PRB to PRM data format conversion**

→ The latest results on the AM stage are quite encouraging, we have good (*ie within requirements*) performances with 1M patterns banks (*1.5M for hybrid*) for most of the towers. More than sufficient for the demonstrator.