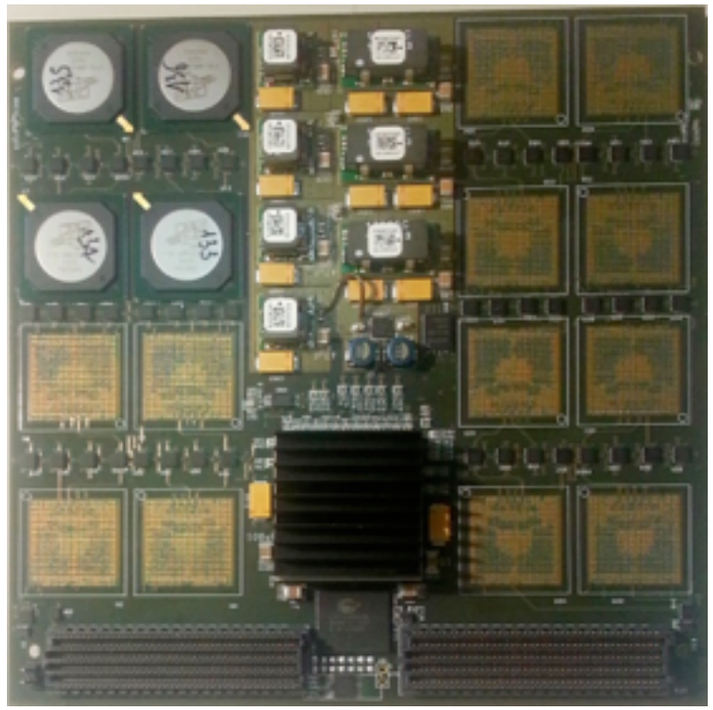
Experiences with the INFN Mezzanine

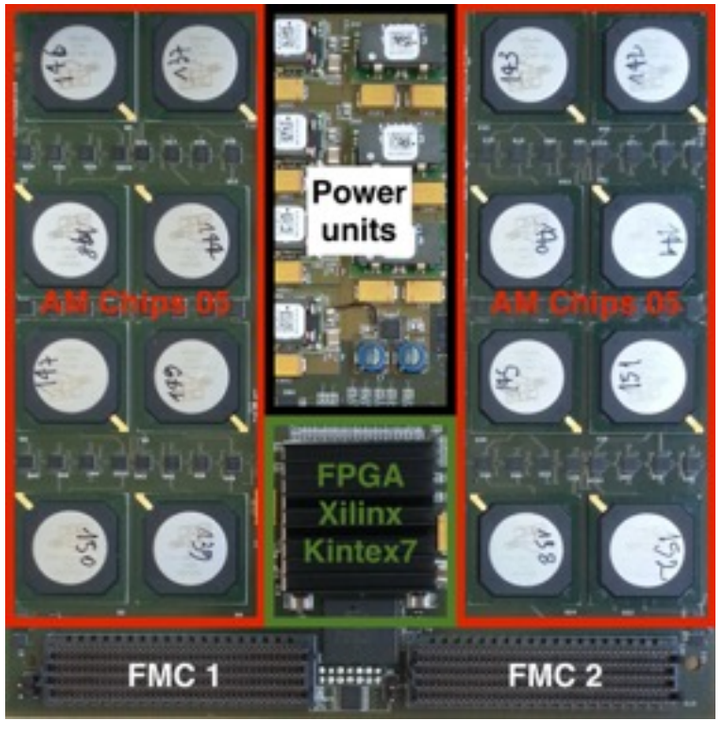
23 Sep 2015

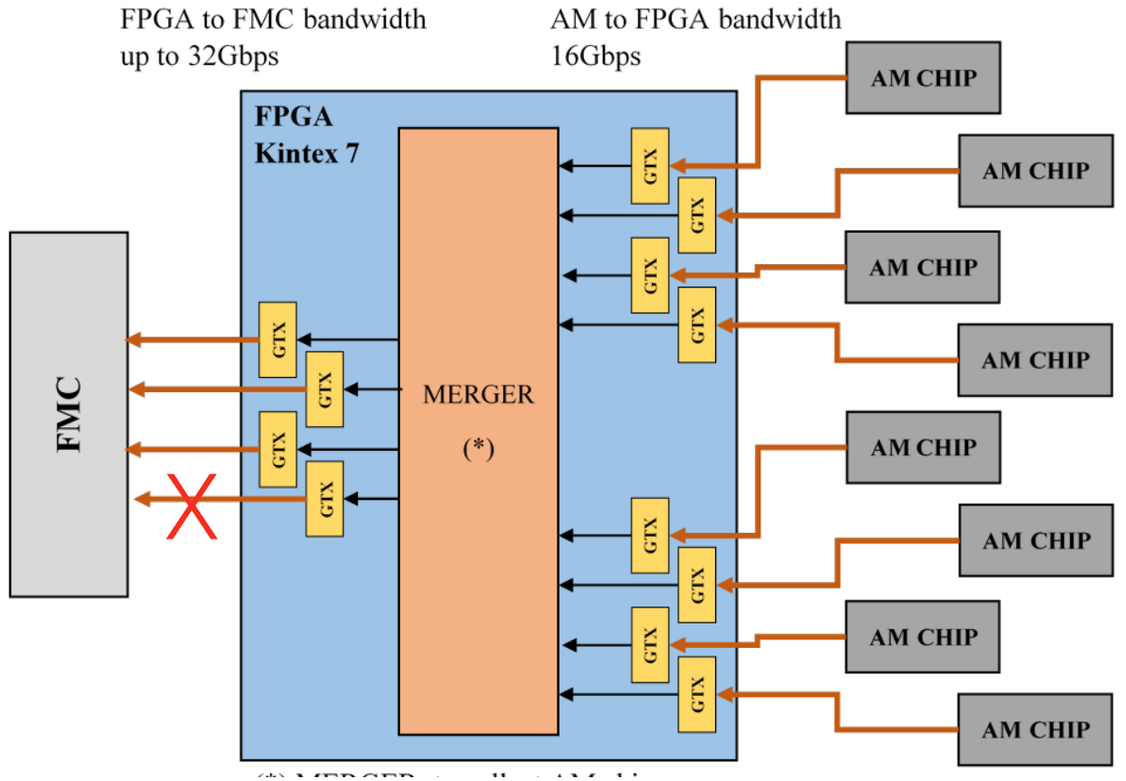
INtelligent Signal Processing for FrontIEr Research and Industry

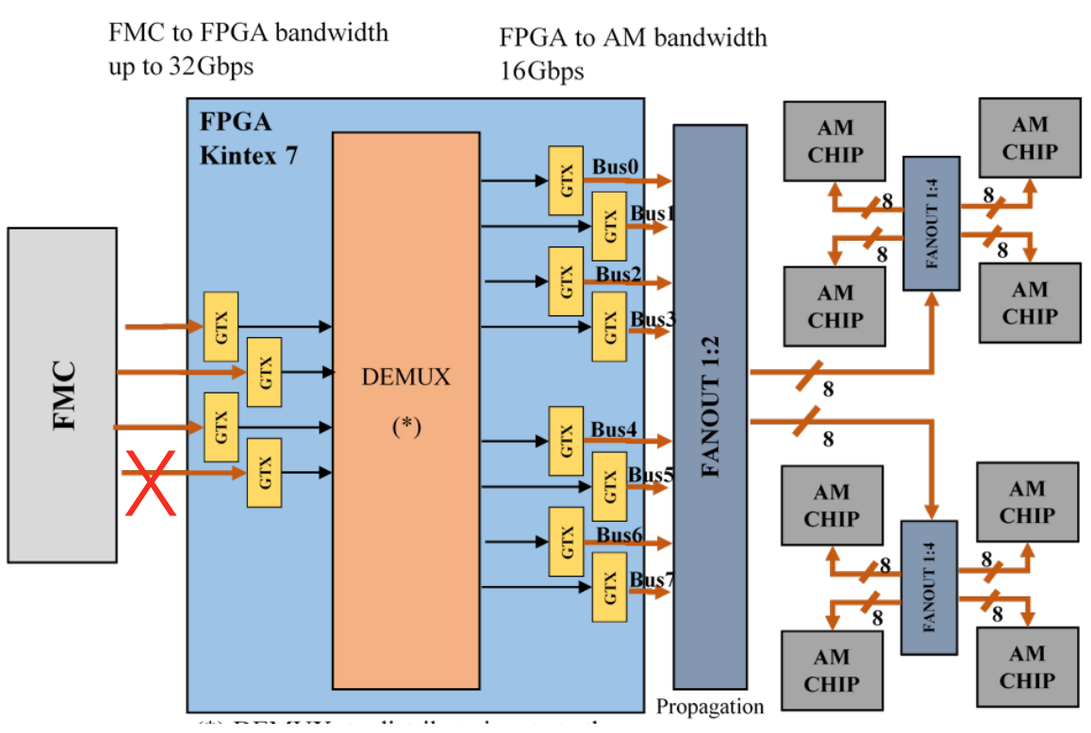
This project has received funding from the European Union's Seventh Framework Program for research, technological development and demonstration under grant agreement n° 317446

INFN Mezzanine

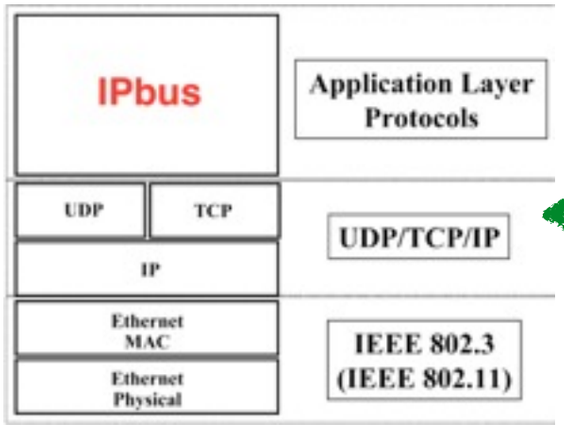


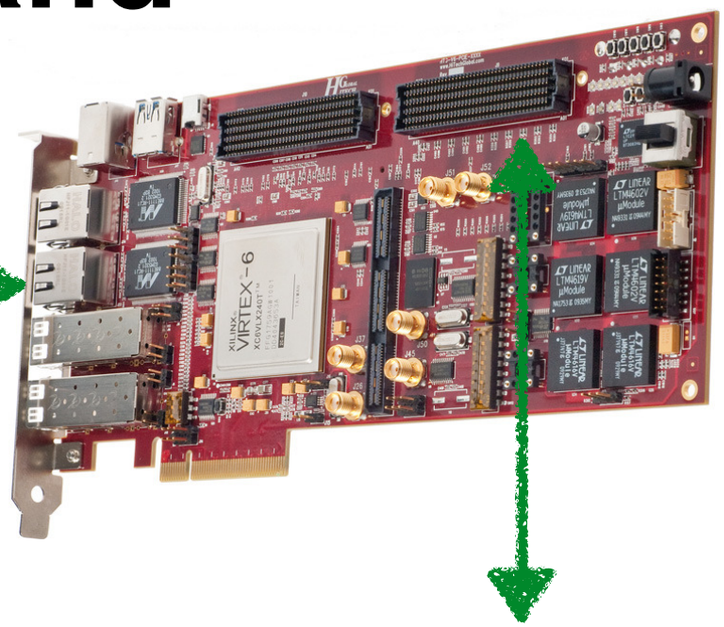






Mezzanine test stand





Virtex 6 firmware:

- Configures AM chip via JTAG
- Tests links (PRBS)
- Sends the hits via GTX@2Gbps to simulate real scenario

The Virtex6 firmware was changed to cope with the mezzanine test

- JTAG mainly software managed, no changes in the firmware
- JTAG links pass trough the Kintex7 and reach the AM chips (JTAG chained)
- Currently only the reset of Kintex7 GTX is done via Virtex6 software

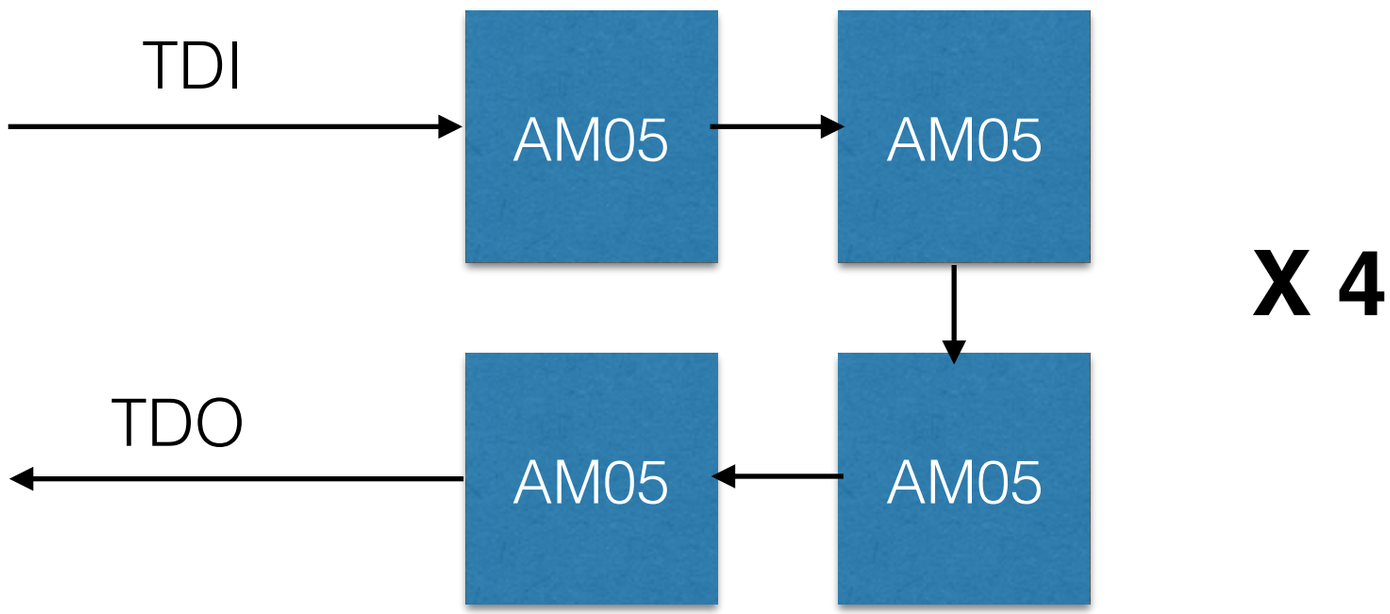
AM chip JTAG

JTAG commands are wrapped into IPbus packets and sent to the Virtex6 (evaluation board) where the JTAG commands are unwrapped and interpreted by a FSM. The JTAG connections pass through the FMC connector and the Kintex7 (mezzanine) and reach the 4 AM chips in daisy-chain.

Actions:

- The single-test-chip Python scripts have been modified to work with a chain of 4 chips
- Retrieving of IDCODEs
- Configuration of AM chip SerDes:
  - PRBS test (in/out)
  - Normal operation (IDLE)

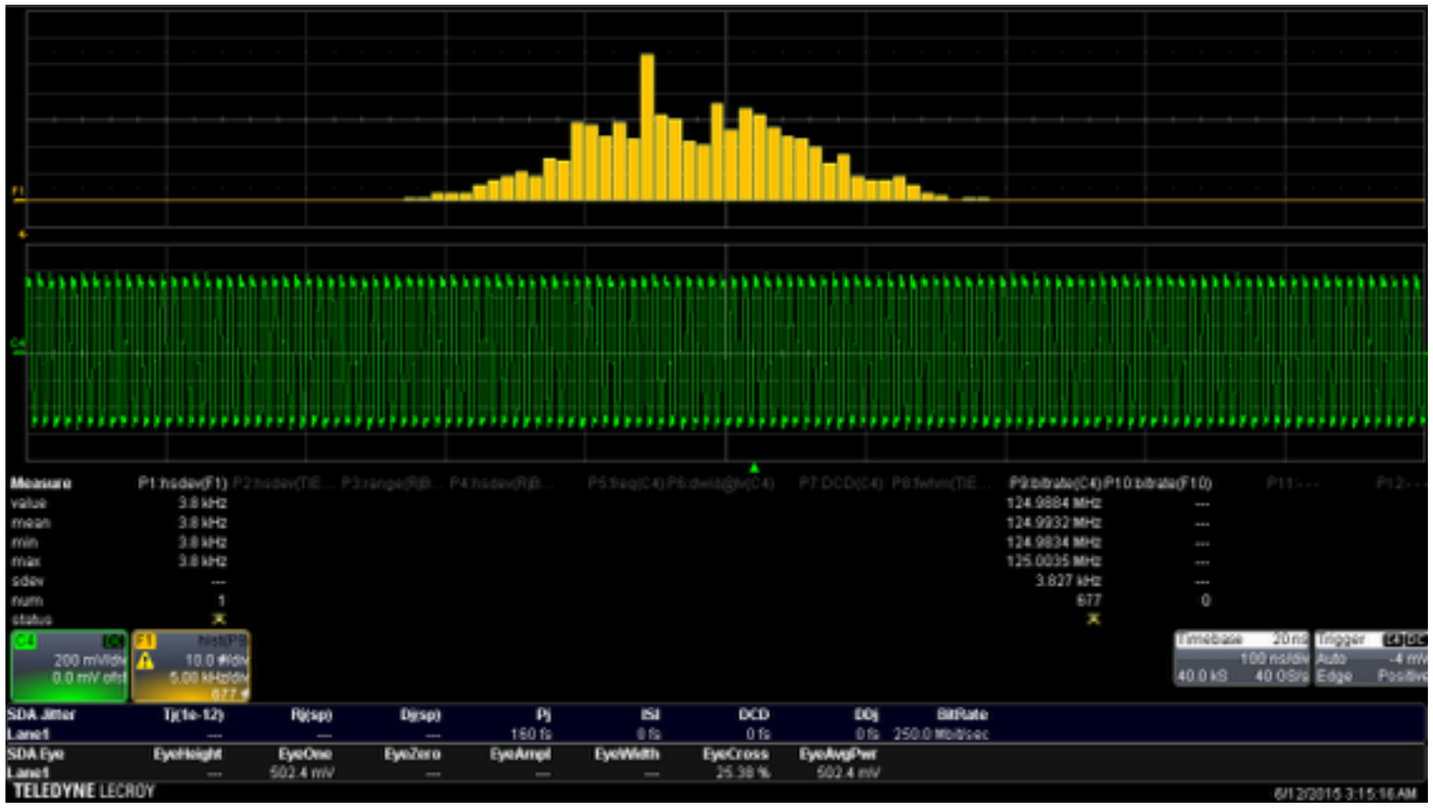
```
GetIDCODE:      0 50004071
GetIDCODE:      1 50004071
GetIDCODE:      2 50004071
GetIDCODE:      3 50004071
```



X 4

GTX reference clock

- The Kintex7 (mezzanine) GTX bit rate is 2 Gbps with a reference clock of 125 MHz.
- The 125 MHz clock is generated by ICS844021I (clock multiplier x5) and by a crystal @25 MHz.
- The crystal component had a wrong pin assignment
- The issue was **fixed** by crystal rotation



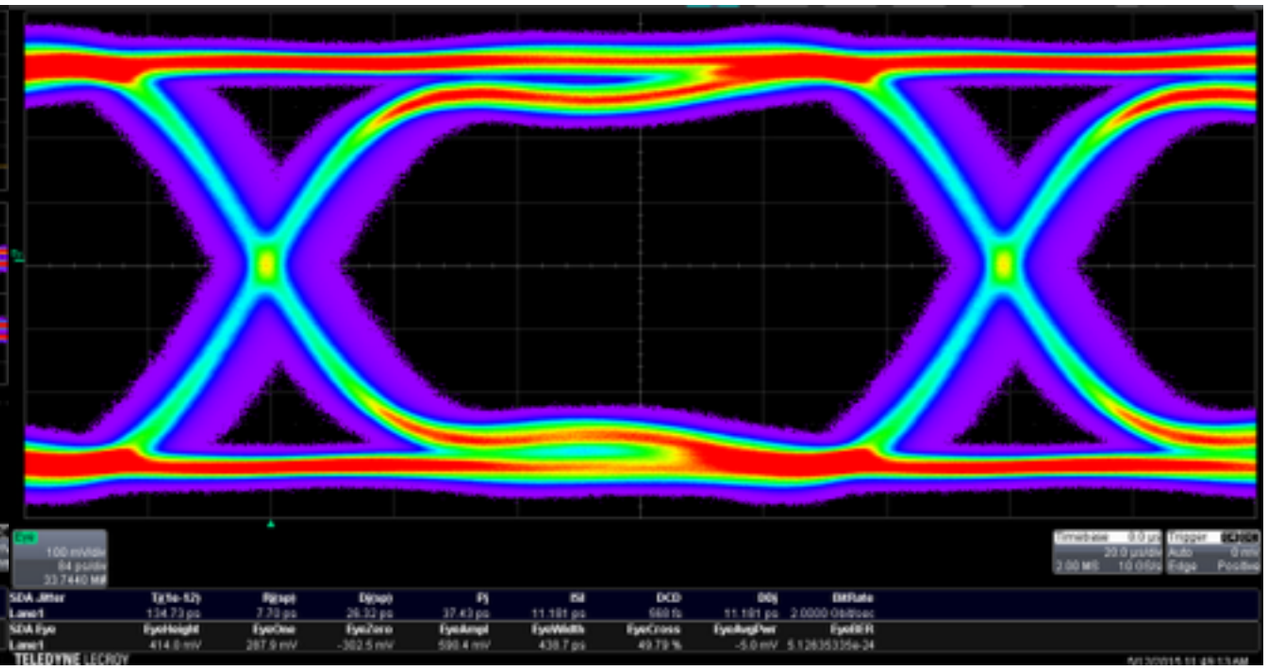
Correct the pin assignment

Frequency: 124.9932 MHz
Standard dev.: 3.8 KHz

AM chips <-> FPGA links

- Each AM chip:
  - 8 SerDes input -> 8 links FPGA -> AM chips (fanouts)
  - 1 SerDes output -> 4 links AM chips -> FPGA
- SerDes are configured to run @ 2Gbps
- Can be configured in normal operation (IDLE) and in PRBS test
- Using a LeCroy 8 GHz Serial data analyzer we tested an output link near the FGPA
- **No errors measured in 8 hours BER<10^{-14}**

FPGA -> AM Chip
PRBS7 sequence identified
Bit rate: 2.0000 Gbps



AM chip -> FPGA
PRBS7 sequence identified
Bit rate: 2.0000 Gbps

Polarity inversion found between the fanout: no actual problem

Check systematically all the links

FPGA -> FMC connectors links

- The mezzanine links between FPGA and FMC connector were tested using a loopback card on the FMC connector
- Eye diagrams obtained with IBERT on Kintex7

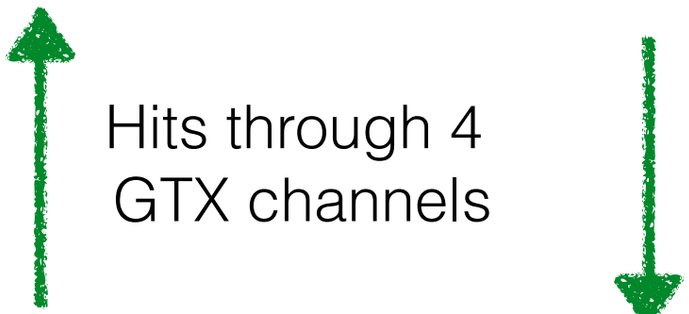
Link0 @ 8 Gbps

Link1 @ 8 Gbps

Link2 @ 8 Gbps

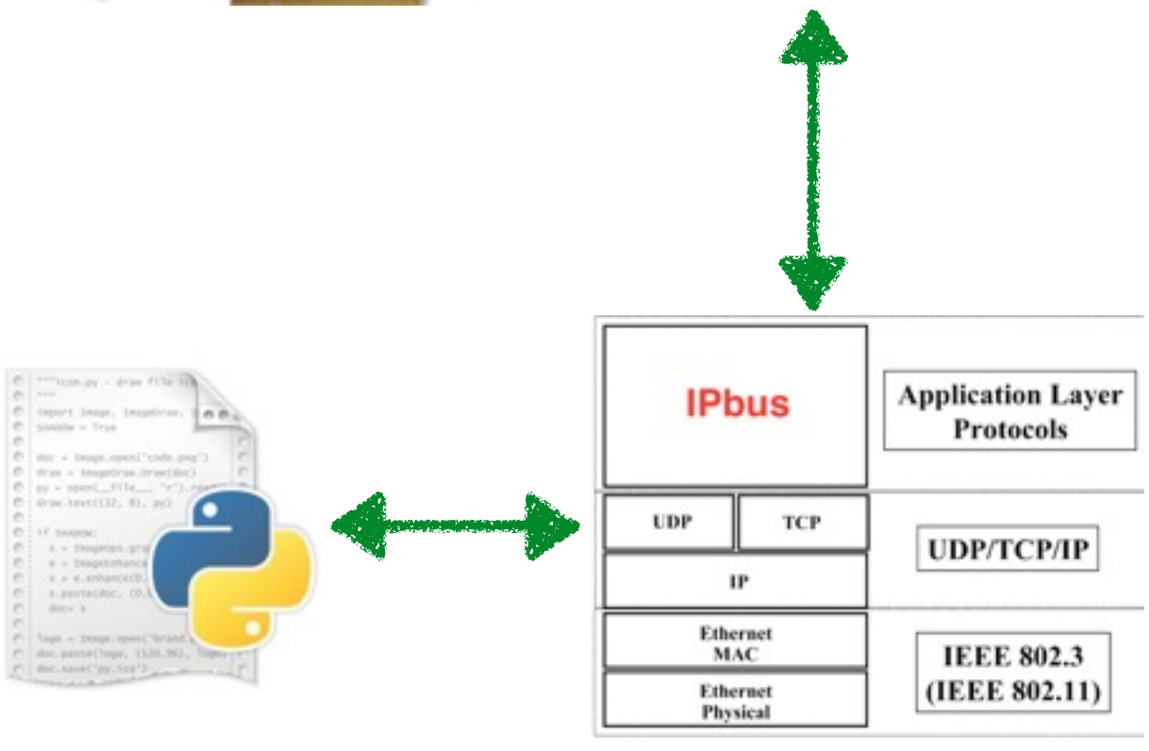
Characterize all the links with the data analiser

Realistic test- Logic



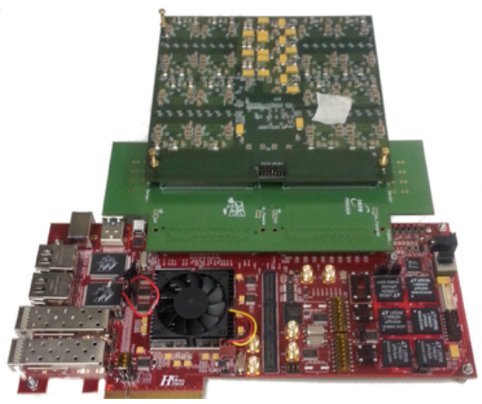
Hits through 4 GTX channels

Matched roads through 4 GTX channels



- Aim: test of the links with a more realistic test
  - send the hits from the evaluation board to the AM chips
  - retrieve in the evaluation board the matched roads from the AM chips

FMC issue



	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	RES1	GND
2	GND	CLK3_M2C_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK3_M2C_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK2_M2C_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
5	CLK2_M2C_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND
			LPC Connector	LPC Connector			LPC Connector	LPC Connector		

Table (11): Vita57 FMC Pin Assignment

- **VADJ FMC pins are connected with the 3.3 Volt pins.**
- **The evaluation board use the VADJ to bring 2.5 Volt ->**
- **The evaluation board didn't work**
- **Fixed removing the VADJ pins from the adaptor FMCs**

Remove the VADJ connection?

Mechanic and electric tests

- Two weeks were spent to integrate the INFN mezzanine with the PulsarIIb at FNAL
- First step: check the electric and mechanic compatibility
- Second step: check of the voltages on the mezzanine and the power consumption
- Initial step conclusion: no major issues were found, although some improvements could be done in the next mezzanine version

Single Pulsar test stand

Recommendations from Jamieson

1) the **JTAG TDO output from the mezzanine is 1.8V and the Pulsar2b board is expecting JTAG signals to be 3.3V levels**. This signal is buffered on the Pulsar2b so I don't think it should be a problem, though.

2) the Kintex-7 system monitor/ADC pins in bank 0 (VREF_P, VP_O) are grounded, so it **is not possible to monitor the internal temperature of this Kintex FPGA**. If aggressive firmware (e.g. lots of GTX transceivers in use, fast data/clock rates) is used a thermocouple probe should be attached to the Kintex part so we can check how hot things are running. (For simple IPBus loopback operations it should not even run warm.)

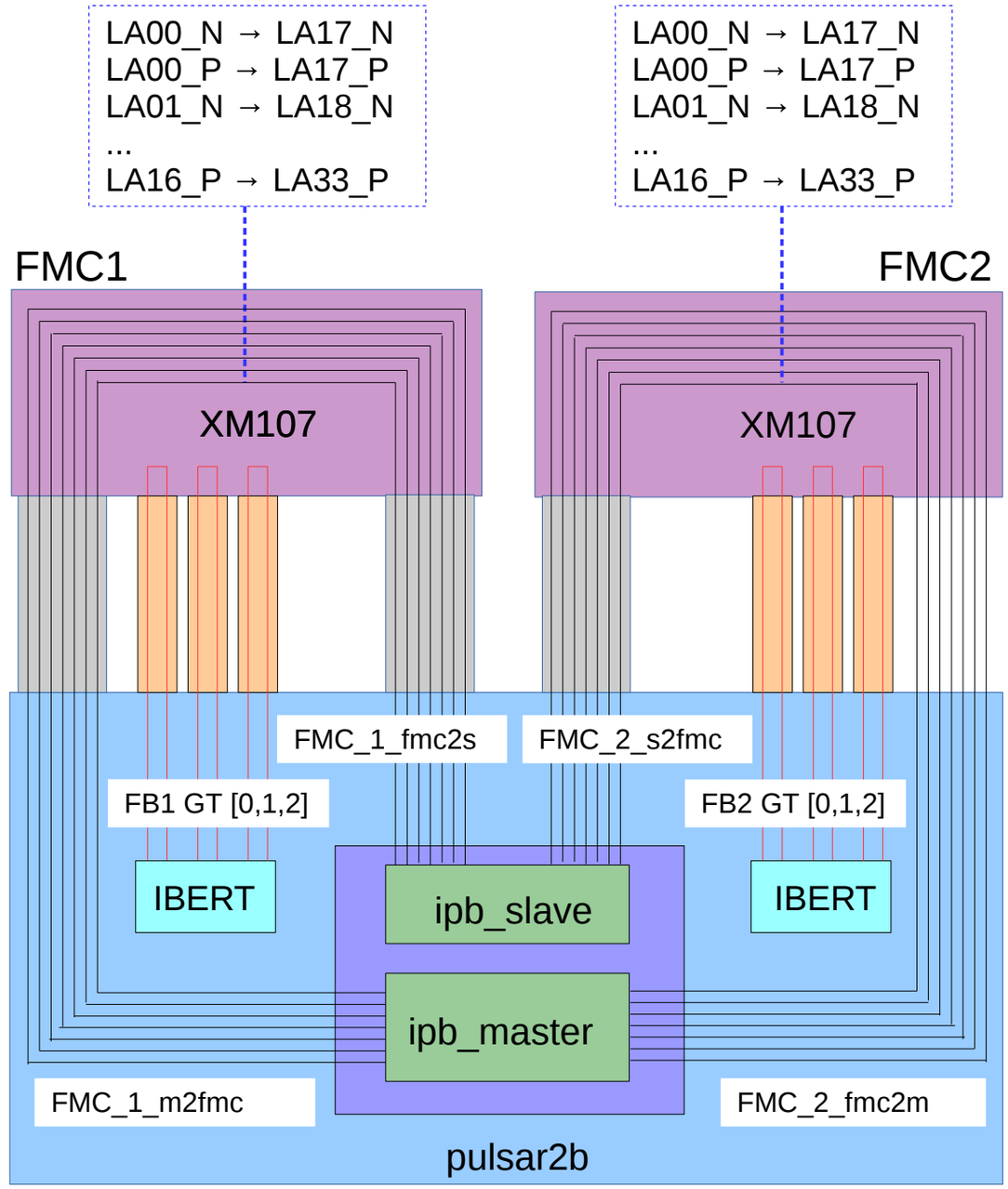
3) **the FMC LVDS lines (LA*, LB*, CLK_DW*, CLK_UP*) are connected to 2.5V I/O banks on the Kintex 355 FPGA**. All of these signals should use the "LVDS_25" I/O standard.

4) If one needs to send an LVDS clock from the mezzanine to the Pulsar2b board, use CLK<0> (CLK_UP_P0/CLK_UP_N0). No other FMC dedicated LVDS clocks are connected on the mezzanine.

5) If one needs to send an LVDS clock from the Pulsar2b to the Mezzanine, I recommend using LA_00 as this connects to a clock capable (CC) input pin pair in the K355 FPGA.

LVDS links

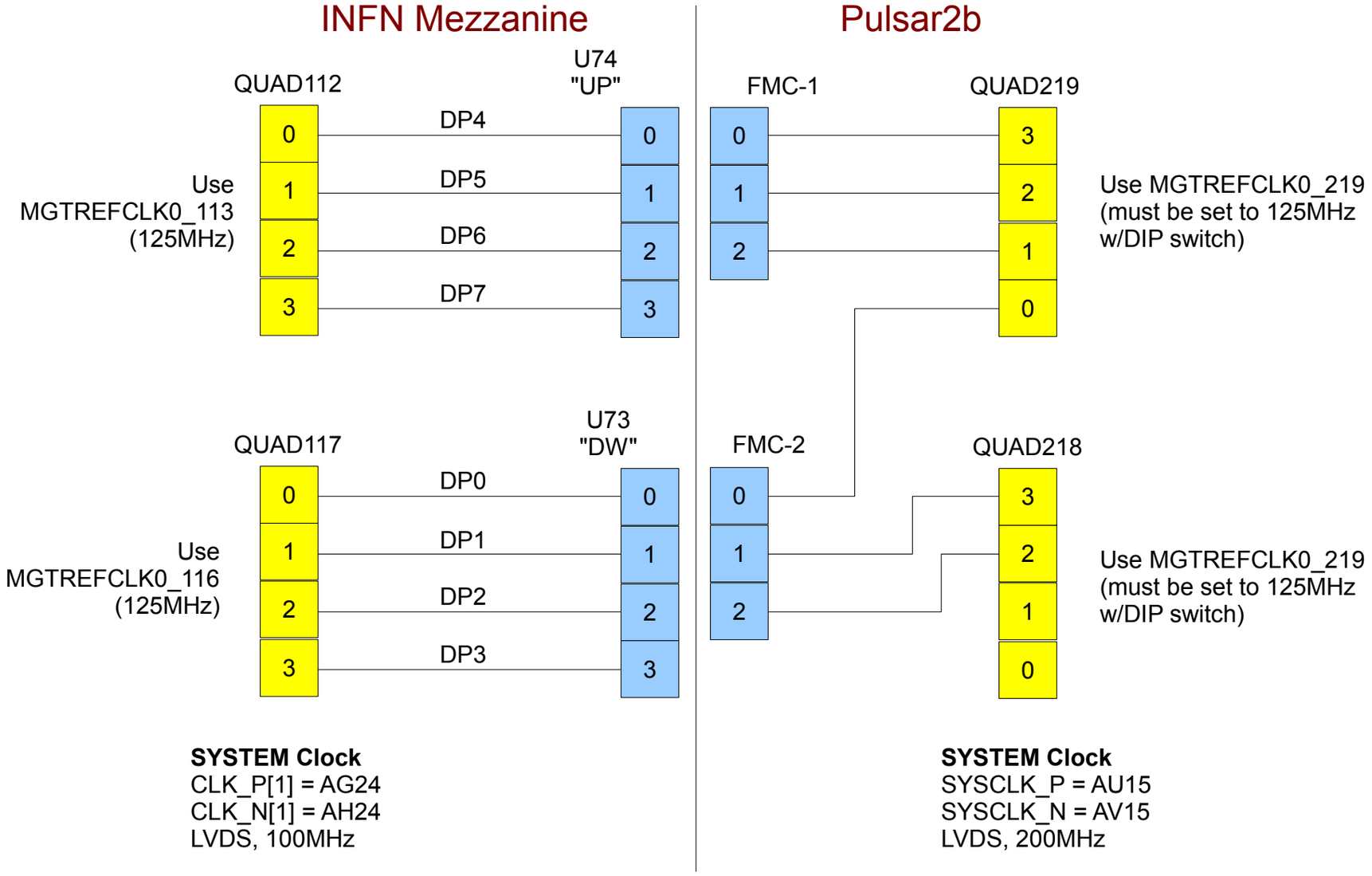
- The mezzanine+Pulsar were mounted on an ATCA shelf slot.
- We developed a Pulsar firmware which permitted to test the LVDS links (in a static way). The schematic on the right shows the principle of the tests.
- The Pulsar LVDS links were tested using the loopback cards and no problems were found.
- Then, the two loopback cards were removed and the mezzanine took their place. The green blocks were substituted by a VIO instance.
- I developed a mezzanine firmware which, paired with the Pulsar firmware, checked the LVDS lines using VIO.
- **All the 68 LVDS links worked properly and no swaps were found.**
- **In case we need more links we could use the DDR technique to double them.**



~half of the LVDS
and GTX links are swapped
(PulsarIIb)

Test of the GTX links

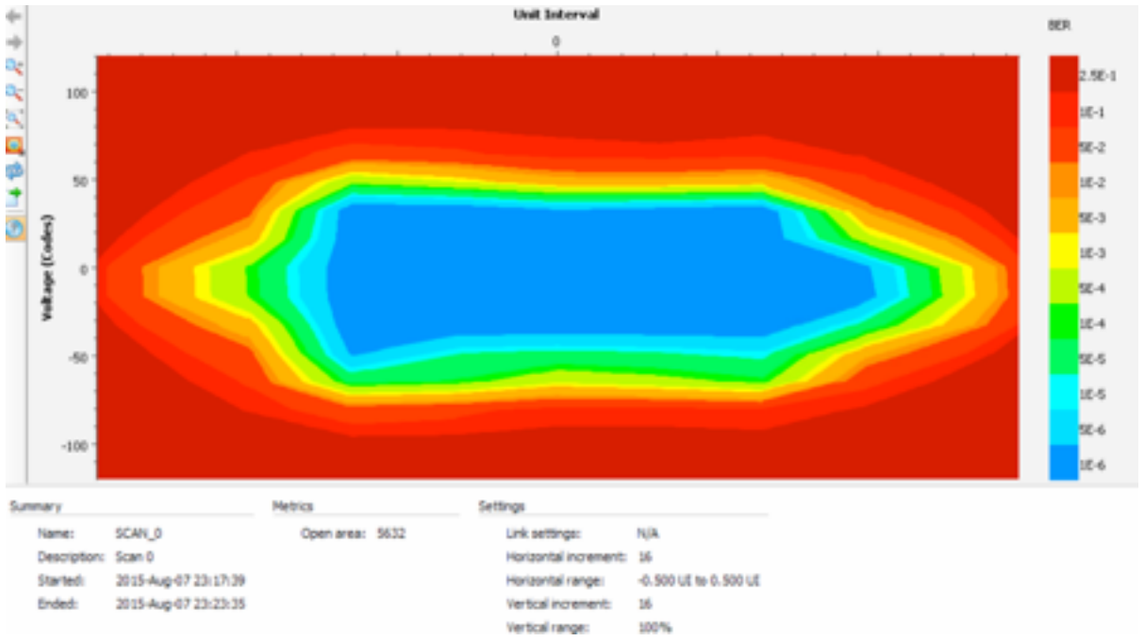
- The GTX links were tested using IBERT in the mezzanine and in the Pulsar firmwares

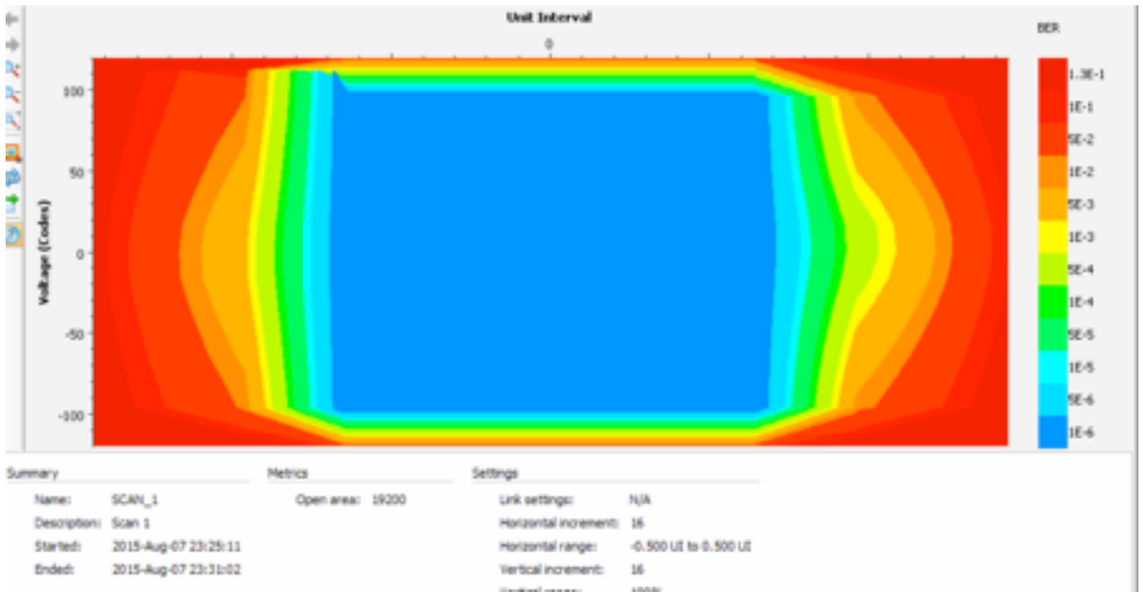


GTX links @4Gbps

- GTx running at 4Gbps are ok

Found Links (12)							Reset	PRBS 7-bit	PRBS 7-bit	Multiple	Multiple	Multiple
Found 0	MGT_X0Y39/TX	MGT_X0Y0/RX	4.000 Gbps	3.96...	0E0	2.525E-13	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)	0.00 dB (000...	269 mV (00...
Found 1	MGT_X0Y38/TX	MGT_X0Y1/RX	4.000 Gbps	3.96...	0E0	2.524E-13	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)	0.00 dB (000...	269 mV (00...
Found 2	MGT_X0Y37/TX	MGT_X0Y2/RX	4.000 Gbps	3.96...	0E0	2.525E-13	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)	0.00 dB (000...	269 mV (00...
Found 3	MGT_X0Y36/TX	MGT_X0Y20/RX	4.000 Gbps	3.96...	0E0	2.524E-13	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)	0.00 dB (000...	269 mV (00...
Found 4	MGT_X0Y35/TX	MGT_X0Y21/RX	4.000 Gbps	3.92...	0E0	2.548E-13	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)	0.00 dB (000...	269 mV (00...
Found 5	MGT_X0Y34/TX	MGT_X0Y22/RX	4.000 Gbps	3.92...	0E0	2.548E-13	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)	0.00 dB (000...	269 mV (00...
Found 6	MGT_X0Y22/TX	MGT_X0Y34/RX	4.000 Gbps	3.92...	0E0	2.547E-13	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB (000...	1018 mV (1...
Found 7	MGT_X0Y21/TX	MGT_X0Y35/RX	4.000 Gbps	3.92...	0E0	2.547E-13	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB (000...	1018 mV (1...
Found 8	MGT_X0Y20/TX	MGT_X0Y36/RX	4.000 Gbps	3.92...	0E0	2.546E-13	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB (000...	1018 mV (1...
Found 9	MGT_X0Y2/TX	MGT_X0Y37/RX	4.000 Gbps	3.92...	0E0	2.546E-13	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB (000...	1018 mV (1...
Found 10	MGT_X0Y1/TX	MGT_X0Y38/RX	4.000 Gbps	3.92...	0E0	2.545E-13	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB (000...	1018 mV (1...
Found 11	MGT_X0Y0/TX	MGT_X0Y39/RX	4.000 Gbps	3.92...	0E0	2.545E-13	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB (000...	1018 mV (1...





GTX links @8Gbps

- The links were not ok running at 8Gbps
- A lot of errors and link instability were found

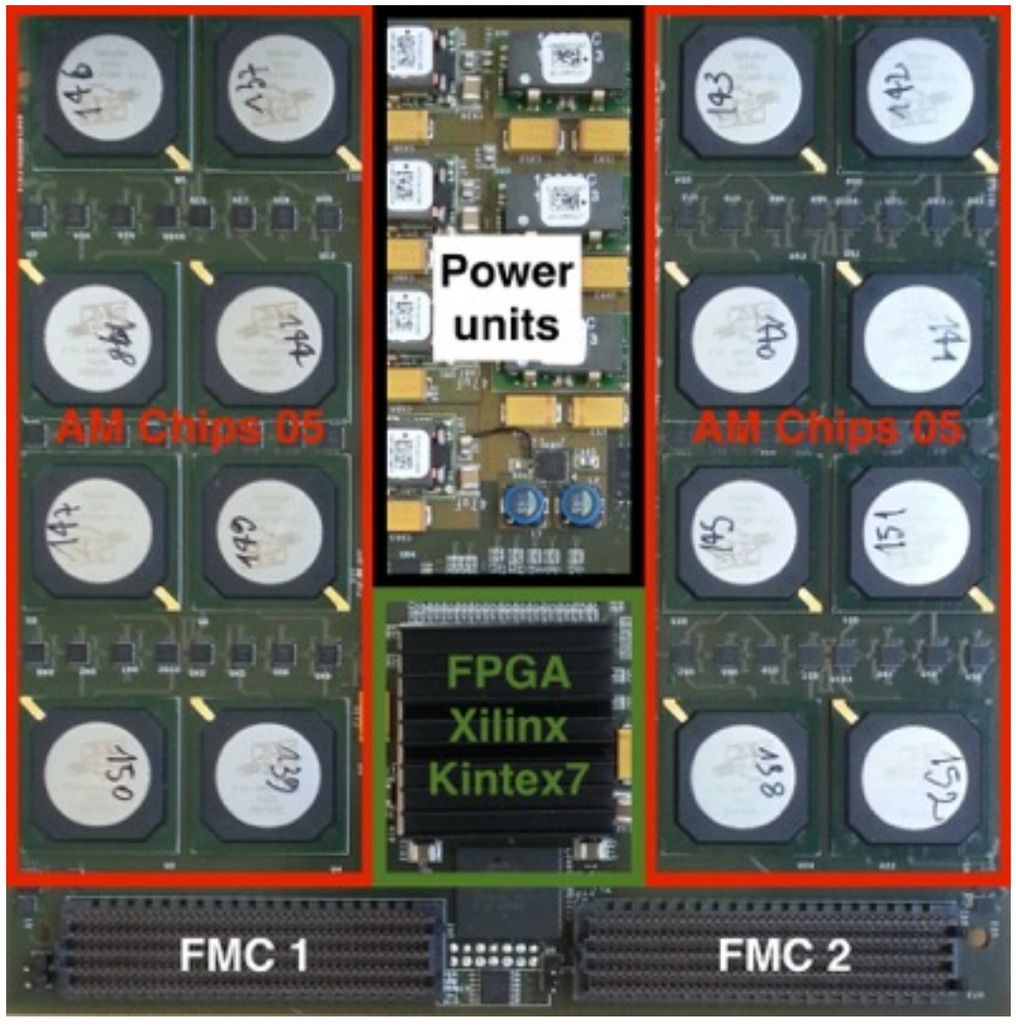
Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE Enabled
Ungrouped Links (0)													
Found Links (11)							Reset	PRBS 7-bit	PRBS 7-bit	Multiple	Multiple	Multiple	☑
Found 0	MGT_X0Y22/TX	MGT_X0Y34/RX	8.000 Gbps	1.422E12	1.07E9	7.527E-4	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB (000...	1018 mV (1...	☑
Found 1	MGT_X0Y21/TX	MGT_X0Y35/RX	8.000 Gbps	1.423E12	8.349E8	5.867E-4	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB (000...	1018 mV (1...	☑
Found 2	MGT_X0Y20/TX	MGT_X0Y36/RX	8.000 Gbps	1.352E12	1.086E9	8.032E-4	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB (000...	1018 mV (1...	☑
Found 3	MGT_X0Y2/TX	MGT_X0Y37/RX	8.000 Gbps	1.354E12	2.188E9	1.616E-3	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB (000...	1018 mV (1...	☑
Found 4	MGT_X0Y1/TX	MGT_X0Y38/RX	8.000 Gbps	1.354E12	1.719E9	1.269E-3	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB (000...	1018 mV (1...	☑
Found 5	MGT_X0Y0/TX	MGT_X0Y39/RX	8.000 Gbps	1.355E12	3.215E9	2.373E-3	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB (000...	1018 mV (1...	☑
Found 6	MGT_X0Y39/TX	MGT_X0Y0/RX	7.999 Gbps	1.356E12	4.938E9	3.642E-3	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)	0.00 dB (000...	269 mV (00...	☑
Found 7	MGT_X0Y38/TX	MGT_X0Y1/RX	7.999 Gbps	1.357E12	4.366E9	3.217E-3	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)	0.00 dB (000...	269 mV (00...	☑
Found 8	MGT_X0Y36/TX	MGT_X0Y20/RX	7.999 Gbps	1.358E12	4.147E9	3.053E-3	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)	0.00 dB (000...	269 mV (00...	☑
Found 9	MGT_X0Y35/TX	MGT_X0Y21/RX	7.999 Gbps	1.358E12	3.911E9	2.88E-3	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)	0.00 dB (000...	269 mV (00...	☑
Found 10	MGT_X0Y34/TX	MGT_X0Y22/RX	7.999 Gbps	1.359E12	2.445E9	1.798E-3	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)	0.00 dB (000...	269 mV (00...	☑
Link Group 8 (1)							Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)	0.00 dB (000...	269 mV (00...	☑
Link 41	MGT_X0Y37/TX	MGT_X0Y2/RX	7.999 Gbps	2.844E12	1.478E12	5.197E-1	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)	0.00 dB (000...	269 mV (00...	☑

- No time to address this issue, since it was discovered at the end of the testing period

-In order to run at 8 Gbps
we need to configure properly the TXDiffSwing
-Same feedback from Kristian who tested the
Pulsar links with a loopback card

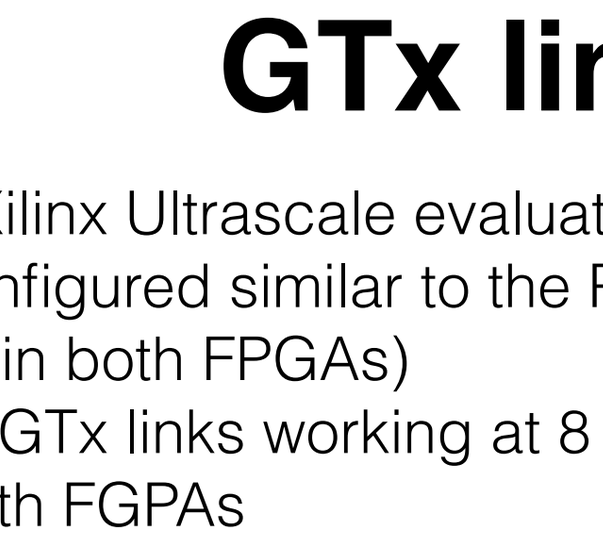
16 AM chip mezzanine

- We received the 16 AM chip mezzanine
- Smoke tests were ok
- JTAG connections to the FPGA and to the first chain of 4 AM chips is ok
- The GTX reference clock was fixed and improved
- **We received the board with only one rotated crystal (we asked for both crystals to be rotated) and it was even broken**
- **Ordered new crystals**



GTx link test @Pisa

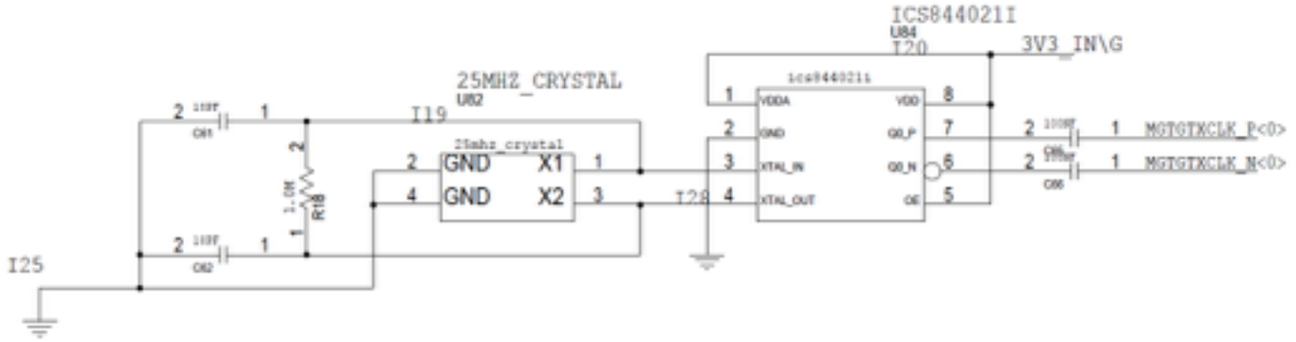
- We used an Xilinx Ultrascale evaluation board
- Test stand configured similar to the PulsarIIb+mezzanine setup (IBERT in both FPGAs)
- We make the GTx links working at 8 Gbps configuring the GTx of both FGPAs
- The evaluation board has only 5 links connected out of 8
- Sporadic errors were anyway found. Using the data analyzer we found that the reference clock may inject too much jitter into the GTx signal



- For the 16 AM chip mezzanine we decided to use a better quartz component of the GTX reference clock
- Indeed, the jitter of the reference clock was reduced and the GTx didn't show any error in some hours of continuous working

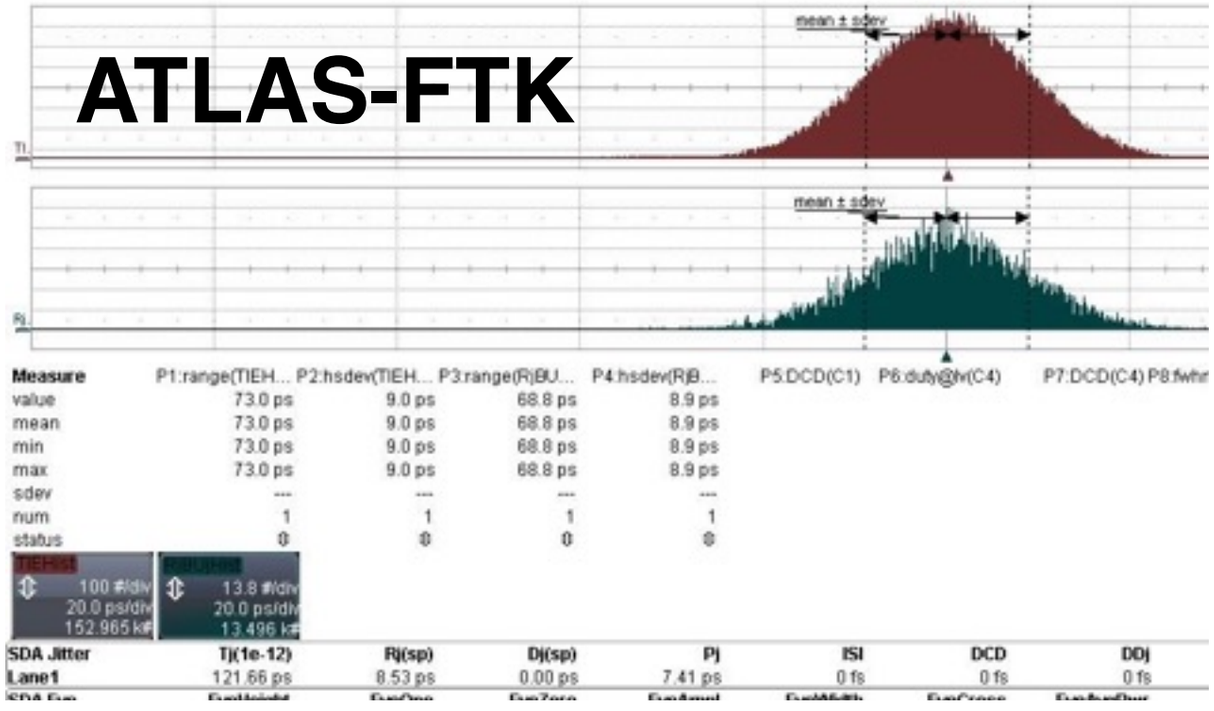
Clocks

- 100 MHz clock for the FPGA
- 4x100 MHz clock for the AM chips (fanout)
- 2x125 MHz clock for the GTX RefClock

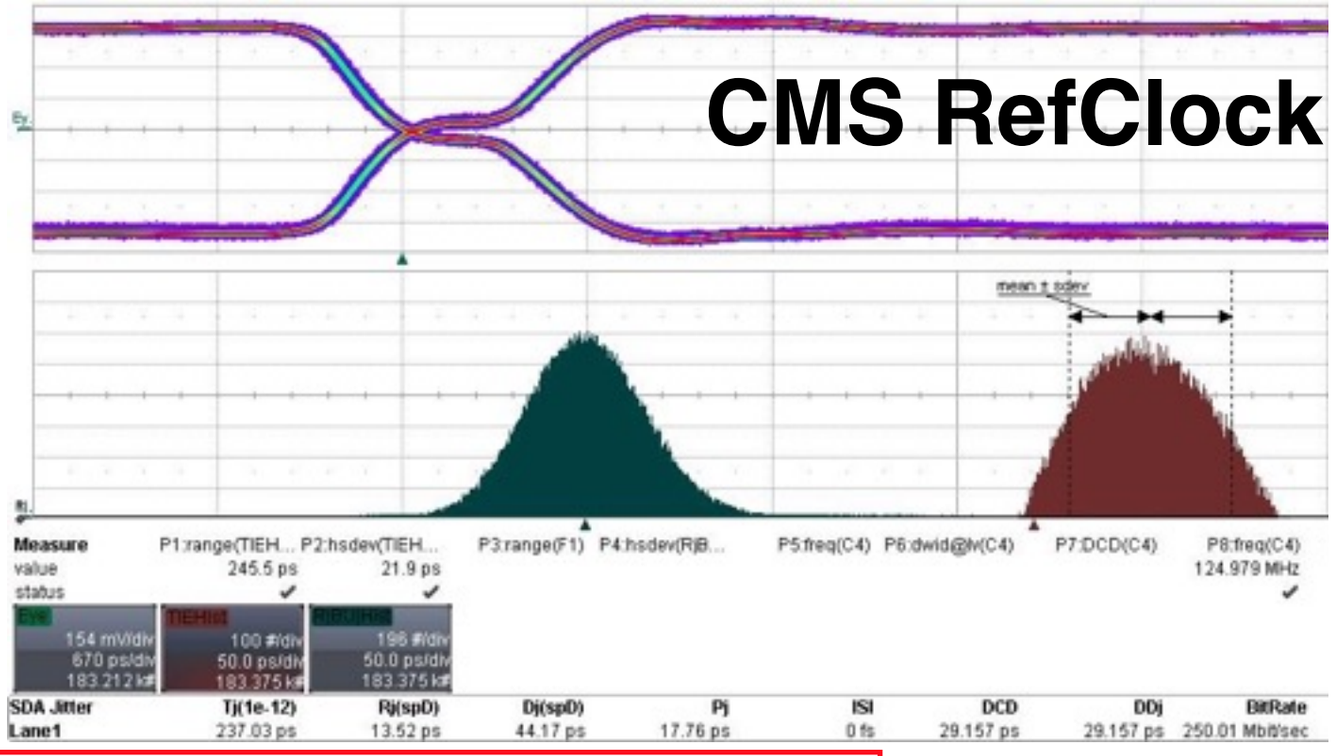


- 100 MHz clocks are ok
- 125 MHz source of issues (pin assignment, jitter)

ATLAS-FTK



CMS RefClock



- To simplify the clock it's maybe better to use a single component
- It may be useful to have programmable clocks (I2C) at least for the GTX RefClock

Serial link for DO-TF configuration

- Implemented an LVDS serial link
- Takes up 5 differential pairs, 1 for the clock, 4 for the data
- Width on the parallel ends is 32 bits
- Speed is 400MHz DDR, which gives 3.2GBits/s (100MT/s for the parallel data)
- Simple custom logic has been developed for data eye calibration and word alignment
- Up so far, link has been tested to have a BER < $2.5 \cdot 10^{-13}$ (0 errors so far) which can be considered sufficient for a one-time communication for configuration (not a full-time link)

Validate all the links

Additional feedbacks

- Temperature sensors (connected with the ATCA shelf manager?)
- Test points and leds
- Mechanic connection: add screws in the middle of the FMC connectors, the current screws are too close to the components
- Additional power close FMC (Jumpers) connected to GND-12V while in the mezzanine is 12V-12V

- Power connectors
- Ethernet connection
- Problem of space: mezzanine's mezzanine?

- GTX max. speed.